VT-1100A/1105A/1310A/1305A

HITACHI
SERVICE MANUAL

TK No. 2508E

VT-1100A/1105A
1310A/1305A

Technical Information

VHS
THIS VIDEO DECK IS A VHS TYPE VIDEO RECORDER.
FOR PROPER OPERATION, ONLY THE VHS TYPE CASSETTE MUST BE USED.

SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

VIDEO CASSETTE RECORDER

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Y CHASSIS SYSTEM CONSISTENCY

The following table shows the differences from X chassis system consistency on Y chassis VTR.

#	ISSUE	(X) CHASSIS	(Y) CHASSIS	
1	Tape speed selector	The selector is lock type switch	The SW is momentary type, and the default value is EP when AC is plugged in.	
2	At the index mark when VTR is rewind and IRT is set.	There are two type 1) Continue to rewind. 2) Start IRT	Continue to rewind.	
3	Memory on/off and counter clear operation	1) It's always allowed whether the display shows tape remain or counter. 2) It's allowed only when the counter is displayed.	OSD Counter Model It's always allowed. FL Counter Model It's allowed only when the counter is displayed.	
4	Memory stop	1) The VTR stops only when the display mode is counter and memory is on. 2) The VTR always stop when memory is on.	The VTR always stop when memory is on.	
5	Timer program menu of 4-program/2-week Timer	Three normal/daily programs and one weekly program.	All the 4 programs are free to program as normal, weekly or daily.	**
6	50/60Hz AC clock base decision	Only one time when AC cord is plugged in.	All the time in every clock pulses.	**
7	Memory stop mode	Rew, A.dub, V.dub	Few, A.dub, V.dub and F.FWD	**
8	Index mark recording for continuous Timer program	The VTR unloads tape at the boundary of Timer Program, then loads tape and writes index mark.	Without unloading, the VTR can write index mark at the boundary of Timer program.	**
9	Start of Timer program & IRT	The VTR begins recording at just start time.	The VTR begins recording at 5 sec before the start time.	**
10	Clock setting operation	Push both CLOCK & ENTER buttons.	Push CLOCK button first, then one finger operation is possible.	**
11	Local slow operation	No way without SLOW button.	Push PLAY button under still picture.	**

** New item.

DIFFERENCE BETWEEN VT-63A and VT-1100A/1105A (CIRCUIT)

MODEL ITEM		VT-63A	VT-1100A/1105A
CHASSIS		X	Y
LUMA	H Q	NO	YES
	DOC (ELEMENT)	FM (GLASS)	VIDEO (CCD)
CHROMA			(IC IS CHANGED)
CYLINDER	SHAPE		MOUNT TYPE OF PRE-AMP
	VIDEO HEAD	2 HEADS	2 HEADS
	MOTOR	SINGLE PHASE	3-PHASE
SERVO	SLOW	NONE	NONE
	STILL	FRAME	FRAME
	F. ADV.	NONE	NONE
	NOISE LOCK SEARCH	NONE	YES
SYSTEM	MODE DISPLAY	YES (LED)	YES (LED)
	TAPE SPEED DISPLAY	YES (LED)	YES (FL)
	TAPE SPEED SWITCH	SLIDE	TACT
	CLOCK BUTTON	HOLD TYPE	TACT TYPE
	POWER LED	YES	YES
TUNER	SHAPE	UNIT TYPE	MOUNTED ON P.C.B
CABINET	MATERIAL	PLASTIC	METAL

1. POWER SUPPLY

Fig. 1-1 and 1-2 show the generation circuits of power sources necessary for the various circuits in the VT-1100A. The power generation circuits are located on four circuit board assemblies - REG/CYL MOTOR DRIVE, U/V TUNING, TIMER INPUT KEY and MAIN.

These power sources can be roughly divided into two.

- 9 power sources generated when power is supplied to the VTR:
  AC4V, A30V, A-30V, A5.6V, BU5V, A5V, A18V, M12V, A12V.
- 3 power sources generated when the power switch is turned ON:
  5V, 10V, 12V.

Table 1-1 shows the specifications and applications of these 12 power sources.

POWER ON/OFF

The power sources, 5V, 10V and 12V, which are generated when the power switch is turned ON are switched ON/OFF by system control μP (IC901: S-μP). To perform this control, the S-μP receives the operation data of power switch (S111: Push-type Switch) as shown in Fig. 1-2, input to timer μP (IC751: T-μP or TI-μP), via the communications lines. S-μP turns the output of the power holding memory in the IC to ON and OFF alternately every time S-μP receives data. The memory output is derived from pin 6 and goes "Hi" when the power switch is turned ON. The output (Hi) at pin 6 turns on the 12V B+ Switches (Q851, Q852). This causes the A12V source to be output via Q852. This output becomes a 12V power source. This 12V source is dropped by 1.8V to 10.2V via the voltage drop diodes (D502 - D505), thus the 10V source is produced. The 12V power source is also applied to pin 2 of 5V regulator (IC851). This activates the 5V regulator and the 5V source is output from pin 1.

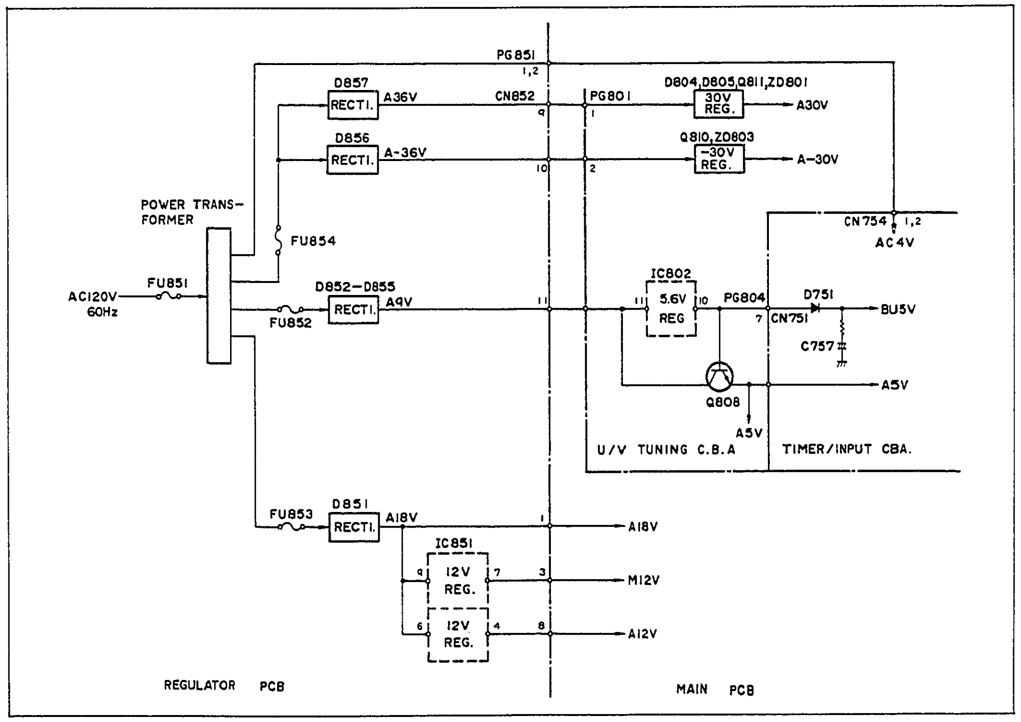

PG851
1,2
D857
RECTI.
A36V
CN852
9
PG801
1
D804,D805,Q811,ZD801
30V REG.
A30V
D856
RECTI.
A-36V
10
2
Q810,ZD803
-30V REG.
A-30V
POWER TRANS-FORMER
FU854
CN754
1,2
AC4V
AC120V
60Hz
FU851
D852—D855
RECTI.
A9V
FU852
11
IC802
11
5.6V REG
10
PG804
7
CN751
D751
BU5V
C757
Q808
A5V
A5V
U/V TUNING C.B.A
TIMER/INPUT CBA.
FU853
D851
RECTI.
A18V
1
A18V
IC851
9
12V REG.
7
3
M12V
6
12V REG.
4
8
A12V
REGULATOR PCB
MAIN PCB

Fig. 1-1 Simplified Power Supply (Always) Circuit Diagram

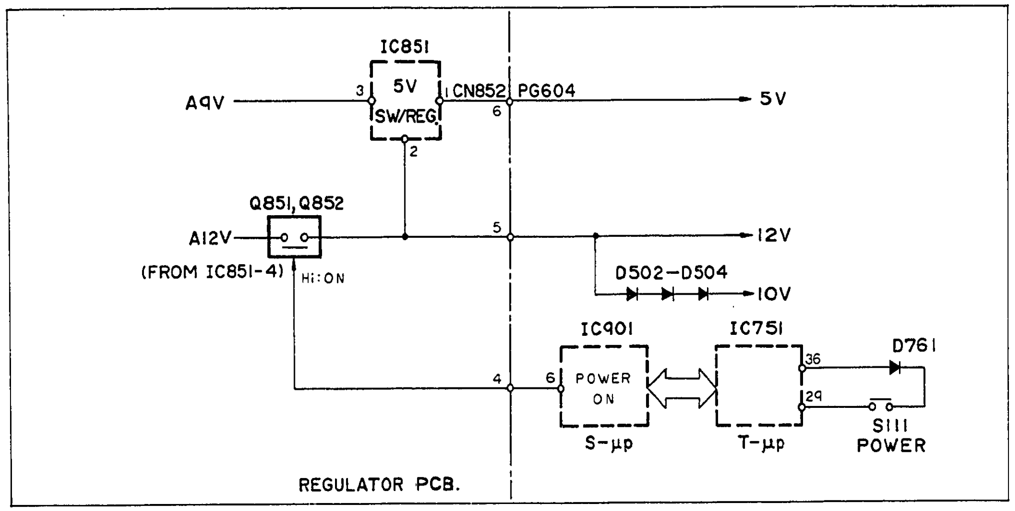

IC851
5V
SW/REG
A9V
3
CN852
PG604
6
5V
2
Q851,Q852
A12V
(FROM IC851-4)
Hi:ON
5
12V
D502–D504
10V
IC901
IC751
D761
4
6
POWER ON
36
29
S-μp
T-μp
S111
POWER
REGULATOR PCB.

Fig. 1-2 Simplified Switched Power Supply Circuit Diagram

	Power supply	Voltage	Generator (location)	Active Mode	Application
1	AC4V	AC4.1V (Unregulated)	Power transformer (REG)	Always	Heater in digital multidisplay
2	A30V	30V (Regulated)	Cathode of ZD801 (U/V TUNING)	Always	Tuning voltage generator circuit
3	A-30V	-30V (Regulated)	Emitter of Q810 (U/V TUNING)	Always	EAROM and timer μP for digital multidisplay
4	A5.6V	5.6V (Regulated)	Pin 10 of IC802 (U/V TUNING)	Always	IR receiver
5	BU5V	5V (Regulated)	C758/759 (TIMER)	Always	Timer μP (This power supply is backed up by C758/759 for approx. 1 sec.)
6	A5V	5V (Regulated)	Emitter of Q808 (U/V TUNING)	Always	9 LEDs, EAROM, tuning μP and system control μP
7	5V	5V (Regulated)	Pin 1 of IC851 (REG)	Power ON	Servo & Luminance/Chroma process IC, cylinder motor drive
8	A18V	18V (Unregulated)	Cathode of D3 (REG)	Always	Capstan motor drive
9	M12V	12V (Regulated)	Pin 7 of IC851 (REG)	Always	Loading and cylinder motor drivers
10	A12V	12V (Regulated)	PIN 4 of IC851 (REG)	Always	Loading motor driver & end lamp
11	10V	10.2V (Regulated)	Cathode of D504	Power ON	CCD 1H delay line on luminance/chroma board
12	12V	12V (Regulated)	Collector of Q851 (REG)	Power ON	Tuner, video input selector, RF converter, audio process IC

Table 1-1 Power Supply

2. SYSTEM CONTROL

2-1 General

The system control circuit inputs the commands given by the operator and sets the mechanism and circuits to the commanded mode. The circuit also inputs the detection outputs from the tape/mechanism protection sensors and protects the VTR and tape against abnormal operations. Fig. 2-1 is a simplified system control diagram. System control is performed by 3 microprocessors (system control μP: S-μP, timer μP: T-μP, tuning μP: TU-μP). S-μP communicates commands given by the operator and information of VTR operation modes, etc. with T-μP, and T-μP communicates with TU-μP. The μP controls the following according to this information.

S-μP:
1. Sets the mechanism, servo, audio/video processing and power supply circuits to the commanded mode according to two types of switch operation data (1: Function switches input by T-μP, 2: Remote function switches input by TU-μP) and timer outputs.
2. Sets the VTR to the stop mode according to the detection outputs of trouble sensors in the mechanism and servo circuit and protects the VTR and tape against abnormal operation.
3. Transmits the VTR operation mode data to T-μP to drive the indicators (STOP and PAUSE etc.) and digital multidisplay and informs the operator of the VTR operation state.

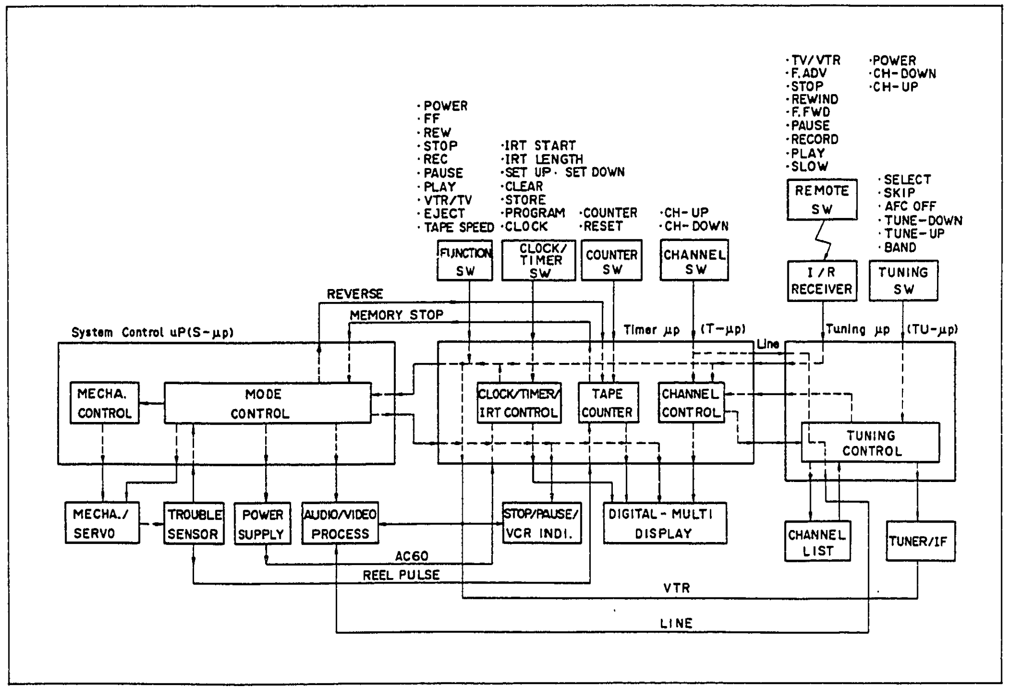

·POWER
·FF
·REW
·STOP
·REC
·PAUSE
·PLAY
·VTR/TV
·EJECT
·TAPE SPEED
·IRT START
·IRT LENGTH
·SET UP· SET DOWN
·CLEAR
·STORE
·PROGRAM
·CLOCK
·COUNTER
·RESET
·CH-UP
·CH-DOWN
·TV/VTR
·F.ADV
·STOP
·REWIND
·F.FWD
·PAUSE
·RECORD
·PLAY
·SLOW
·POWER
·CH-DOWN
·CH-UP
·SELECT
·SKIP
·AFC OFF
·TUNE-DOWN
·TUNE-UP
·BAND
FUNCTION SW
CLOCK/TIMER SW
COUNTER SW
CHANNEL SW
REMOTE SW
I/R RECEIVER
TUNING SW
REVERSE
MEMORY STOP
System Control uP(S-μp)
Timer μp (T-μp)
Line
Tuning μp (TU-μp)
MECHA. CONTROL
MODE CONTROL
CLOCK/TIMER/IRT CONTROL
TAPE COUNTER
CHANNEL CONTROL
TUNING CONTROL
MECHA./SERVO
TROUBLE SENSOR
POWER SUPPLY
AUDIO/VIDEO PROCESS
STOP/PAUSE/VCR INDI.
DIGITAL-MULTI DISPLAY
CHANNEL LIST
TUNER/IF
AC60
REEL PULSE
VTR
LINE

Fig. 2-1 System Control Block Diagram

4. Transmits the tape running direction data to the counter in T-μP to determine the counter mode.
5. Receives the memory stop data from T-μP and sets the VTR to the stop mode.

The data required in 1 - 3 above is transmitted and received via communications lines between the μPs.

T-μP:
1. Receives the function switch operation data and transmits the data to S-μP via the communications lines; S-μP determines the VTR operation mode according to the data.
2. Receives the clock/timer switch operation data and supplies it to the internal power frequency counter for the clock/timer/IRT. Using the data, the counter determines display switching, the present time, timer ON/OFF times and IRT ON/OFF times.
3. Receives the counter switch operation data and supplies it to the internal tape counter to switch the display between clock and counter and to reset the counter.
4. Receives the channel switch operation data and supplies it to TU-μP via the communications lines. TU-μP reads the tuning data of the channel commanded by T-μP from the channel list and converts it to a control voltage, then applies it to the tuner/IF circuit to select a channel. TU-μP also supplies the channel information to the internal channel controller in T-μP to change the channel indication on the digital multidisplay.
5. Receives the VTR operation mode from S-μP via the communications lines to drive the stop/pause/etc. indicators and informs the operator of the VTR operation state.
6. Receives the AUX select signal data during operating the channel up/down switch and controls the internal line/tuner switching memory output. This output is transmitted to TU-μP via the communications lines and is output from TU-μP to become the input select control signal for the audio/video processing circuit.
7. Inverts the internal VTR/TV switching memory output to ON/OFF alternately every time T-μP receives VTR/TV switch operation data. This output becomes the ON/OFF control signal for the RF converter circuit and the TV/VTR select control signal of the VHF output.
8. Detects the power frequency and a power failure data using the power frequency detection system. T-μP switches off the indicators and the indication in the digital multidisplay during a power failure to save power consumption of the μP and backs up the RAM storing the program data, tape counter data and channel data using a large capacitance capacitor for approx. 1 second, and at the same time, it increments the time using the built-in reference clock signal.

TU-μP:
1. Receives the IR remote function switch operation data and transmits it to S-μP via the communications lines, passing through T-μP. However, the remote channel up/down operation data, direct channel operation data and TV/VTR operation data are used in the μP. Receiving the data, S-μP determines the VTR operation mode and T-μP determines the channel.
2. Receives the line/tuner select data from the T-μP via the communications lines and outputs it to control the line/tuner input selection in the audio/video processing circuit.

2-2 Communications between μPs

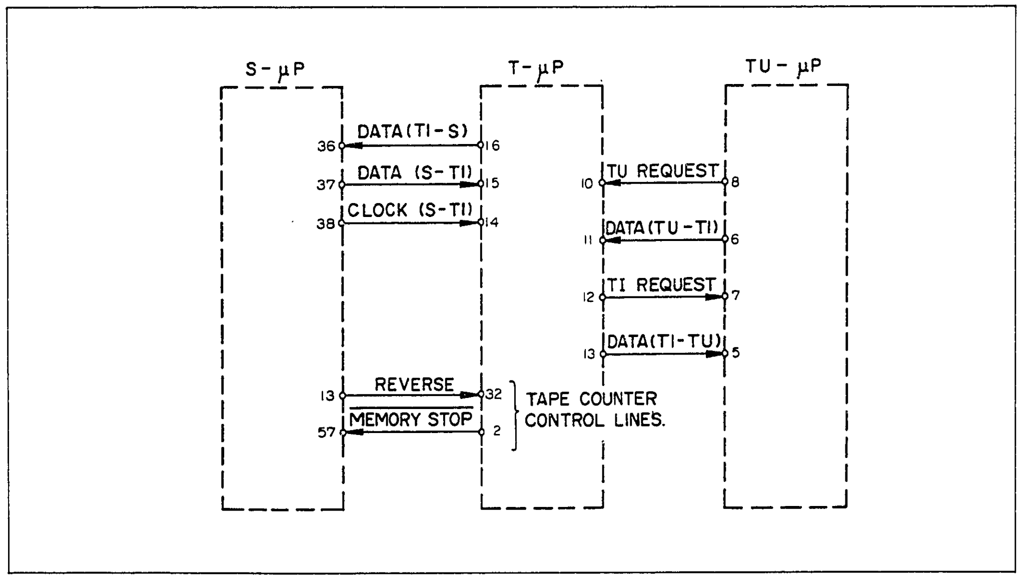


Fig. 2-2 Communications between μPs

As described previously, to fulfil the functions of the μPs, one μP needs the data in other μPs, so the μPs must always communicate with each other.

Fig. 2-2 shows the communications lines between the μPs. Communications between S-μP and T-μP are performed with a period of approx. 35ms. This is because T-μP must always know the operation data of S-μP which determines the VTR operation mode to inform the operator of the VTR's mode using LEDs and the digital multidisplay and also T-μP must transmit the operator's switch operation data detected by T-μP or TU-μP without a time lag.

S-µP and T-µP are connected via 3 communications lines (CLOCK (S-TI), DATA (S-TI), DATA (TI-S)) and 2 tape counter control lines (COUNT REV., $\overline{\text{MEMORY STOP}}$). The CLOCK (S-TI) signal is output from S-µP and synchronizes the data transfer between S-µP and T-µP. DATA (S-TI) and DATA (TI-S) are data buses; 8-bit serial data is transferred from S-µP to T-µP using DATA (S-TI) line and vice versa using DATA (TI-S) line. To match the phases of 8-bit serial data output from T-µP and S-µP, a header pulse is output when S-µP starts transmitting the 8-bit serial data (before the D0 bit is output). T-µP detects this header pulse at the rise of CLOCK (S-TI) signal. The phase of 8-bit serial data to be output by T-µP is matched with the phase of the header pulse. Fig. 2-3 shows the timing of these phases and Table 2-1 shows the 8-bit serial data output from S-µP and T-µP.

The tape counter control lines are provided to cancel the time lag between the tape counter in T-µP and S-µP. If S-µP and T-µP communicate the tape counter up/down count switching command and memory stop command, given to S-µP, via the communications lines, a time lag occurs causing counting errors and the tape stop position to drift when the memory stop function is used. Therefore, data must be communicated directly between S-µP and tape counter. The tape counter control lines consist of the "REVERSE" signal which determines the tape counter up/down count mode and the "MEMORY STOP" signal which gives the memory stop command to S-µP.

Data is communicated between T-µP and TU-µP when the remote function switch or channel switch is pressed by the operator and the channel is changed. T-µP and TU-µP are connected via 4 communications lines (DATA (TU-TI), DATA (TI-TU), TU REQUEST, TI REQUEST. DATA (TU-TI) and DATA (TI-TU) are 8-bit serial data communications lines. Data is transferred from TU-µP to T-µP via DATA (TU-TI) line and from T-µP to TU-µP via DATA (TI-TU) line, acknowledging the reception µP each bit. TI REQUEST and TU REQUEST are the data transfer control signals output to TU-µP from T-µP and to T-µP from TU-µP respectively.

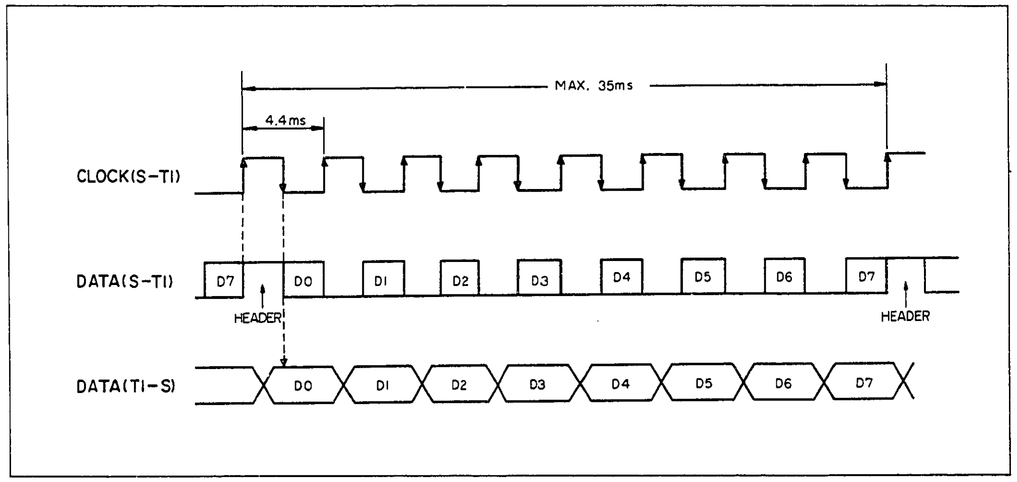
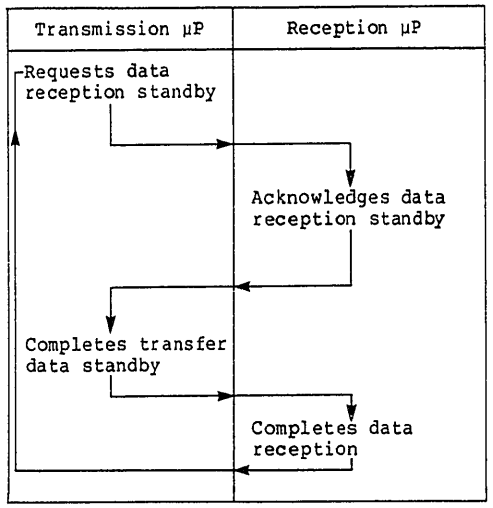

MAX. 35ms
4.4ms
CLOCK(S-TI)
DATA(S-TI)
D7
D0
D1
D2
D3
D4
D5
D6
D7
HEADER
HEADER
DATA(TI-S)
D0
D1
D2
D3
D4
D5
D6
D7

Fig. 2-3 Timing of Communications between S-µP and T-µP

The transmission and reception µPs play the following roles.


Transmission µP
Reception µP
Requests data reception standby
Acknowledges data reception standby
Completes transfer data standby
Completes data reception

As described above, the transmission µP requests the reception µP to acknowledge and obtains acknowledgement from the reception µP. The transmission µP repeats this procedure twice for every bit. If the transmission µP cannot obtain acknowledgement from the reception µP within approx. 100 ms after it requests the reception µP to acknowledge, the transmission µP stops transmitting data and returns to the main loop.

Fig. 2-4 is a timing chart of data transfer between T-µP and TU-µP. Table 2-2 shows the 8-bit serial codes on the DATA (TI-TU) line and Table 2-3 the 8-bit serial codes on the DATA (TU-TI) line.

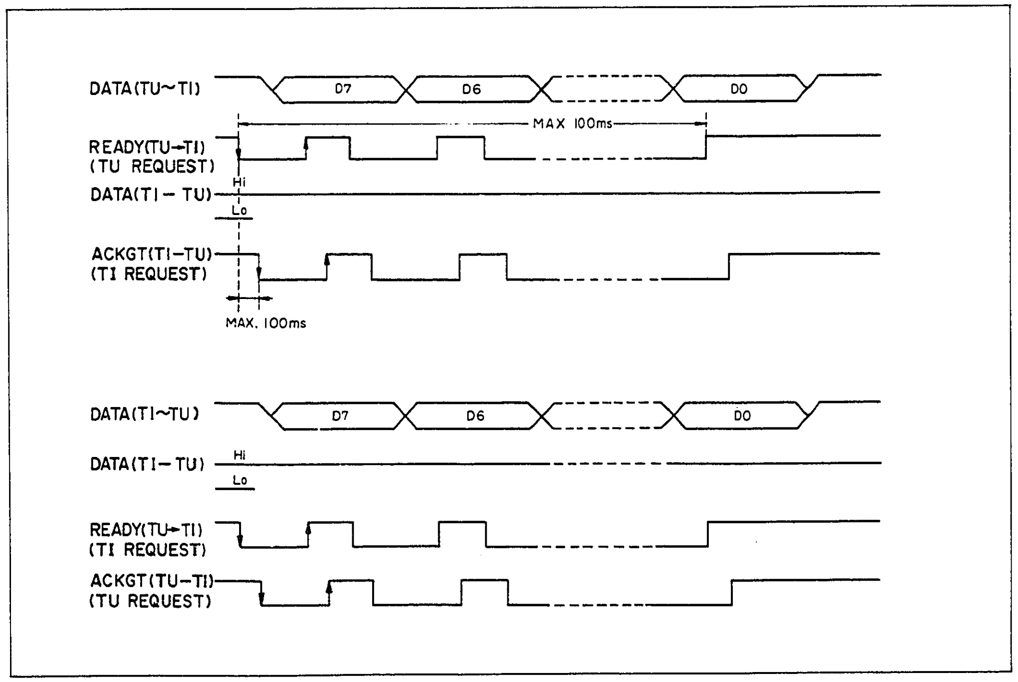

DATA(TU~TI)
D7
D6
D0
MAX 100ms
READY(TU→TI)
(TU REQUEST)
DATA(TI – TU)
Hi
Lo
ACKGT(TI–TU)
(TI REQUEST)
MAX. 100ms
DATA(TI~TU)
D7
D6
D0
DATA(TI–TU)
Hi
Lo
READY(TU←TI)
(TI REQUEST)
ACKGT(TU–TI)
(TU REQUEST)

Fig. 2-4 Timing of Communications between T-µP and TU-µP

Table 2-1 Data (S-T) & Data (T-S)

	D3-D0 D7-D4	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Data (TI-S)	0	DISCNECT	PLAY	REC	REVERSE	F.ADV	SLOW		FWD SEARCH	REV SEARCH	F.F	REW	STOP	A.DUB	V.DUB	PAUSE	EJECT
	1	PROG.S TGL	PWR TGL	PWR ON	PWR OFF	T.STBY	TIME ON	COUNTER /REMAIN		KEY OFF				SS UP	SS DWN		
	2	SP	LP	EP	SAP	NO SAP	NO SAP										
	3																
	4																
	5																
	6																
	7																
Data (S-TI)	0	POWER ON	PLAY	REC	A.DUB	F.ADV	SLOW	SEARCH	FWD SEARCH	REV	F.F	REW	STOP	REVERSE	V.DUB		SP NO TAB
	1	POWER OFF	STILL	REC PAUS	A.DUB PAUS	PWR OFF				REPEAT			STOP PAUS		V.DUB PAUS		LP PROG.S OFF
	2	POWER ON	PLAY	REC	A.DUB	F.ADV	SLOW		FWD SEARCH	REV SEARCH	F.F	REW	STOP	REVERSE	V.DUB		EP TAB
	3	POWER OFF	STILL	REC PAUS	A.DUB PAUS	PWR OFF				REPEAT			STOP PAUS		V.DUB PAUS		PROG.S OFF
	4	POWER ON	PLAY	REC	A.DUB	F.ADV	SLOW		FWD SEARCH	REV SEARCH	F.F	REW	STOP	REVERSE	V.DUB		DEW SP NO TAB
	5	POWER OFF	STILL	REC PAUS	A.DUB PAUS	PWR OFF				REPEAT			STOP PAUS		V.DUB PAUS		DEW LP PROG.S ON
	6	POWER ON	PLAY	REC	A.DUB	F.ADV	SLOW		FWD SEARCH	REV SEARCH	F.F	REW	STOP	REVERSE	V.DUB		DEW EP NO TAB
	7	POWER OFF	STILL	REC PAUS	A.DUB PAUS	PWR OFF				REPEAT			STOP PAUS		V.DUB PAUS		PROG.S ON

PROG.S : Program Search

Table 2-2 Data (TI-TU)

D3-D0 D7-D4	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	00 CH	01 CH	02 CH	03 CH	04 CH	05 CH	06 CH	07 CH	08 CH	09 CH						
1	10 CH	11 CH	12 CH	13 CH	14 CH	15 CH	16 CH	17 CH	18 CH	19 CH						
2	20 CH	21 CH	22 CH	23 CH	24 CH	25 CH	26 CH	27 CH	28 CH	29 CH						
3	30 CH	31 CH	32 CH	33 CH	34 CH	35 CH	36 CH	37 CH	38 CH	39 CH						
4	40 CH	41 CH	42 CH	43 CH	44 CH	45 CH	46 CH	47 CH	48 CH	49 CH						
5	50 CH	51 CH	52 CH	53 CH	54 CH	55 CH	56 CH	57 CH	58 CH	59 CH						
6	60 CH	61 CH	62 CH	63 CH	64 CH	65 CH	66 CH	67 CH	68 CH	69 CH						
7	70 CH	71 CH	72 CH	91 CH	92 CH	95 CH	96 CH	97 CH	98 CH	99 CH						
8																
9																
A	ST UP	ST DOWN									SC OFF	SC ON	TUNER LINE			
B																
C																
D			CH UP	CH DOWN		MUTE DISABL	MUTE ENABL	DISABLE	ENABLE							
E		KEY OFF														
F																

SC : Simulcast
ST : Slow Tracking

Table 2-3 Data (TU-T)

D3-D0 D7-D4	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	00 CH	01 CH	02 CH	03 CH	04 CH	05 CH	06 CH	07 CH	08 CH	09 CH				LOCK		
1	10 CH	11 CH	12 CH	13 CH	14 CH	15 CH	16 CH	17 CH	18 CH	19 CH			VHF(L)	VHF(H)	SUPER AFC OFF	UHF AFC ON
2	20 CH	21 CH	22 CH	23 CH	24 CH	25 CH	26 CH	27 CH	28 CH	29 CH						
3	30 CH	31 CH	32 CH	33 CH	34 CH	35 CH	36 CH	37 CH	38 CH	39 CH						
4	40 CH	41 CH	42 CH	43 CH	44 CH	45 CH	46 CH	47 CH	48 CH	49 CH						
5	50 CH	51 CH	52 CH	53 CH	54 CH	55 CH	56 CH	57 CH	58 CH	59 CH						
6	60 CH	61 CH	62 CH	63 CH	64 CH	65 CH	66 CH	67 CH	68 CH	69 CH						
7	70 CH	71 CH	72 CH	91 CH	92 CH	95 CH	96 CH	97 CH	98 CH	99 CH						
8																
9																
A																
B																
C				DISP	POWER OFF	POWER ON	DIGIT 9	DIGIT 8	DIGIT 7	DIGIT 6	DIGIT 5	DIGIT 4	DIGIT 3	DIGIT 2	DIGIT 1	DIGIT 0
D			CH UP	CH DOWN		POWER										F.ADV
E	STOP	KEY OFF	REWIND	F.FWD	R.SRCH	F.SRCH	STILL/ PAUSE		RECORD	CNT/ RMN	PLAY		AUDIO A/B	M.STOP SW		SLOW
F	R.SRCH	F.SRCH			ST UP	ST DOWN		PROG.		CLEAR	TV/VTR	PROG-S SW	V.DUB	A.DUB	SS UP	SS DOWN

SS : Slow Speed

2-3 Key Input

The key input circuit is an interface between the operator and each μP. The operator's commands are detected by the key matrix and IR receiver circuits and are supplied to the μPs to control the mechanism and circuits.

2-3-1 Key matrix circuit

Fig. 2-5 is a simplified diagram of the key matrix circuit of the switches on the front panel of the VTR. These switches, other than NORM/SELECT mode selector (S790), are of the push type and are input to T-μP and TU-μP via a matrix system.

T-μP uses 8 of the grid drive signals and one (Sh) of the segment drive signals which drive the digital multidisplay as key scan signals. There are 4 (MATRIX 0 -MATRIX 3) feedback input ports of the key scan signals. The matrix switch circuit detects 22 switch operations. The detected switch operation data is transmitted to S-μP and TU-μP via the circuits in T-μP and communications buses to trigger the functions of each μP. TU-μP has 2 outputs ($\overline{\text{PHASE 0}}$, $\overline{\text{PHASE 1}}$) and 3 feedback input ports (MATRIX 0 - MATRIX 2) of the scan signals required by the matrix switch circuit. This matrix circuit detects 6 switch operations.

The detected switch operation data is transmitted to the tuning controller in the TU-μP to set the tuning data.

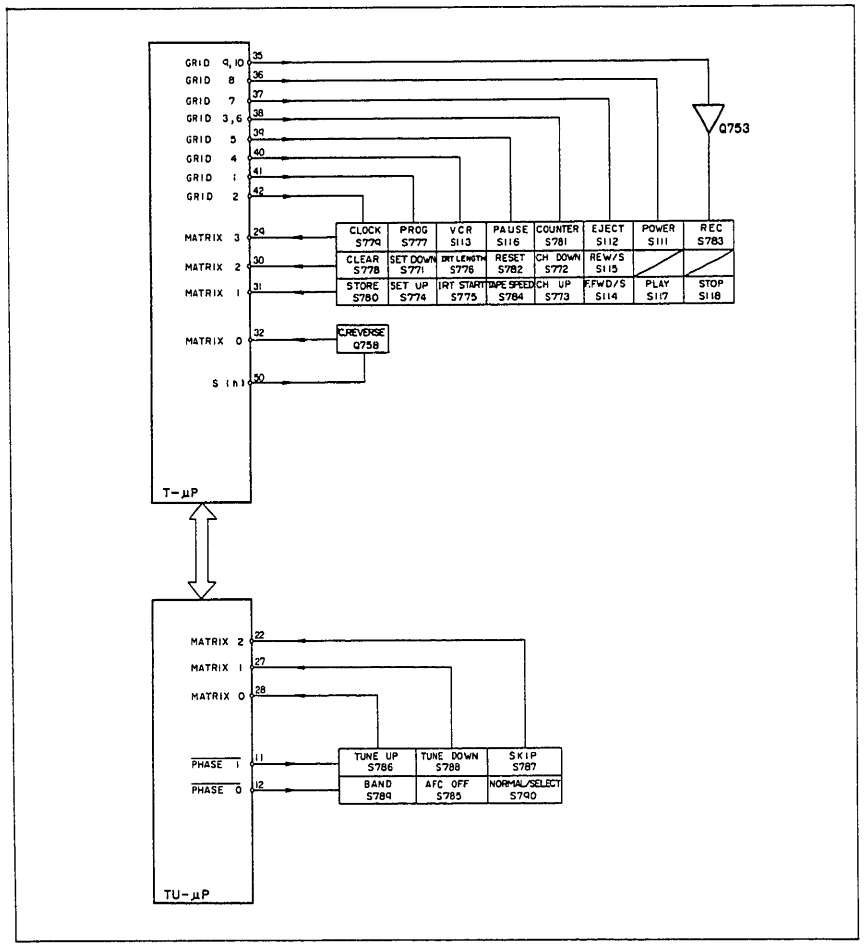

GRID 9,10
GRID 8
GRID 7
GRID 3,6
GRID 5
GRID 4
GRID 1
GRID 2
MATRIX 3
MATRIX 2
MATRIX 1
MATRIX 0
S (h)
Q753
CLOCK S779
PROG S777
VCR S113
PAUSE S116
COUNTER S781
EJECT S112
POWER S111
REC S783
CLEAR S778
SET DOWN S771
IRT LENGTH S776
RESET S782
CH DOWN S772
REW/S S115
STORE S780
SET UP S774
IRT START S775
TAPE SPEED S784
CH UP S773
F.FWD/S S114
PLAY S117
STOP S118
C.REVERSE Q758
T-µP
TU-µP
TUNE UP S786
TUNE DOWN S788
SKIP S787
BAND S789
AFC OFF S785
NORMAL/SELECT S790
PHASE 1
PHASE 0

Fig. 2-5 Simplified Key Matrix Circuit Diagram

2-3-2 IR remote control system

The IR receiver circuit can receive the IR signals transmitted by the exclusive remote controller.

The exclusive remote controller has 9 switches (PLAY, RECORD, PAUSE, F. FWD, REWIND, STOP, POWER, CH-UP, CH-DOWN).

Fig. 2-6(a) is a simplified circuit diagram of the exclusive IR remote controller circuit.

The µP in the remote controller detects switch operations via a matrix system and encodes the input into to the IR code,

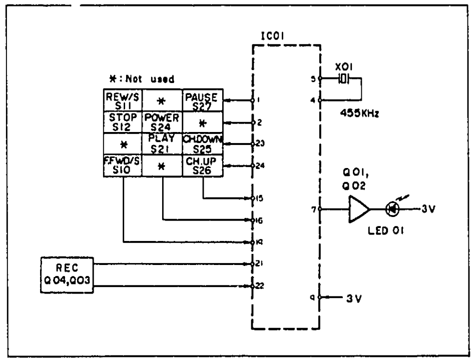

IC01
*: Not used
REW/S S11
PAUSE S27
STOP S12
POWER S24
PLAY S21
CH.DOWN S25
F.FWD/S S10
CH.UP S26
X01
455KHz
Q01, Q02
LED 01
-3V
REC Q04,Q03

Fig. 2-6(a) Simplified IR Remote Controller Circuit Diagram

then pulse-pitch-modulates the code to generate a PPM signal. The µP modulates the 38kHz carrier signal using this PPM signal and outputs it to pulse-drive the LEDs.

Fig. 2-6(b) is a simplified diagram of the IR receiver circuit. This circuit consists of photodiode (PD1), IR AGC/detector/shaper IC (IR751), amplifier (Q756, Q757) and TU-µP.

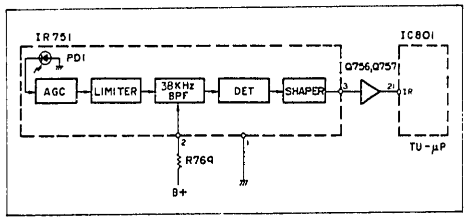

IR751
PD1
AGC
LIMITER
38KHz BPF
DET
SHAPER
Q756,Q757
IC801
TU-µP
R769
B+

Fig. 2-6(b) Simplified IR Receiver Circuit Diagram

PD1: Receives the 38kHz IR signal transmitted from the IR remote controller via the infrared filter on the front of the VTR. The output voltage according to the strength of infrared signal is generated at the cathode of PD1.

IR751:

Consists of the AGC, limiter, 38kHz bandpass filter (BPF), detector and shaper.

AGC: Generates an error signal according to the strength of infrared signal to control the amplification and produces an IR signal of the constant output.

LIMITER:

Sets the amplitude of IR signal constant.

38kHz BPF:

Suppresses unnecessary signal components in the 38kHz IR signal. The center frequency of the BPF is determined by the resistance between pin 2 and B+.

DETECTOR:

Removes the 38kHz carrier components from the IR signal using an AM detection system to detect the PPM signal.

SHAPER:

Forms the wave of PPM signal to obtain a pulse with a steep ramp.

Q756/Q757:

Amplifies the PPM signal shaped and output from IR751 to an optimum input level for TU-µP.

TU-µP:

Decodes the PPM signal and transmits it to T-µP via the communications bus.

2-4 Mechanism/Circuit Control

When the µPs input operator's command via the key input circuit, the mechanism and circuits are set to the commanded mode. This operation is controlled by the mechanism/servo section and audio/video processing section.

2-4-1 Mechanism/servo control

General

Fig. 2-8 is a simplified diagram of the mechanism/servo control. S-µP mainly controls the whole mechanism and circuits and T-µP is concerned with partial control.

1. Cassette loading motor control:
   Controls loading and ejection of a cassette.
2. Tape loading motor control:
   Determines the mechanism operation modes - tape loading/unloading,

action/release of various brakes, backtension, take-up mechanism, etc.

3. Tape protection sensor monitoring:
   Detects abnormal operations in tape running using the dew, tape end and reel sensors.
4. Capstan motor control:
   Determines the tape speed and running direction, and fast forwards and rewinds the tape and takes up slack tape, etc.
5. Tape counter control:
   Makes T-μP count the pulses output by the HALL IC and calculates the amount of tape taken up to show it in the digital multidisplay. When the indication reaches "9999" in the fast forward and rewind modes, T-μP gives the stop command to S-μP.
6. Servo control:
   Determines the operation mode of the servo circuit. The servo circuit receives the feedback signals from the FG (Frequency Generator) and TACH pulse output from the cylinder and capstan motors and maintains the specified relationships between the speeds and phases (positions) of both motors.
7. Record safety tab detection:
   Detects the safety tab on the rear of a cassette to prevent the prerecorded programs from being erased by a mistake.

The above are the outline of mechanism/servo control. Next, the mechanism/servo control is described in details.

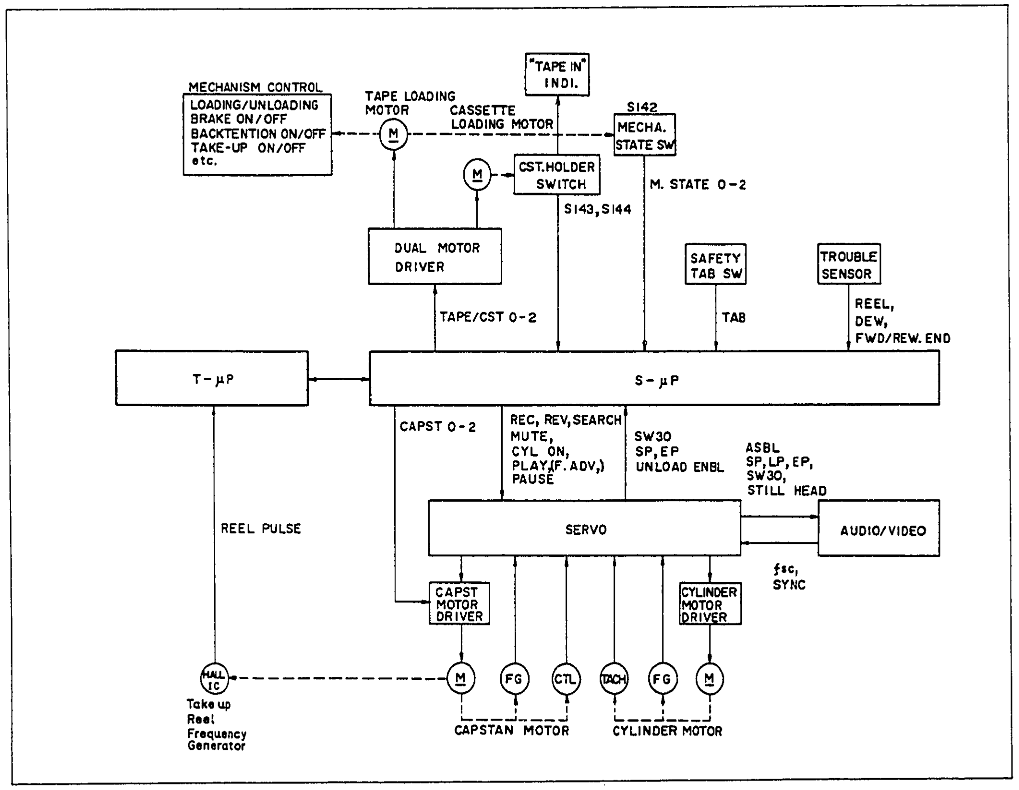

MECHANISM CONTROL
LOADING/UNLOADING
BRAKE ON/OFF
BACKTENTION ON/OFF
TAKE-UP ON/OFF
etc.
TAPE LOADING MOTOR
CASSETTE LOADING MOTOR
M
"TAPE IN" INDI.
S142
MECHA. STATE SW
CST.HOLDER SWITCH
S143,S144
M. STATE 0-2
DUAL MOTOR DRIVER
SAFETY TAB SW
TROUBLE SENSOR
TAPE/CST 0-2
TAB
REEL, DEW, FWD/REW. END
T-μP
S-μP
CAPST 0-2
REC, REV,SEARCH
MUTE,
CYL ON,
PLAY(F.ADV,)
PAUSE
SW30
SP,EP
UNLOAD ENBL
ASBL
SP,LP,EP,
SW30,
STILL HEAD
REEL PULSE
SERVO
AUDIO/VIDEO
fsc, SYNC
CAPST MOTOR DRIVER
CYLINDER MOTOR DRIVER
HALL IC
FG
CTL
TACH
Take up Reel Frequency Generator
CAPSTAN MOTOR
CYLINDER MOTOR

Fig. 2-8 Mechanism/Servo Control

Casstte/tape loading motor control

Fig. 2-9 is a simplified diagram of the cassette/tape loading motor control circuit. S-μP controls the rotation directions of both the cassette and tape loading motors using dual motor driver IC902 via 3 output lines. The rotation speeds are fixed and determined by the voltage (12V) applied to pin 9 of IC902. The driving periods of both motors are determined by the state sensor fed back from the respective objects of control. The driving period of the cassette loading motor is determined by two casstte holder state sensors S143/S144. The S143/S144 outputs also drive the "CASSETTE IN" indicator via cassette-in detector consisting of D910, D917. The driving period of the tape loading motor is determined by mechanism state sensor, S142.

Tape/mechanism protection

The cassette and tape loading motor control systems have protection devices which protect the tape, cassette, mechanism and motors when any abnormalities occur in the mechanism during loading or unloading. If the motor controller in S-μP cannot obtain the required state data from the controlled object when the loading or unloading operation period continues for more than 5 seconds for the cassette loading motor control system and more than 7 seconds for the tape loading motor control system, the controller reverses the motor rotation and returns it to the start position. If any abnormality occurs and it does not return to the start position, the controller shuts off the VTR power.

The protection device in the tape loading

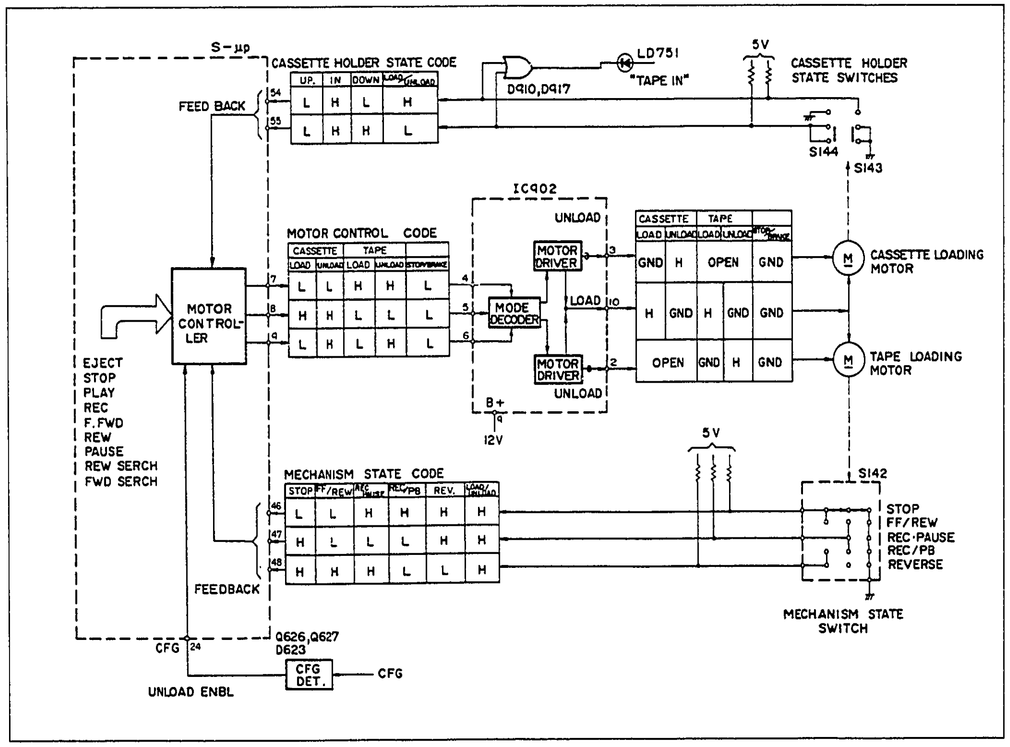
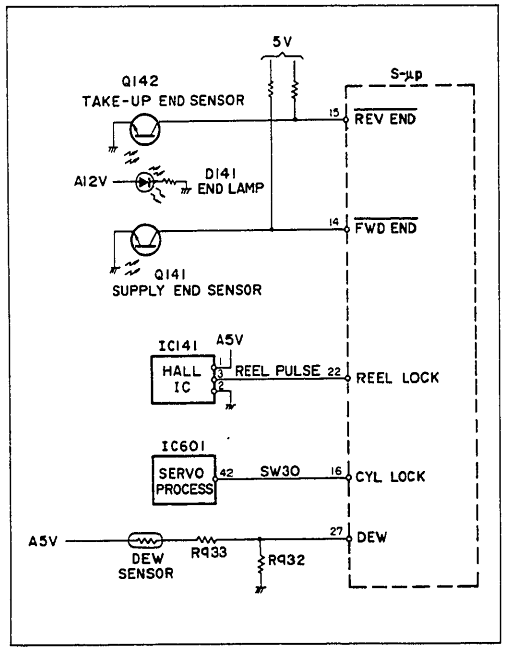

S-μp
CASSETTE HOLDER STATE CODE
UP. | IN | DOWN | LOAD/UNLOAD
54: L | H | L | H
55: L | H | H | L
FEED BACK
D910,D917
LD751
"TAPE IN"
5V
CASSETTE HOLDER STATE SWITCHES
S144
S143
IC902
UNLOAD
MOTOR CONTROL CODE
CASSETTE LOAD | CASSETTE UNLOAD | TAPE LOAD | TAPE UNLOAD | STOP/BRAKE
7: L | L | H | H | L
8: H | H | L | L | L
9: L | H | L | H | L
MOTOR CONTROLLER
MOTOR DRIVER
MODE DECODER
LOAD
B+
12V
CASSETTE LOAD | CASSETTE UNLOAD | TAPE LOAD | TAPE UNLOAD | STOP/BRAKE
3: GND | H | OPEN | GND
10: H | GND | H | GND | GND
2: OPEN | GND | H | GND
CASSETTE LOADING MOTOR
TAPE LOADING MOTOR
EJECT
STOP
PLAY
REC
F.FWD
REW
PAUSE
REW SERCH
FWD SERCH
MECHANISM STATE CODE
STOP | FF/REW | REC PAUSE | REC/PB | REV. | LOAD/UNLOAD
46: L | L | H | H | H | H
47: H | L | L | L | H | H
48: H | H | H | L | L | H
FEEDBACK
5V
S142
STOP
FF/REW
REC·PAUSE
REC/PB
REVERSE
MECHANISM STATE SWITCH
CFG
24
Q626,Q627
D623
CFG DET.
UNLOAD ENBL

Fig. 2-9 Simplified Tape/Cassette Motor Control Diagram

motor control system also monitors whether slack tape is taken up normally by the supply reel during unloading. If unloading stopped with this tape take-up incomplete and the eject operation was done, the tape would be damaged. To prevent this, as soon as unloading starts, the rectified and inverted CFG signal (called "$\overline{\text{UNLOAD ENABLE}}$") is supplied through pin 24 of IC901 to the motor controller in S-µP from the servo circuit to monitor whether the capstan motor, the motive power to take up slack tape, rotates normally. When the CFG signal goes "Hi" during unloading, the unloading operation stops and the VTR enters the power off mode immediately.

Tape protection sensors

Fig. 2-11 is simplified diagram of the tape protection sensor circuit. This unit has 5 tape protection sensors - end sensors, reel lock sensor, cylinder lock sensor and dew sensor.

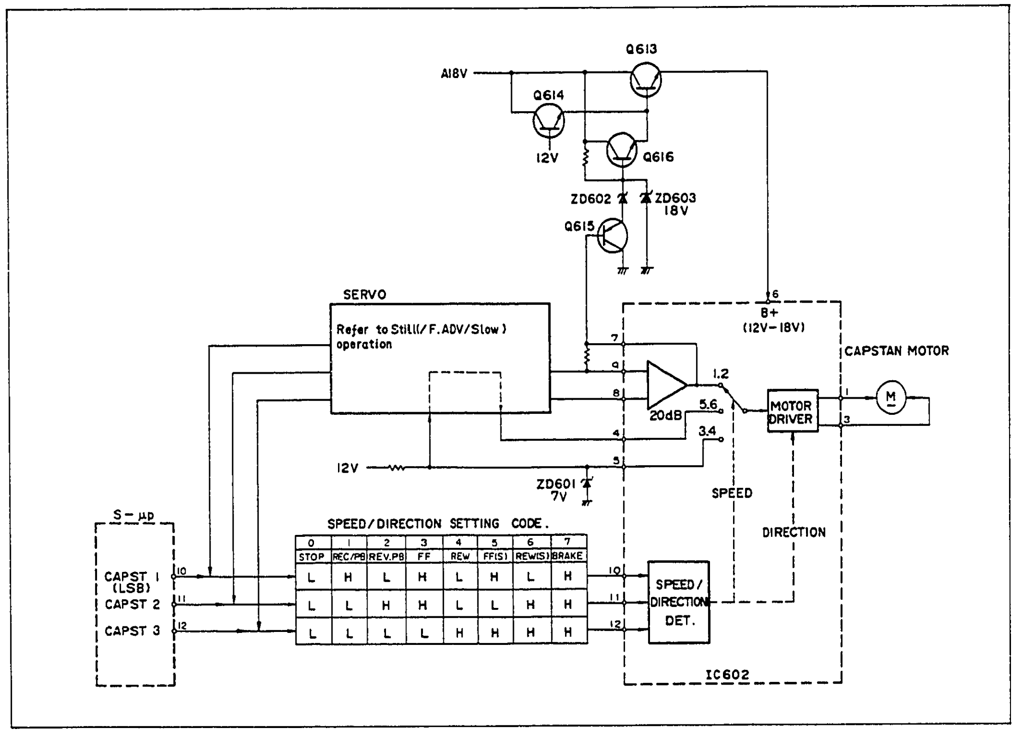


5V
S-µp
Q142
TAKE-UP END SENSOR
15
REV END
A12V
D141
END LAMP
14
FWD END
Q141
SUPPLY END SENSOR
IC141
A5V
HALL IC
3
2
REEL PULSE
22
REEL LOCK
IC601
SERVO PROCESS
42
SW30
16
CYL LOCK
A5V
DEW SENSOR
R933
R932
27
DEW

Fig. 2-11 Simplified Tape Protection Sensor Circuit Diagram

- End sensor:
  The take-up end sensor Q142 (supply end sensor Q141) receives light emitted by the end lamp through the tape leader at the reverse (forward) tape end and detects the tape end. When the forward end sensor receives light at the tape end in modes other than timer and IRT recording, it sets the VTR to the rewind mode automatically. When the rewind tape end sensor receives light, it sets the VTR to the stop mode automatically.
- Reel lock sensor:
  Detects the tape take-up condition and sets the VTR to the stop mode if any abnormalities occur. The rotation speed of the take-up reel disk is detected by the HALL IC, IC141, and the period of the HALL IC signal is calculated and the reel sensor detects any abnormality in the tape take-up operation.
  If the frequency is less than the values below in each mode, the tape take-up is abnormal.
    REC/PB/SEARCH: 6 sec.
    REW/F.FWD : 3 sec.
  However, this frequency detection is not performed in the pause mode.
- Cylinder lock sensor:
  Detects faulty tape winding onto the cylinder and abnormal rotation of the cylinder motor due to a motor fault and sets the VTR to the stop mode. Faulty rotation of the cylinder is detected by calculating the frequency of the head switching (SW30) signal. If the frequency is less than approx. 10Hz, it is judged that the cylinder speed is faulty.
- Dew sensor:
  Detects condensation in the VTR (especially on the cylinder) during Power ON and flashes the stop indicator while dew is present to warn the operator; at the same time, it inhibits any function switch inputs. Condensation is detected when the dew sensor, the resistance of which changes low when condensation occurs, increases the voltage drop across resistor R932.

Capstan motor control



A18V
Q613
Q614
12V
Q616
ZD602
ZD603
18V
Q615
SERVO
Refer to Still(/F.ADV/Slow) operation
6
B+
(12V-18V)
CAPSTAN MOTOR
7
9
8
4
5
20dB
1.2
5.6
3.4
MOTOR DRIVER
M
1
3
12V
ZD601
7V
SPEED
DIRECTION
S-µp
CAPST 1 (LSB)
CAPST 2
CAPST 3
10
11
12
SPEED/ DIRECTION DET.
IC602

SPEED/DIRECTION SETTING CODE.

0	1	2	3	4	5	6	7
STOP	REC/PB	REV.PB	FF	REW	FF(S)	REW(S)	BRAKE
L	H	L	H	L	H	L	H
L	L	H	H	L	L	H	H
L	L	L	L	H	H	H	H

Fig. 2-12 Simplified Capstan Motor Control Circuit Diagram

The capstan motor keeps the tape speed constant in the record and playback modes and takes up the tape onto the take-up or supply reel in the fast forward, rewind, (frame advance) and unloading modes. Fig. 2-12 is a simplified diagram of the capstan motor control circuit. To perform the above controls, S-µP determines the motor speed and rotation direction using capstan motor driver IC602. The power supply voltage applied to IC602 pin 6 is adjusted to an optimum value from a minimum of 12V to a maximum of 18V due to its load by the variable power supply circuit consisting of Q613 - Q616, ZD602 and ZD603 to reduce motor's power consumption. The variable power supply circuit output is derived from the emitter of Q613. Two output voltage limiting voltages and a variable voltage are applied to Q613's base to control the output voltage of the variable power supply circuit. One limiting voltage maintains the output voltage at more than 12V using Q614. The other limiting voltage maintains the output voltage at less than 18V using ZD603. The latter limiting voltage is produced by adding the terminal voltage (17V) of ZD602 to the voltage obtained by amplifying the capstan drive voltage in the servo system by approx. 20 dB through Q615. Since this voltage is controlled so it is proportional to the load, the output voltage follows it.

S-µP transmits 3-bit capstan speed/direction setting codes to IC602. (However, the control codes are supplied from the servo circuit in the frame advance mode.) IC602 decodes them to determine the motor's speed and rotation direction. The motor speed is determined by the voltages applied to the 3 speed setting inputs of IC602 as shown in the table below.

Speed setting pins of IC602	Voltage	Selected codes
8 and 9	0 - 5V (Variable)	1 (001) or *1 2 (010)
4	9V: Speed up (9V: SP 6V: $\overline{\text{SP}}$) 5V: Speed down (5V: SP 4V: $\overline{\text{SP}}$ 4V: Normal	5 (101) or 6 (110) *2
5	7V	3 (011) or 4 (100)

*1: The capstan drive voltage from the servo circuit is applied and is amplified in the IC by 20 dB, then it is supplied to the motor driver in IC602.

*2: The supply voltage and mode are determined by the servo circuit. Normally, 4V is applied. In the frame advance or slow motion mode, the speed up voltage (9-6V) or speed down voltage (5-4V) is selected and applied to pin 4. In this mode, the servo circuit sets IC602 to the "FF(S)" or "REW(S)" mode and makes IC602 select the voltage applied to pin 4. (See the servo circuit for details.)

The rotation direction is determined by selecting the output ports of the motor driver in IC602 according to the capstan speed/direction setting codes. When the LSB of the capstan speed/direction setting codes is "Lo" (excluding the stop mode), the reverse mode is selected and the motor drive current flows from pin 3 to pin 1. When the LSB is "Hi" (excluding when braked), the forward mode is selected and the motor drive current flows from pin 1 to pin 3. The 2 output ports are set open in the stop mode, and when braking is applied, the output ports are short-circuited.

Tape counter control

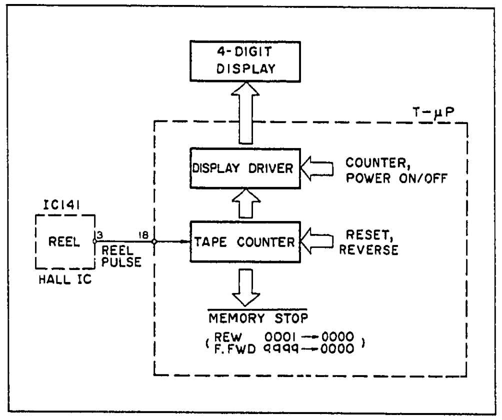


Fig. 2-13 Simplified Tape Counter Circuit Diagram

Fig. 2-13 is a simplified diagram of the tape counter control circuit. The tape counter in T-µP counts the reel pulses generated by the take-up reel disk rotation and indicates them in the digital multidisplay by 4 digits. The reel pulse is derived from HALL IC (IC141). The HALL IC detects the change in magnetic flux caused by the rotation of the magnet magnetized in 8 poles on the take-up reel disk and generates 4 cycles of square wave when the disk rotates by one turn. T-µP determines the counter mode so the counter counts up when the "REVERSE" signal described in "Communications between µPs" is "Lo" and the counter counts down when the signal is "Hi", and counts the reel pulses. The count data is transmitted to the display driver. When the counter display mode is commanded by the operator, the 4-digit clock/counter display in the digital multidisplay is switched to the counter display mode from the clock display mode and the count data is displayed. When the power is turned off from on in the counter display mode, the display is automatically switched to the clock. When the power is turned on again, the counter display is restored. When the reset is commanded by the operator, the counter is reset to 0. The tape counter has a memory stop function. When the digital multidisplay is in the counter display mode and the counter reaches "9999" during rewind or "0000" during fast forward, the memory stop signal (Pulse width: 400ms) is generated and supplied to S-µP via the "MEMORY STOP" line described in "Communications between µPs". When S-µP receives the "MEMORY STOP" signal in the fast forward or rewind mode, it sets the VTR to the stop mode.

Servo Circuit Control

Fig. 2-14 shows the control lines between the servo circuit and S-µP and between the servo circuit and audio/video processing circuit. S-µP and the servo circuit are connected via 10 outputs REC, PLAY, SEARCH, (F. ADV), PAUSE, REVERSE, MUTE, $\overline{\text{CYL ON}}$, $\overline{\text{SP SW}}$, $\overline{\text{EP SW}}$ and 4 inputs SP, EP, CYL LOCK, UNLOAD ENBL (CFG).

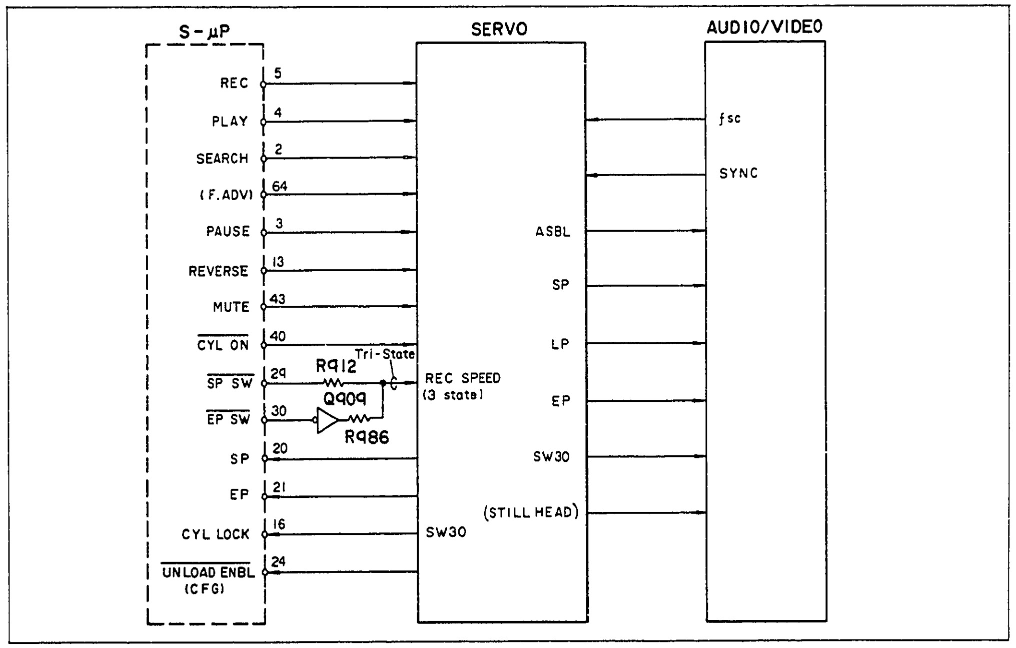


Fig. 2-14 Servo Circuit Control

- The outputs - "REC, PLAY, SEARCH, (F.ADV), PAUSE, REVERSE" - determine the operation mode of the servo circuit.
- The output, "MUTE", determines the control pulse recording inhibit period during loading and recording pause.
- The output, "$\overline{\text{CYL ON}}$", operates the cylinder servo.
- The outputs, "$\overline{\text{SP SW}}$" and "$\overline{\text{EP SW}}$", determine the recording tape speed. Using both outputs, the tristate voltage (SP: 0V, LP: 2.5V, EP: 3.8V) is produced and supplied to the servo circuit.
- The inputs, "SP" and "EP", receive the tape speed data necessary for the tape speed to be indicated in the digital multidisplay.
- Inputs, "CYL LOCK" and "UNLOAD $\overline{\text{ENBL}}$"(CFG), are trouble sensors described in "Tape protection sensor".

The servo circuit and audio/video processing circuit are connected via 6 outputs (ASBL, SP, LP, EP, SW30, STILL HEAD) and 2 inputs (fsc, SYNC).

- The output, "ASBL", inhibits recording of audio/video signals for approx. 0.7 seconds just after recording pause is released to optimize tracking.
- The outputs, "SP, LP, EP", determine the emphasis/deemphasis of the audio/video signals during recording and play.
- The output, "SW30", switches the playback outputs of 2 video heads to a continuous signal, changes the phase shifting direction of the chroma signal for every channel and shifts the carrier frequency used for the luminance signal modulation by fH/2 for every channel.
- The output, "STILL HEAD", selects the video head exclusive for still play in the still mode.
- The input, "fsc", produces the clock signal necessary in the digital servo system.
- The input, "SYNC", synchronizes the cylinder servo during recording with the vertical sync signal in the incoming video signal.

The servo circuit operation will be described later in detail.

2-5 Digital Multidisplay/Mode Indicator Control

The VTR uses LEDs and a digital multidisplay to inform the operator whether the VTR is operated as commanded by the operator and warn the operator of the abnormal operations of the VTR. The LEDs and digital multidisplay are driven by T-µP.

Fig. 2-15 shows the connections between T-µP and the LEDs and digital multidisplay. The LEDs are directly driven by T-µP and display 7 operation modes (STOP/DEW WARNING, PAUSE, VTR, PLAY, REC, F.FWD and REW). All the indicators except "VTR" are controlled by the operation mode data supplied from S-µP and the "VTR" indicator is controlled by the TV/VTR memory output of T-µP.

The digital multidisplay is driven by the dynamic drive system and indicates the following 8 items.

1. Input signal (AUX)
2. Channel
3. Tape speed
4. Tape counter
5. Clock
6. Program
7. IRT start/length/remaining time

Concerning items 1 - 3 above, exclusive segments are provided in the digital multidisplay. For the remaining items 4 - 7, one item is selected by the operator and is displayed. Fig. 2-16 shows the locations of the grids and segments in the digital multidisplay. Table 2-5 shows the relation of grids and segments with respect to the displayed contents. T-µP receives the display data and display select data from the internal circuits and S-µP to control the display. When a power failure occurs (detected by the power failure signal), all displays go off to reduce the backup power consumption. When the power is turned off, only the clock is displayed.

When the power is turned on, only the operation mode which was selected by the operator is displayed. To drive the digital multidisplay dynamically, T-µP outputs 8-phase grid drive pulses (GRID 1 - GRID 10) with 60Hz and duty cycle 9% and 9 segment drive pulses (Sa - Si). To prevent flickering caused by the difference between the power frequency of the heater in the display and the grid lighting frequency, the frequency of grid drive pulses is synchronized with the heater power frequency (60Hz) input from pin 19.

Table 2-5 Grid/Segment Matrix

SEGMENT \ GRID	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1
a	SP		a	a	:	a	a		a	a
b		AUX	b	b	3	b	b		b	b
c		TIMER	c	c		c	c		c	c
d		PROG	d	d		d	d	CH	d	d
e	LP		e	e		e	e	IRT	e	e
f	SLP		f	f		f	f	PM	f	f
g		ON	g	g		g	g	AM	g	g
h		OFF	1	2		4	WKL	WED		AFC
i		1W	2W	SUN		MON	TUE	THU	FRI	SAT

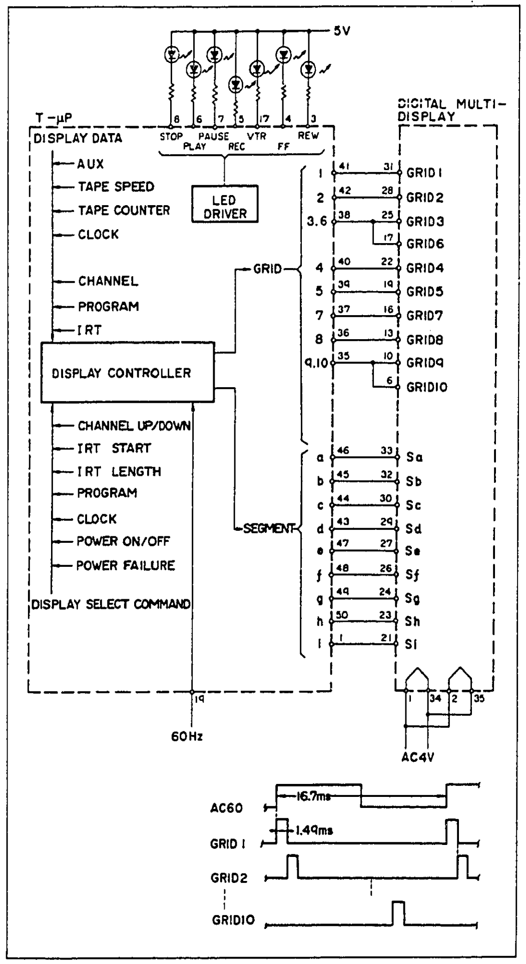

5V
T-µP
DISPLAY DATA
STOP
PLAY
PAUSE
REC
VTR
FF
REW
LED DRIVER
AUX
TAPE SPEED
TAPE COUNTER
CLOCK
CHANNEL
PROGRAM
IRT
DISPLAY CONTROLLER
CHANNEL UP/DOWN
IRT START
IRT LENGTH
PROGRAM
CLOCK
POWER ON/OFF
POWER FAILURE
DISPLAY SELECT COMMAND
GRID
SEGMENT
DIGITAL MULTI-DISPLAY
GRID1
GRID2
GRID3
GRID6
GRID4
GRID5
GRID7
GRID8
GRID9
GRID10
Sa
Sb
Sc
Sd
Se
Sf
Sg
Sh
Si
60Hz
AC4V
AC60
GRID 1
GRID2
GRID10
16.7ms
1.49ms

Fig. 2-15 Simplified Digital Multidisplay/Indicator Control Diagram

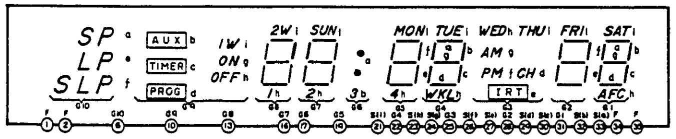

SP
LP
SLP
AUX
TIMER
PROG
1W
ON
OFF
2W
SUN
MON
TUE
WED
THU
FRI
SAT
AM
PM
CH
IRT
WKL
AFC

Fig. 2-16 Grid/Segment Location

2-6 Clock/Timer/IRT Control

The VT-1100A/1105A have timer recording and instant recording timer (IRT) functions. When the operator inputs required TV programs and the times using these functions, recording starts automatically when the preset time is reached and the VTR power is turned off or it enters the timer standby mode when the recording stops.

The timer can preset 2 TV programs in 2 weeks including weekly or daily programs.

The IRT has a simplified program setting function which is able to timer-record one program.

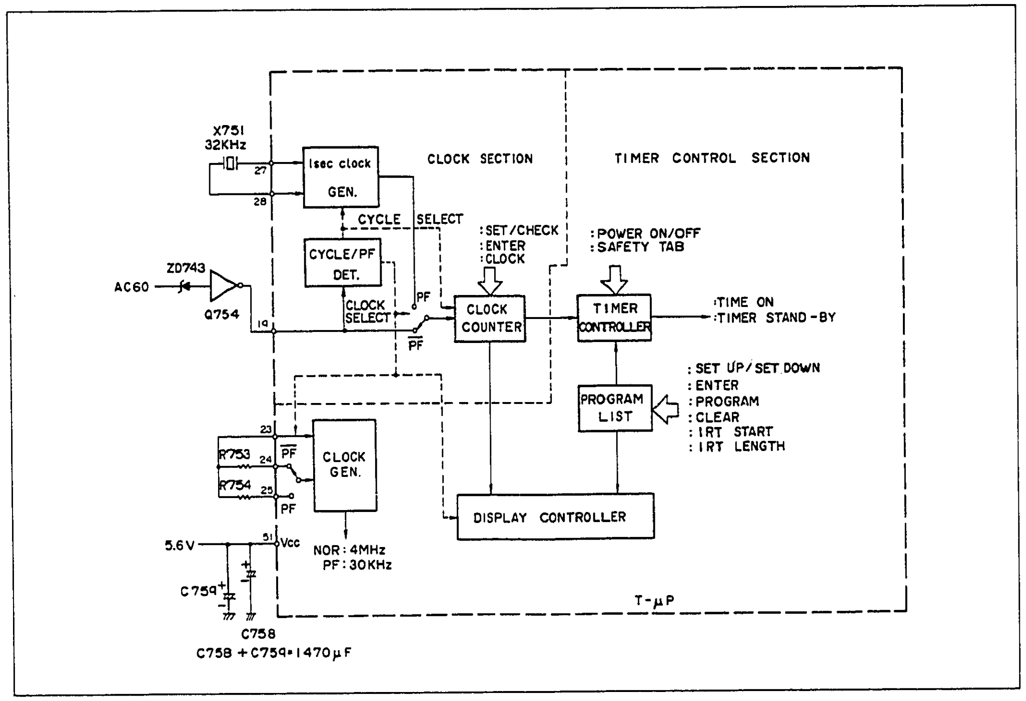


Fig. 2-17 Simplified Clock/Timer/IRT Control Diagram

Fig. 2-17 is a simplified diagram of the clock/timer/IRT control circuit in T-μP. The power input, pin 51, of T-μP receives the 5V source from the power supply circuit normally and from the large-capacitance capacitor C759 during a power failure. When a power failure occurs, the latter power supply maintains the present time and input data in the program list for approx. 1 second. The clock/timer/IRT control is realized by the clock section determining the time, the timer control section determining the timer output and the program list storing the required TV-program data.

The clock section consists of the clock counter, 1 sec clock generator and power cycle/failure detector.

Clock Counter:

Counts the power frequency input from pin 19 via inverter Q754 in the normal mode and the frequency output from the REF 50/60 generator in T-μP during a power failure to determine the time and date. The determined time and date are indicated in the digital multidisplay via the display controller. The time is corrected when the data in the clock counter is modified by operating the CLOCK, ENTER and SET keys which are input via the key matrix circuit.

1 sec Clock Generator:

When a power failure occurs, the clock (power frequency) signal is not supplied to the clock counter. This generator generates a signal the frequency of which is near the frequency of the clock signal which has been supplied before a power failure and supplies it to the clock counter. The 1 sec clock generator generates the frequency determined by the resonance frequency of the quartz crystal connected to pins 27 and 28 and counts it down to the power frequency detected by the power cycle/failure detector.

Power Cycle/Failure Detector:

Always detects the frequency and supply state (power failure) of the AC power supply input via pin 19. When the power frequency period is less than 18.3 ms, the detector detects that the power frequency is 60Hz, and when the period is between 18.3 and 50 ms, it detects 50Hz, and when the period is 50 ms or more, it detects a power failure.

When receiving the power frequency detection output, the power cycle/failure detector controls the following 2 items:

1. Determines the division ratio so the output frequency of the 1 sec clock generator is equal to the power frequency before a power failure occurs.
2. Determines the preset data in the clock counter to correct the counting difference between power frequencies of 50Hz and 60Hz.

When receiving the power failure detection output, the power cycle/failure detector controls the following 3 items:

1. Selects the clock signal applied to the clock counter. It selects the power frequency input at pin 19 normally and selects the 1 sec clock generator output during a power failure.
2. Opens all input ports to reduce consumed power of T-μP during a power failure. This switches off the indicators and digital multidisplay.
3. Switches the μP's system clock frequency to reduce the consumed power of the μP. It selects resistor R753 connected to pin 24 normally to switch the system clock frequency to 4MHz and selects R754 connected to pin 25 during a power failure to switch the frequency to 30kHz.

The timer controller section uses the data (time and date) output from the clock counter section, data in the program list described later and the operation mode data from S-μP, and determines the command codes applied to S-μP.

When a program is set and the power switch of the VTR is turned off, T-μP transmits the "TIMER STAB" code to S-μP to set the VTR to the timer standby mode.

When a cassette without its safety tab is loaded and the timer standby code is applied to the S-μP, the S-μP ejects the cassette immediately and the T-μP flashes "TIMER" in the digital multidisplay to warn the operator.

When the "TIME ON" time is reached, T-μP transmits the "TIME ON" code to S-μP.

When receiving this code, S-µP transmits the "REC" code to T-µP. During the TIME ON period, T-µP controls the TIME ON code output so the operation mode data sent from S-µP is always "REC". However, T-µP interrupts the timer recording when condensation (dew) occurs or the tape end is detected.

The program list stores the input data - times and dates of programs for timer recordings and the time (length) of IRT program, etc. Table 2-6 shows the data stored in the program list.

TIMER PROGRAM LIST				
PROG. NO.	CHANNEL	DAY	TIME ON	TIME OFF
1				
2				
3				
4				
IRT PROGRAM LIST				
CHANNEL	TIME ON	LENGTH		

Table 2-6

The above data is input by operating 9 keys (SET UP, SET DOWN, STORE, PROGRAM, CLEAR, IRT START, IRT LENGTH, CHANNEL UP, CHANNEL DOWN) as described in "Key Input". The programming procedure is as follows.
When the "PROG." key is pressed, the digital multidisplay enters the program display mode and the program No. can be selected and input. The program No. is selected by pressing the "SET UP/DOWN" key. Pressing the "STORE" key enables the channel, day, time ON and time OFF to be input in sequence in the determined program No. line. The setting procedure is that the "SET UP/DOWN" key is pressed to select the input data, then the "STORE" key is pressed to store the data in the designated line in the program list. Data input of one program is completed in this way and is followed by the data input procedure of the next program.
When the necessary data input is completed, the program Nos. (1, 2 or W) light from flashing.
The input data of each program No. is deleted when the timer recording of the program is completed or the "CLEAR" key is pressed after recalling the program No. However, the input data of the weekly or daily program is erased only when the "CLEAR" key is pressed.

IRT Control

Instant recording timer (IRT) is timer recording with the simplified program setting procedure. The recording start time can be set within a maximum of 24 hours from the present time at 30-minute or 1-hour intervals. The recording end time is determined automatically by selecting 6 recording length times (30, 60, 90, 120, 180, 240 minutes). When a recording length time is selected without setting the recording start time, the present time is set automatically for the start time and recording starts immediately.
To release IRT, set the recording length time to display "0:00" and then wait for 8 seconds. The above times can be set only when the VTR power is turned on.
The remaining time to be recorded is indicated in the digital multidisplay during IRT. When the display reaches "0:00", the VTR power is turned off.

3. SERVO

3-1 General

The servo system in the VTR is divided into three loops according to the objects of control - the cylinder servo controlling the rotating video heads, the capstan servo controlling the video tracks and the tension servo.

The tension servo loop maintains the tape tension constant; it keeps the compression strength of tape against the video heads in the optimum condition so a stable RF signal is produced during recording and playback. The tension servo operation is performed entirely mechanically.

Fig. 3-1 is a simplified cylinder and capstan servo operation diagram. The cylinder servo loop controls the phase and speed of the cylinder motor in the video head assembly; it determines the position of vertical sync signal on the video tape to satisfy the specified format (VHS magnetic tape pattern in the VHS system) and suppresses the time axis fluctuations of video signal to become minimum.

The capstan servo loop controls the phase and speed of the capstan motor in the capstan assembly so the video heads can trace (play back) the recorded video tracks correctly.

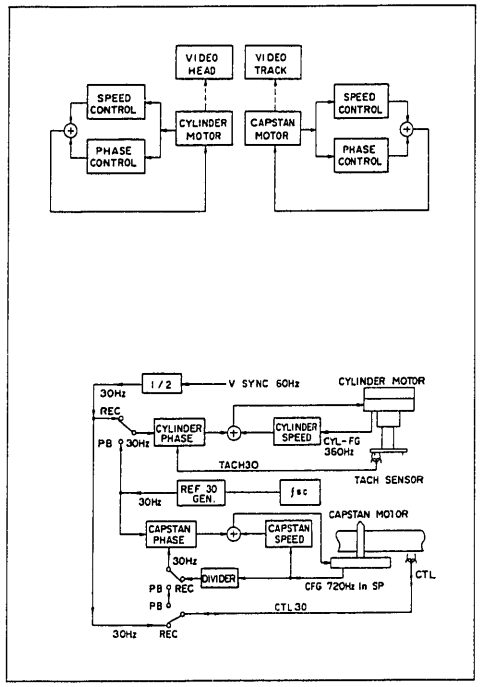


Fig. 3-1 Cylinder/Capstan Control

Recording Cylinder Servo

From the composite video signal supplied from a TV or video camera, only V. SYNC (60Hz) is derived by the video circuit in the VTR and is divided by two to become SYNC 30. Using this SYNC 30 as a reference signal and the TACH signal as a comparison signal, the cylinder servo loop compares the phases of both signals and generates an error voltage according to the phase difference.
The cylinder servo loop detects the period of CYL-FG pulses of which the frequency is 360Hz with respect to 30 rotations of the cylinder and generates an error voltage according to the rotation speed error (wow & flutter).

The cylinder servo loop feeds back both error voltages negatively to the cylinder to control the speed and phase of the cylinder.

Recording Capstan Servo

The capstan servo loop must run the tape smoothly at an accurate speed to record the SYNC 30 signal correctly on the bottom track of the tape without time fluctuations. To do this, the capstan servo loop detects the period of CFG pulses (720Hz in SP) to control the speed. To control the phase, the capstan servo loop compares REF30Hz produced by the crystal oscillator in the VTR and 30Hz obtained by dividing the CFG frequency and uses the resultant signal.

The tape speed during recording can be set by operating the tape speed select switch.

Playback Cylinder Servo

The playback cylinder servo operates in the same way as the recording cylinder servo except that it changes the reference signal from SYNC 30 to REF30Hz produced by the crystal oscillator.

Playback Capstan Servo

The capstan servo loop uses the CTL pulse (30Hz) played back by the CTL head as the comparison signal for the phase control circuit during playback. This is greatly different from the recording capstan servo and the important point in the playback capstan servo. The playback capstan servo compares the phases of REF30Hz and CTL30Hz on the tape to control the tape transport. The speed control loop is the same as in recording.

Since the tape speed is automatically detected and switched when a recorded tape is running, the tape speed select switch on the front panel is not concerned with tape speed switching during the PB mode.

The tracking is optimized by shifting the phase of the capstan.

Servo Control Signals

As described previously, the servo system handles different signals in each mode. The signals are collected and listed below.

Cylinder Servo

System	Mode	Reference Signal	Waveform	Comparison Signal	Waveform
Cylinder Phase Control	Recording	SYNC30Hz	Sample pulse	TACH30	Digital trapezoid
	Playback	REF30Hz		TACH30	
Cylinder Speed Control	Recording	CYL-FG 360Hz	Sample pulse	CYL-FG 360 Hz	Digital sawtooth
	Playback	CYL-FG 360Hz		CYL-FG 360 Hz	

Capstan Servo

System	Mode	Reference Signal	Waveform	Comparison Signal	Waveform
Capstan Phase Control	Recording	REF30Hz	Digital trapezoid	CFG30 *2	Sample pulse
	Playback	REF30Hz		CTL30	
Capstan Speed Control	Recording	CFG *1	Sample	CFG *1	Digital sawtooth
	Playback	CFG *1		CFG *1	

*1: The frequency of CFG pulse is varied in various conditions as follow.

1. SP: 720Hz
2. LP: 360Hz
3. EP: 240Hz
4. SEARCH: 2160Hz

*2: CFG30 is produced by dividing the above CFG to 30Hz.

3-2 Servo Circuit

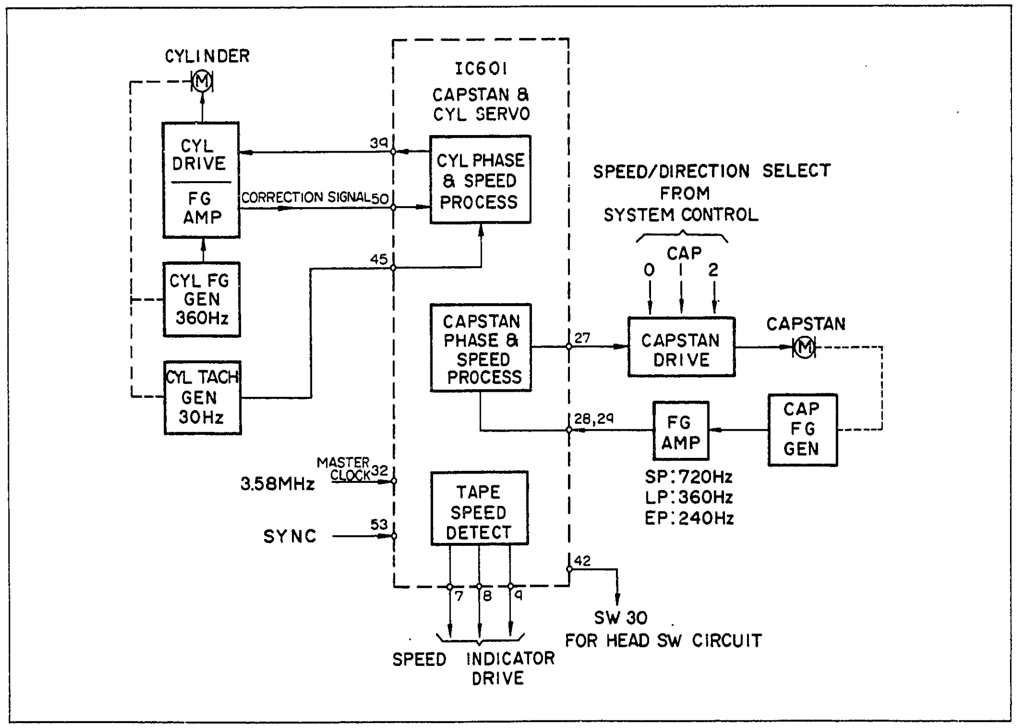

CYLINDER
M
CYL DRIVE
FG AMP
CYL FG GEN 360Hz
CYL TACH GEN 30Hz
IC601
CAPSTAN & CYL SERVO
39
CORRECTION SIGNAL
50
45
CYL PHASE & SPEED PROCESS
CAPSTAN PHASE & SPEED PROCESS
TAPE SPEED DETECT
3.58MHz
MASTER CLOCK
32
SYNC
53
7
8
9
SPEED INDICATOR DRIVE
42
SW 30 FOR HEAD SW CIRCUIT
SPEED/DIRECTION SELECT FROM SYSTEM CONTROL
CAP
0
1
2
27
CAPSTAN DRIVE
CAPSTAN
M
28,29
FG AMP
CAP FG GEN
SP:720Hz
LP:360Hz
EP:240Hz

Fig. 3-2 Servo Block Diagram

Fig. 3-2 is a block diagram of the servo circuit. The cylinder drive signal leaves IC601 at pin 39 from which it is applied to the cylinder drive FG amplifier circuit. This cylinder drive IC applies the drive signal to the cylinder motor and amplifies the FG signal. As the cylinder rotates, it is mechanically coupled to both the cylinder FG generator and cylinder tach generator. These two signals are used as the feedback and comparison signals in cylinder motor servo loops. The cylinder FG (frequency generator) signal is 360 Hz and is applied to the FG amplifier in the cylinder drive IC. A correction signal is generated by the FG generator and applied to pin 50 of IC601, the capstan and cylinder servo processing IC.

The capstan motor drive signal generated by IC601 is supplied from pin 27 to the capstan drive circuit. The capstan drive circuit also receives speed control signals from the system control µP. The capstan control signals are necessary to allow different modes of operation SP, LP, and EP, and fast foward, rewind, and search. As the capstan motor rotates, it is electromechanically coupled to the capstan FG generator which generates a 720Hz signal in the SP mode, 360Hz in LP, 240Hz in EP and 2160Hz during forward and reverse search. The capstan FG signal is then passed through an FG amplifier and applied to pins 28 and 29 of IC601.

During playback, the speed detection circuit in IC601 determines the playback speed. Pins 7, 8 and 9 provide this information to the system control circuit and drive the speed indicator in the digital multidisplay.

Capstan and cylinder servo IC601 also receives a 3.58 MHz signal at pin 32 from the signal processing circuit. The 3.58 MHz signal is used in the IC as a master clock to synchronize the operation of the servo loops. A composite sync is also applied to pin 53; this provides synchronization during various modes of operation. The 30Hz signal used in the head switching circuit is supplied from pin 42 of the capstan/cylinder servo IC601.

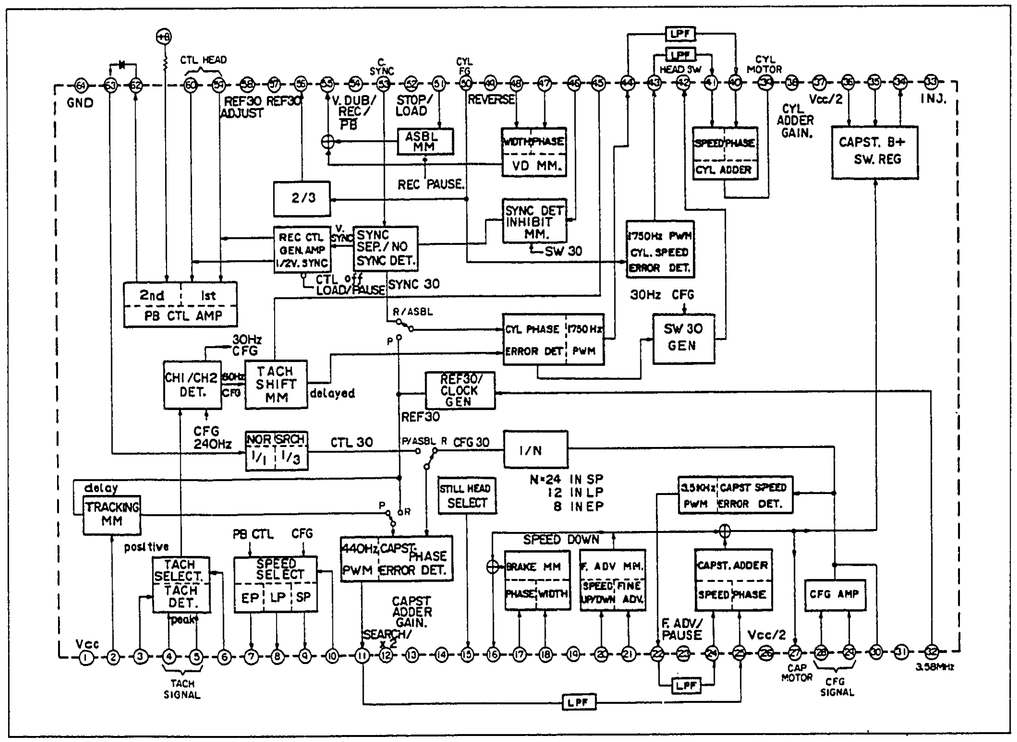
3-3 Capstan and Cylinder Servo Processing

3-3-1 General

Fig. 3-3 is a block diagram of the main servo processing IC. Digital counters are utilized extensively within the IC for the speed and phase loops of both cylinder and capstan. The digital counters detect speed and phase errors and generate the correction signals. Earlier servo systems utilized a combination of both digital and analog circuits in order to generate trapezoid correction waveforms. The digital capstan and cylinder servo processing IC, IC601, does not generate these waveforms internally. Instead, the correction signal generated by the digital counter is utilized to control the duty cycle of a pulse width modulated circuit to develop the capstan and cylinder drive signals.

The CYL-FG signal is applied to pin 50. The cylinder FG signal is used as a comparison signal in the cylinder speed loop. The tach signal is applied to pins 4 and 5 of IC601, peak-detected, a positive tach pulse is selected and is applied to the tach shift monostable multivibrator (MM) which supplies the delayed tach signal to both the cylinder phase loop and the switching 30Hz generator. The switching 30Hz generator in IC601 supplies a head switching 30Hz signal from pin 42. The cylinder phase loop utilizes the delayed tach signal provided by the tach shift MM as a comparison signal. The delayed tach signal is compared to the composite sync information at pin 53 during recording and the reference 30Hz generator output during playback. The reference 30Hz signal is generated by dividing down the 3.58MHz supplied to pin 32. During playback, the output from the reference 30Hz generator (30Hz) is applied to the capstan phase error detector via the tracking MM. During recording, vertical sync information is supplied to the record control track generator. The record control pulse is supplied from pins 59 and 60 to the control track head.

The cylinder speed error PWM signal from pin 43 is passed through a lowpass filter to pin 41. The cylinder phase error PWM



+B
CTL HEAD
C. SYNC
CYL FG
LPF
LPF
HEAD SW
CYL MOTOR
GND
REF30 ADJUST
REF30
V. DUB/ REC/ PB
STOP/ LOAD
REVERSE
CYL ADDER GAIN.
Vcc/2
INJ.
ASBL MM
WIDTH PHASE
VD MM.
SPEED PHASE
CYL. ADDER
CAPST. B+ SW. REG
REC PAUSE.
2/3
SYNC DET INHIBIT MM.
SW 30
REC CTL GEN. AMP 1/2V. SYNC
V. SYNC
SYNC SEP./ NO SYNC DET.
1750Hz PWM CYL. SPEED ERROR DET.
CTL off LOAD/PAUSE
SYNC 30
2nd
Ist
PB CTL AMP
30Hz CFG
R/ASBL
CYL PHASE ERROR DET
1750Hz PWM
SW 30 GEN
30Hz CFG
P
CHI/CH2 DET.
60Hz
CFG
TACH SHIFT MM
delayed
REF30/ CLOCK GEN
REF30
CFG 240Hz
NOR SRCH
1/1
1/3
CTL 30
P/ASBL
R
CFG 30
I/N
N=24 IN SP
12 IN LP
8 IN EP
delay
TRACKING MM
STILL HEAD SELECT
3.5KHz PWM
CAPST SPEED ERROR DET.
P
R
positive
PB CTL
CFG
440Hz PWM
CAPST. PHASE ERROR DET.
SPEED DOWN
TACH SELECT.
TACH DET.
SPEED SELECT
EP
LP
SP
BRAKE MM
PHASE
WIDTH
F. ADV MM.
SPEED UP/DOWN
FINE ADV.
CAPST. ADDER
SPEED
PHASE
CFG AMP
peak
CAPST ADDER GAIN.
SEARCH/ x2
F. ADV/ PAUSE
Vcc/2
Vcc
TACH SIGNAL
LPF
LPF
CAP MOTOR
CFG SIGNAL
3.58MHz

Fig. 3-3 Detailed Main Servo Processing IC Block Diagram

signal from pin 44 is supplied through another lowpass filter to pin 40. The cylinder speed and phase error signals from pins 41 and 40 respectively are applied to an adder circuit to develop the cylinder drive signal at pin 39.

The capstan phase and speed loops are similar to those of the cylinder. The frequency of the capstan FG signal (CFG) depends upon the mode of operation. The CFG signal is applied from pins 28 and 29 of IC601 to the capstan speed loop and capstan FG 30Hz generator circuits. The capstan FG signal is compared to an internal reference value in the capstan speed loop generating the speed error PWM signal at pin 22. The capstan FG signal frequency is 720 Hz for SP, 360 Hz for LP, and 240 Hz for EP. The capstan FG 30 (CFG) generator consists of a programmable divider which develops a 30Hz output signal. During the SP mode, the FG signal is divided by 24, in LP, by 12 and in EP, by 8. During recording the CFG 30 signal is used as the comparison signal in the capstan phase loop. During playback, a 30Hz comparison signal is generated from the playback control track pulse (CTL) which is applied at pins 59 and 60. The CTL pulse is amplified by the 1st and 2nd amplifiers in IC601 and is output from pin 62. The amplified CTL pulse at pin 62 is reapplied through pin 63 to the CTL divider in IC601. The CTL divider consists of a programmable divider which develops a 30Hz output signal. In modes other than search, the CTL signal is directly applied to the capstan phase loop for comparison. The CTL signal is divided by 3 during search.

A reference signal for the capstan phase loop during playback is supplied by the tracking MM. The tracking MM adjusts the delay of the reference 30Hz from the reference 30Hz generator. During recording, the reference signal for capstan phase is applied directly from the reference 30Hz generator. The capstan phase error PWM signal leaves IC601, pin 11, and is applied through a lowpass filter to pin 25. The speed error PWM signal from the capstan speed loop is applied to a lowpass filter from pin 22 and is fed back into the IC via pin 24. The capstan speed and phase error signals from pins 24 and 25 are applied to an adder circuit to generate the capstan drive signal at pin 27.

3-3-2 Cylinder processing

Fig. 3-4 is a simplified diagram of the cylinder speed control circuit. The cylinder FG signal (360Hz), amplified by motor driver/amplifier IC1651, is applied to pin 50 of IC601. Then the cylinder FG signal is applied to the cylinder speed error detection circuit. The cylinder speed error detection circuit consists of three digital counters which generate the digital speed error signal. A 1.8MHz (fsc/2) clock signal which is generated from the counted down 3.58MHz signal determines the speed at which the counters operate and is applied to the cylinder error detect circuit. The cylinder speed must be varied slightly during still, forward and reverse search modes. The STILL, SEARCH and REVERSE commands are applied to pins 23, 12 and 49 respectively. The cylinder speed error detection circuit also supplies a control signal to the cylinder phase loop to turn it on and off. The digital speed error signal generated by the cylinder speed error detection circuit is applied to the speed PWM which operates at a frequency of 1750Hz. The digital speed error signal controls the duty cycle (or "on" time) of the speed PWM circuit. The detail operation of the cylinder speed loop is described later.

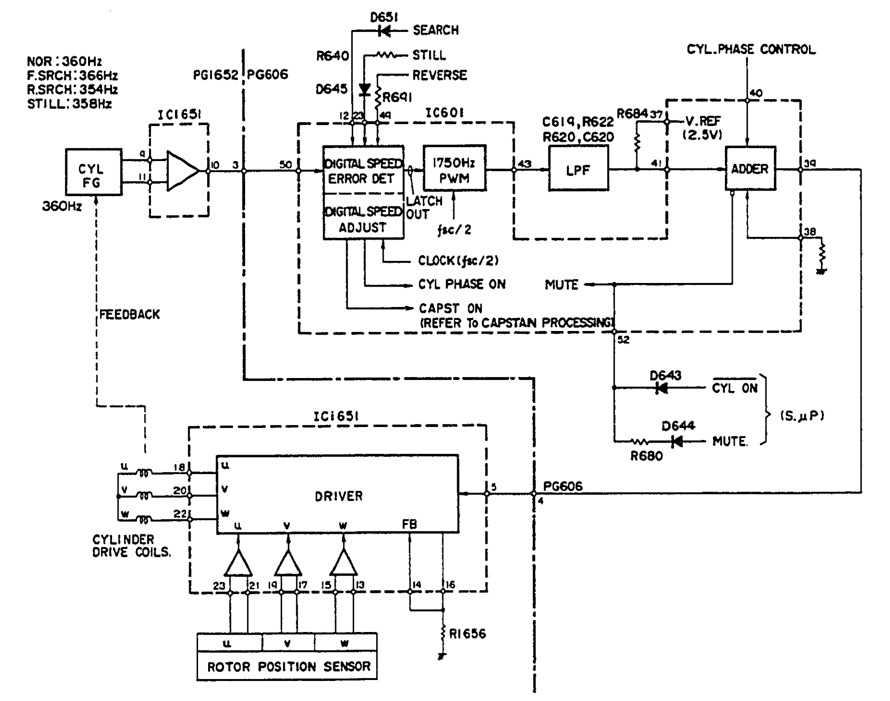


Fig. 3-4 Simplified Cylinder Speed Control Circuit Diagram

The PWM signal is supplied from pin 43 to a lowpass filter which generates a DC speed error correction voltage which is input via pin 41. The DC speed error correction voltage is applied to an adder circuit together with the phase error correction voltage from pin 40. The combined speed and phase error correction voltages generate a cylinder drive voltage at pin 39 of IC601.

During the stop mode it is necessary to stop the cylinder from rotating. To do this, a cylinder servo operation control command, "$\overline{\text{CYL ON}}$", is applied to pin 52 from the S-μP. When the voltage at pin 52 goes "Hi", the cylinder drive voltage at pin 39 becomes zero.

As with the cylinder speed, cylinder phase correction is performed in servo processing IC601. Fig. 3-6 is a simplified diagram of the cylinder phase control circuit. The cylinder tach signal is applied to the shaper at pins 4 and 5 of IC601. This shaper peak-detects the cylinder tach signal to form a pulse with a steep ramp. This output is applied to the tach selector. The tach selector selects the positive pulses of the cylinder tach signal in a VTR with 2 (or 3) video heads and selects the negative pulses in a VTR with 4 (or 5) video heads in the SP mode. This selection is determined by the voltage applied to pin 6 of IC601. To select positive pulses, pin 6 is set to "Hi" (5V), and to select negative pulses, pin 6 is set to "Lo" (GND). Since the VT-1100A/1105A have 2 video heads, pin 6 is held at "Hi" (5V). The output of the tach selector is applied to the CH1/CH2 tach separator. The CH1/CH2 tach separator provides two outputs, a 30Hz signal which is applied to the switch 30Hz generator and a divided FG (60Hz signal) which is applied to the tach shift MM.

The delay of the tach shift MM is determined by time constant (RT601, C617) at pin 45. The output of the tach shift MM is applied to both the switching 30Hz generator and the cylinder phase error detection circuit. This delayed tach signal operates as the comparison signal for the cylinder phase error detection circuit.

During recording, the reference signal is developed from the composite sync signal which is applied to pin 53 of IC601. This composite sync signal is applied to a sync separator which supplies a 60Hz output. The 60Hz from the sync separator is applied to the cylinder phase error detection circuit and to the record control track pulse (CTL) generator. The record CTL pulse generator is triggered by the 30Hz sync signal from the sync separator and produces a 30Hz record CTL pulse whose duty cycle is set to approx. 70%. The record CTL pulse is applied through pins 60 and 59 to the control head to drive it.

During playback, the reference signal for the cylinder phase error detection circuit is developed by the reference 30Hz generator. A 3.58MHz signal is supplied from the signal processing circuit to pin 32 of IC601. The reference 30Hz generator counts down the 3.58MHz signal and supplies a 30Hz reference signal through the record/playback switch to the cylinder phase error detection circuit. This 30Hz signal is compared to the comparison signal from the tach shift MM. With a rate of 447kHz, the cylinder phase error detection circuit generates the phase error correction data. The phase error correction data is applied to the cylinder phase PWM circuit operating at a rate of 1.75kHz and controls the duty cycle.

As described earlier, the phase PWM duty cycle is set to 50% by a control signal from the speed loop during starting up. The PWM signal is applied to a lowpass filter at pin 44. The lowpass filter generates a DC phase error correction voltage and applies it to a limiter circuit. The limiter is provided to prevent the cylinder phase processing circuit from attempting to correct speed errors. Then the DC phase error correction voltage is applied to pin 40. The phase error and speed error signals are then applied to an adder circuit which develops the cylinder drive signal at pin 39.

Since the unit features noise-locked search in both forward and reverse, the cylinder motor must be phase locked. Cylinder phase lock during search is performed by adjusting the reference 30Hz. During forward search, the reference 30Hz signal is adjusted to 29.49Hz, and in reverse search, to 30.51Hz.

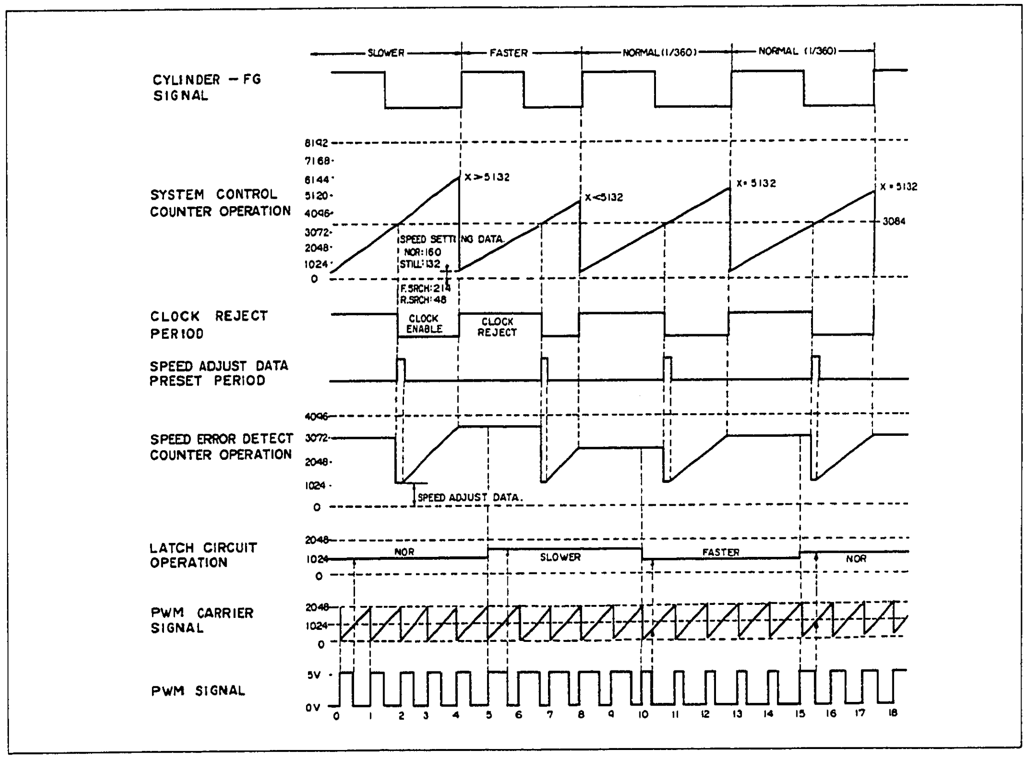


Fig. 3-5 Cylinder Speed Error Data Development

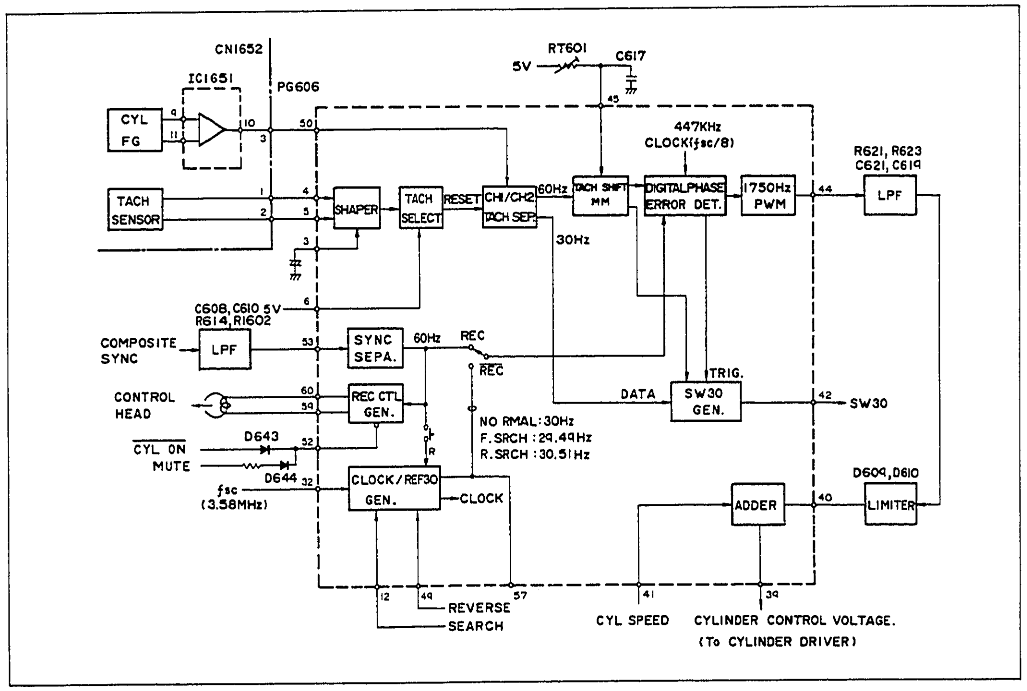

CN1652
IC1651
PG606
CYL FG
9
11
10
3
50
RT601
5V
C617
45
447KHz CLOCK(fsc/8)
R621, R623
C621, C619
TACH SENSOR
1
2
4
5
3
SHAPER
TACH SELECT
RESET
CH1/CH2 TACH SEP.
60Hz
TACH SHIFT MM
DIGITAL PHASE ERROR DET.
1750Hz PWM
44
LPF
30Hz
C608, C610 5V
R614, R1602
6
COMPOSITE SYNC
LPF
53
SYNC SEPA.
60Hz
REC
REC
TRIG.
DATA
SW30 GEN.
42
SW30
CONTROL HEAD
60
59
REC CTL GEN.
NO RMAL:30Hz
F.SRCH :29.49Hz
R.SRCH :30.51Hz
CYL ON
MUTE
D643
52
D644
32
R
fsc (3.58MHz)
CLOCK/REF30 GEN.
CLOCK
D609, D610
ADDER
40
LIMITER
12
49
57
REVERSE
SEARCH
41
39
CYL SPEED
CYLINDER CONTROL VOLTAGE.
(To CYLINDER DRIVER)

Fig. 3-6 Simplified Cylinder Phase Control Circuit Diagram

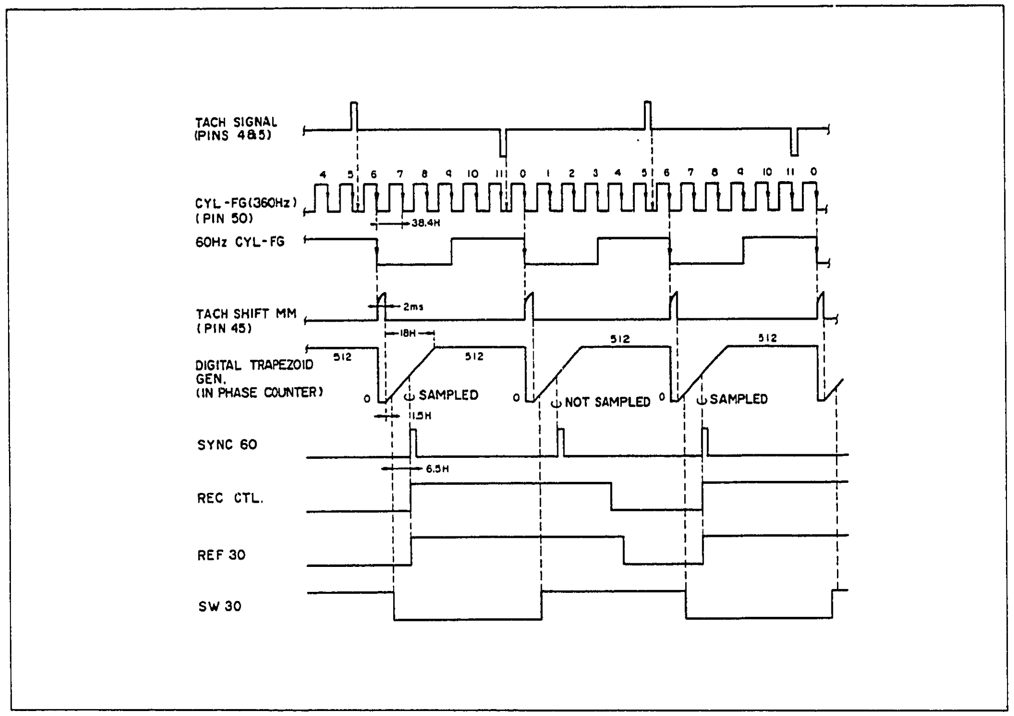

TACH SIGNAL (PINS 4&5)
CYL-FG(360Hz) (PIN 50)
60Hz CYL-FG
TACH SHIFT MM (PIN 45)
DIGITAL TRAPEZOID GEN. (IN PHASE COUNTER)
SYNC 60
REC CTL.
REF 30
SW 30
38.4H
2ms
18H
1.5H
6.5H
512
SAMPLED
NOT SAMPLED
SAMPLED

Fig. 3-7 Cylinder Phase Error Data Development

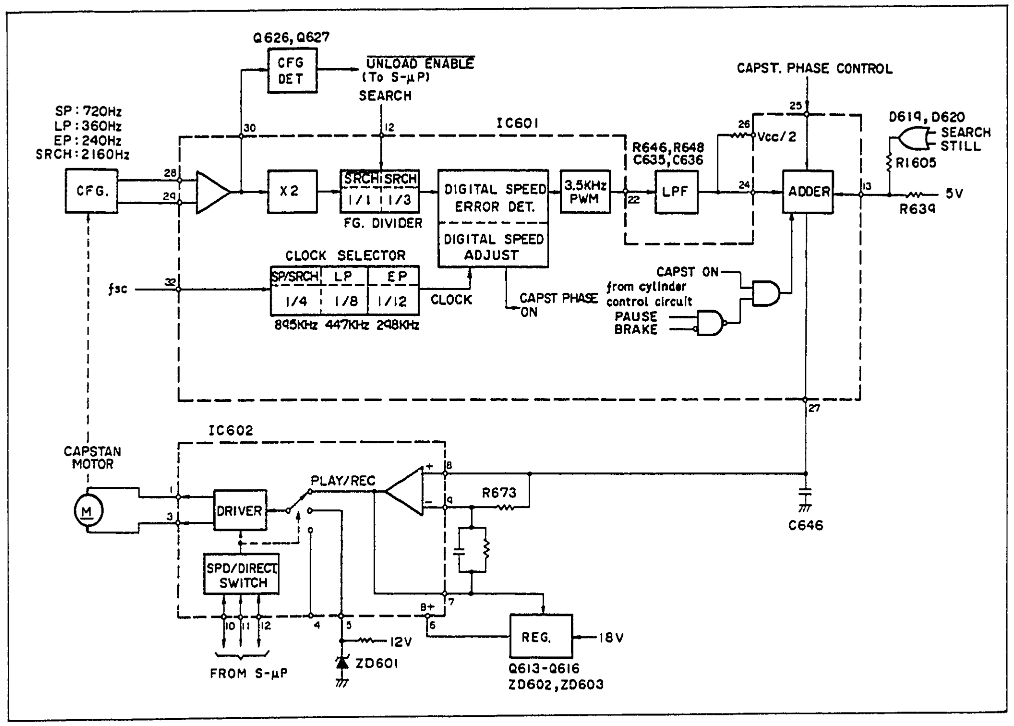

Q626,Q627
CFG DET
UNLOAD ENABLE (To S-μP)
SEARCH
CAPST. PHASE CONTROL
SP:720Hz
LP:360Hz
EP:240Hz
SRCH:2160Hz
IC601
CFG.
X2
SRCH 1/1 SRCH 1/3
FG. DIVIDER
DIGITAL SPEED ERROR DET.
DIGITAL SPEED ADJUST
3.5KHz PWM
R646,R648 C635,C636
LPF
Vcc/2
ADDER
D619,D620
SEARCH STILL
R1605
5V
R639
CLOCK SELECTOR
SP/SRCH LP EP
1/4 1/8 1/12
895KHz 447KHz 298KHz
CLOCK
CAPST PHASE ON
CAPST ON
from cylinder control circuit
PAUSE
BRAKE
fsc
IC602
CAPSTAN MOTOR
M
DRIVER
PLAY/REC
R673
SPD/DIRECT SWITCH
FROM S-μP
12V
ZD601
REG.
18V
Q613-Q616 ZD602,ZD603
C646

Fig. 3-8 Simplified Capstan Speed Control Circuit Diagram

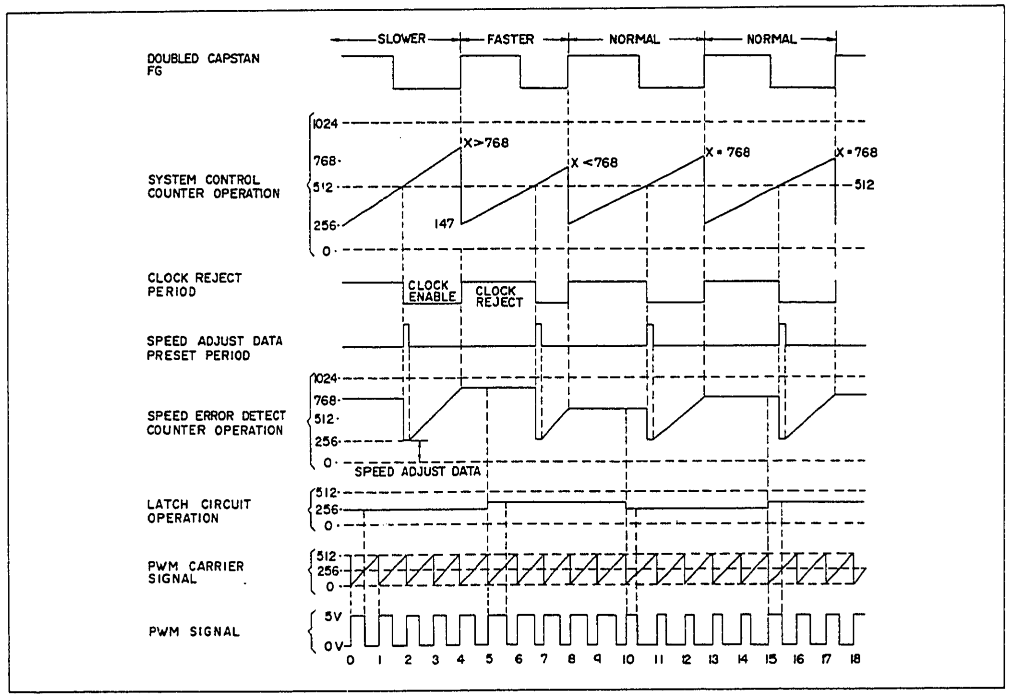

SLOWER
FASTER
NORMAL
NORMAL
DOUBLED CAPSTAN FG
SYSTEM CONTROL COUNTER OPERATION
1024
768
512
256
0
X>768
X<768
X=768
147
CLOCK REJECT PERIOD
CLOCK ENABLE
CLOCK REJECT
SPEED ADJUST DATA PRESET PERIOD
SPEED ERROR DETECT COUNTER OPERATION
SPEED ADJUST DATA
LATCH CIRCUIT OPERATION
PWM CARRIER SIGNAL
PWM SIGNAL
5V
0V
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

Fig. 3-9 Capstan Speed Error Data Development (in LP Mode)

3-3-3 Capstan processing

The capstan speed processing circuit in IC601 is similar to the cylinder speed processing circuit. Fig. 3-8 is a simplified diagram of the capstan speed control circuit. The frequency of the capstan FG signal applied to pins 28 and 29 varies depending upon the speed of operation (SP, LP, EP). The capstan FG signal frequency is 720Hz in SP, 360Hz in LP, and 240 Hz in EP. The capstan FG signal is applied from pins 28 and 29 to the phase loop and a doubler (X2) circuit. During normal play and record operations, the X2 capstan FG signal is applied directly to the capstan speed error detection circuit for comparison.

During forward and reverse search, the capstan rotates at a faster rate and generates a capstan FG signal of 2160Hz. In order for the capstan speed processing circuit to operate correctly, the capstan FG signal must be divided down during search mode. This is performed by applying the SEARCH command, "Hi", to pin 12. A "Hi" at pin 12 routes the FG signal through the divide-by-3 circuit in the search mode. The reference signal for the capstan speed detection circuit is generated internally from a master clock which is divided down from 3.58MHz. This reference signal also varies depending on the mode of operation - 895kHz during SP or search, 447kHz in LP, and 298kHz in EP. Selection of the correct reference signal is controlled by the speed select circuit in IC601.

The digital capstan speed error signal is supplied from the error detection circuit to the capstan speed PWM operating at 3.5kHz and this controls the duty cycle.

The PWM signal is applied from pin 22 to a lowpass filter which generates a DC error signal. This speed error voltage is applied at pin 24 together with the phase error signal from pin 25 to an adder circuit.

The adder circuit is active when the capstan servo operation command, "CAPST ON", is applied from the cylinder processing circuit or when the brake pulse is generated in the interval brake pulse generator in the still mode.

The "CAPST ON" command goes "Hi" when the cylinder motor reaches approx. 1314 rpm, at which point the capstan motor can turn on.

Capstan phase processing is similar to that of the cylinder. Fig. 3-10 is a simplified diagram of the capstan phase control circuit. During recording, the 30Hz feedback signal required by the capstan phase error detection circuit in IC601 is obtained from the capstan FG signal supplied at pins 28 and 29. Since the capstan FG signal frequency varies according to the speed of operation, it must be applied to the CFG 30Hz generator (FG divider). The CFG 30Hz generator divides the capstan FG signal by a different ratio for the different speeds of operation - by 24 in SP, by 12 in LP, and by 8 in EP. In the record mode, the capstan phase error detection circuit also receives reference 30Hz generated by applying 3.58MHz at pin 32 to the reference 30Hz generator. The capstan phase error detection circuit has a frequency of 447 kHz, which is generated by the master clock. By comparing the 30Hz that is generated by the CFG 30 generator and the reference 30Hz, the capstan phase error detection circuit supplies the digital data to the phase PWM. The digital data controls the duty cycle of the phase PWM which operates at 440 Hz, generating the phase error correction signal. The output of the phase PWM is supplied at pin 11 to a lowpass filter. Then the DC phase error correction voltage is applied to an adder circuit generating the capstan drive voltage at pin 25.

During playback, the capstan phase error detection circuit receives a feedback signal from the control track head at pins 59 and 60. The playback control (CTL) signal is applied to the amplifier and then through pins 62 and 63 to the CTL divider. During normal playback, the CTL signal is directly applied to the capstan phase error detection circuit. During search, it is necessary to divide the CTL pulse frequency depending upon the speed of operation. With this, the search signal is supplied at pin 12 to the CTL divider and the reference 30Hz generator. The 30Hz generated by the reference 30Hz generator is supplied to the tracking MM.

As was described previously, the VT-1100A/1105A feature noise-lock search. In order to maintain capstan phase correction during the search mode, the reference 30Hz must be adjusted. During reverse search, the reference 30Hz signal is 30.51Hz, and in forward search, it is 29.49Hz. The tracking MM provides a delayed 30Hz reference signal to the capstan phase error detection circuit. The delay of the tracking MM is controlled by the tracking presets and the tracking control, RV751, connected to pin 2 (on the front panel). The operation of the remaining capstan phase error detection circuit is identical to that in the record mode.

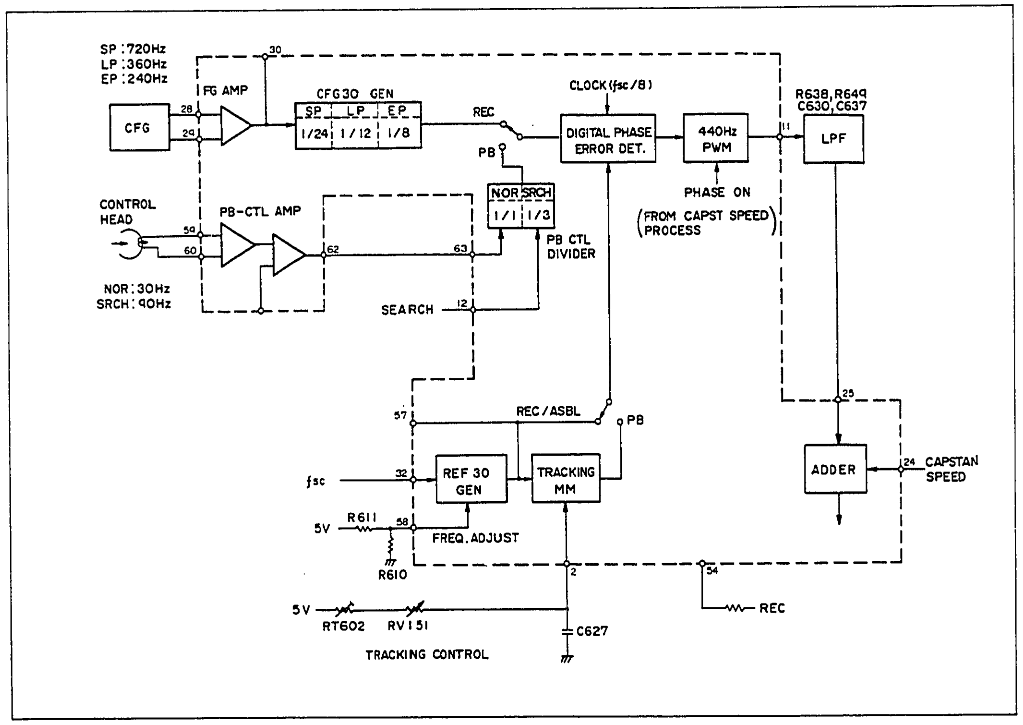

SP : 720Hz
LP : 360Hz
EP : 240Hz
30
FG AMP
CFG
28
29
CFG30 GEN
SP
LP
EP
1/24
1/12
1/8
REC
PB
CLOCK (fsc/8)
DIGITAL PHASE ERROR DET.
440Hz PWM
11
R638, R649
C630, C637
LPF
PHASE ON
(FROM CAPST SPEED PROCESS)
CONTROL HEAD
PB-CTL AMP
59
60
62
63
NOR
SRCH
1/1
1/3
PB CTL DIVIDER
NOR : 30Hz
SRCH : 90Hz
SEARCH
12
57
REC/ASBL
PB
25
fsc
32
REF 30 GEN
TRACKING MM
ADDER
24
CAPSTAN SPEED
5V
R611
58
FREQ. ADJUST
R610
2
54
REC
5V
RT602
RV151
TRACKING CONTROL
C627

Fig. 3-10 Simplified Capstan Phase Control Circuit Diagram

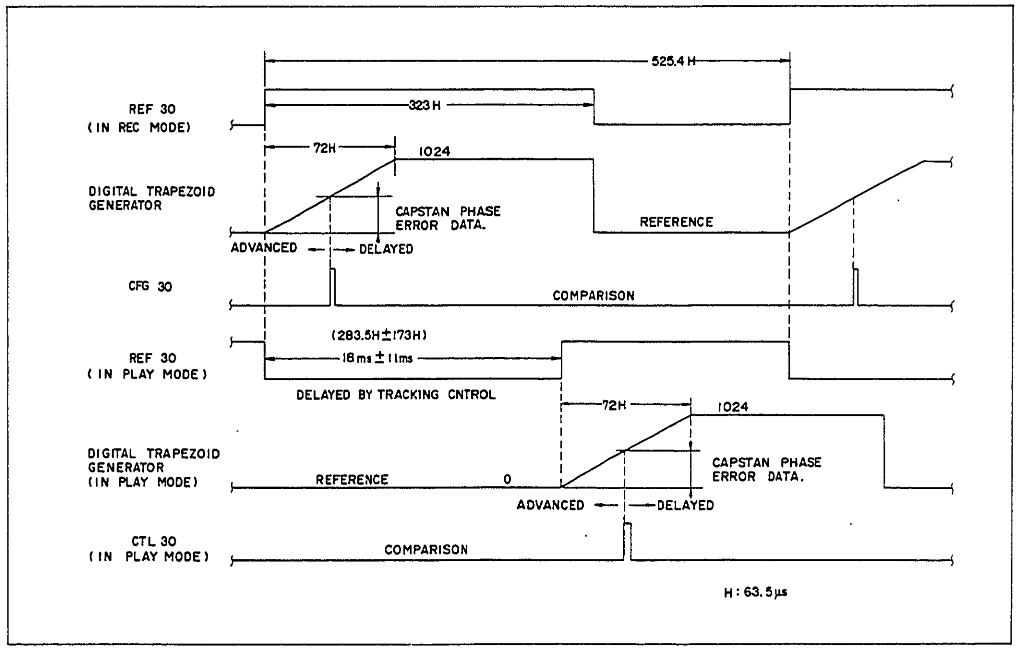


Fig. 3-11 Capstan Phase Error Data Development

3-3-4 Switch 30Hz generator

The tach detector and switch 30Hz generator provide the correct delayed switch 30Hz signal which is used for head switching and provided to the luminance/chroma and system control circuit. Fig. 3-12 is a simplified diagram of the switching 30Hz generator circuit and Fig. 3-13 is a head switching signal development. The switching 30Hz output at pin 42 of IC601 is developed by dividing down the 360Hz cylinder FG signal. The amount of delay introduced to the switching 30Hz output is determined by the delay through the tach shift MM and a fixed approx. 1.5H delay circuit. The tach shift MM is adjustable via the switching point adjustment, RT601, which is connected to pin 45 of IC601.

The cylinder tach and FG signals are applied to pins 4 and 50 respectively. The cylinder tach signal is supplied to the reset terminal of the FG divider circuit. The FG signal is applied to the clock input of the FG divider. By utilizing the tach pulse to reset the FG divider, it is possible to count down the cylinder FG signal of 360Hz to generate switching 30Hz. The FG divider develops two outputs: a 30Hz signal is developed by a divide-by-12 circuit, while 60Hz is developed by a divide-by-6 circuit. The 30Hz signal is applied to the D input of flip-flop 1. The 60Hz output of the divide-by-6 circuit is applied to the tach shift MM.

The delay of the tach shift MM is determined by the time constant at pin 45. A delayed 60Hz pulse from the tach shift MM is applied to the $\overline{\text{CLOCK}}$ input of flip-flop 1 and through another 1.5H delay to the $\overline{\text{CLOCK}}$ input of flip-flop 2. A 30Hz signal at the D terminal of flip-flop 1 is supplied to the $\bar{Q}$ output and applied to the D input of flip-flop 2. A 30 Hz signal from flip-flop 1 is delayed via the tach shift MM. The tach shift delayed 30 Hz at the D input of flip-flop 2 is then supplied to the Q output after a 1.5H delay. The Q output of flip-flop 2 is coupled to pin 42 and used as the switching 30Hz signal.

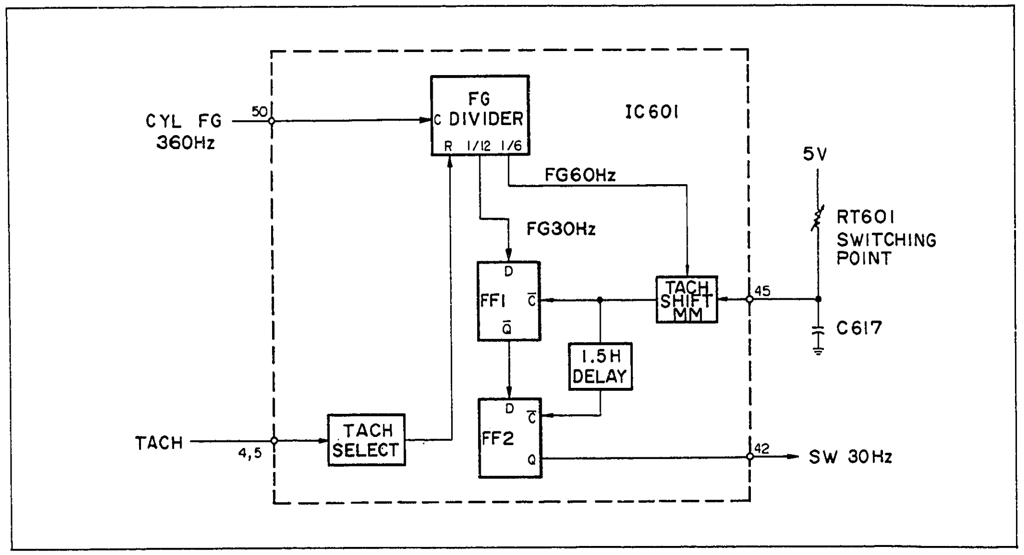


Fig. 3-12 Simplified Tach Detector/Switch 30Hz Generator Diagram

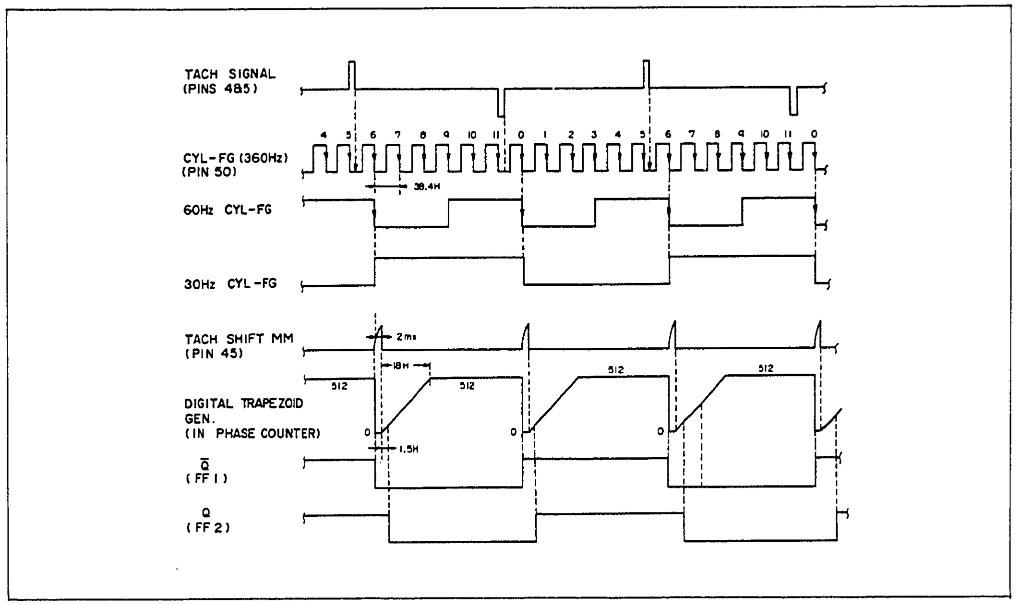


Fig. 3-13 Head Switching Signal Development

3-3-5 Tape speed selection/detection

The tape speed detection circuit determines the correct tape speed automatically during playback. The tape speed is selected manually during recording. Fig. 3-14 is a simplified diagram of the tape speed selection/detection circuit. The tape speed circuit in servo processing IC601, consists of three basic areas - playback speed detection, record speed selection and tape speed latch circuits. During playback, the speed detection portion of the IC receives two input signals -the capstan FG signal applied to pins 28 and 29 and the control track pulse applied to pins 59 and 60. The playback speed detection circuit divides the capstan FG frequency by the playback control track pulse frequency. The frequency of the capstan FG varies with the playback speed, (for example, it is 720Hz in SP, 360Hz in LP, and 240Hz in EP). The playback control track pulse frequency remains constant at 30 Hz. With the varying capstan FG frequency and constant playback control track pulse, the three tape speeds can be detected. This tape speed information is supplied to the playback section of a selector switch in IC601.

During recording, the internal selector switch is placed in the Record mode by supplying a "Mid" level signal to pin 54. Tape speed information is then supplied from the system control μP to the speed latch and generates the SP, LP or EP signals at pins 9, 8 and 7 respectively. These signals are used in the luminance/chroma, audio and system control circuits.

During recording, the tape speed is determined by the record speed selection circuit, which receives a speed selection voltage corresponding to the tape speed information from the digital/analog (D/A) converter Q909. During SP, pin 10 is grounded meeting the criteria of the SP speed select voltage of less than or equal to 0.4 volts. Record speed selection determines the record speed is SP and provides an appropriate signal to the speed latch circuit.

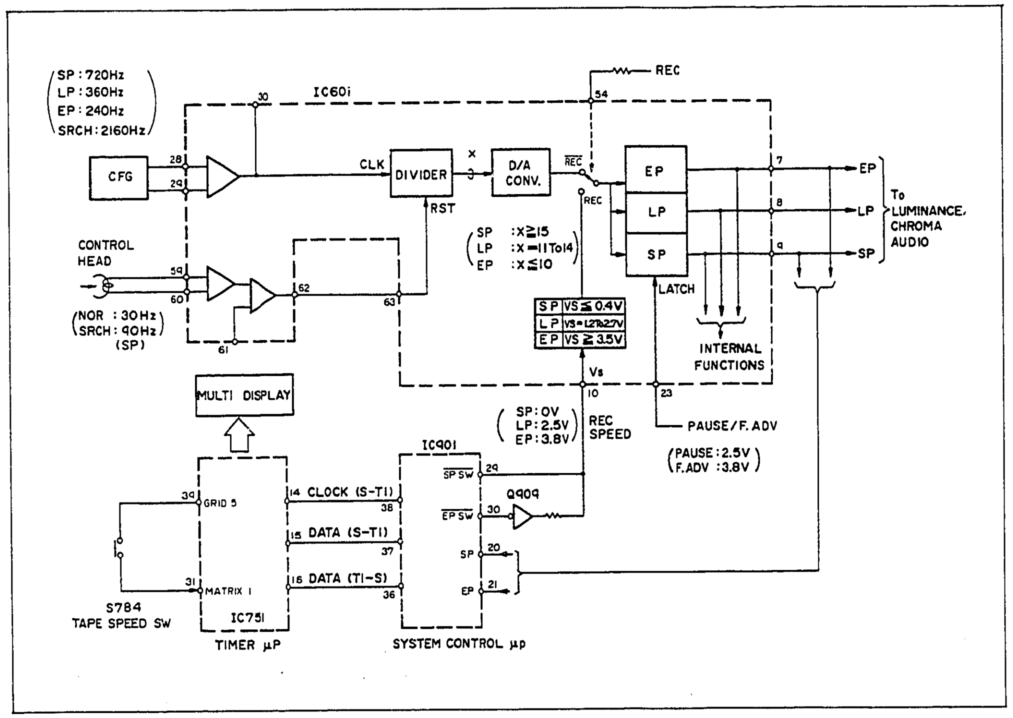

SP : 720Hz
LP : 360Hz
EP : 240Hz
SRCH : 2160Hz
IC601
30
REC
54
CFG
28
29
CLK
DIVIDER
X
D/A CONV.
REC
EP
LP
SP
7
8
9
EP
LP
SP
To LUMINANCE, CHROMA AUDIO
RST
SP :X≥15
LP :X=11To14
EP :X≤10
CONTROL HEAD
59
60
62
63
NOR : 30Hz
SRCH : 90Hz
(SP)
61
SP VS≤0.4V
LP VS=1.2To2.7V
EP VS≥3.5V
LATCH
INTERNAL FUNCTIONS
Vs
10
23
MULTI DISPLAY
SP:0V
LP:2.5V
EP:3.8V
REC SPEED
PAUSE/F.ADV
PAUSE:2.5V
F.ADV :3.8V
IC901
39
GRID 5
14 CLOCK (S-T1)
38
15 DATA (S-T1)
37
16 DATA (T1-S)
36
SP SW
29
Q909
EP SW
30
SP
20
EP
21
31
MATRIX 1
S784
TAPE SPEED SW
IC751
TIMER μP
SYSTEM CONTROL μp

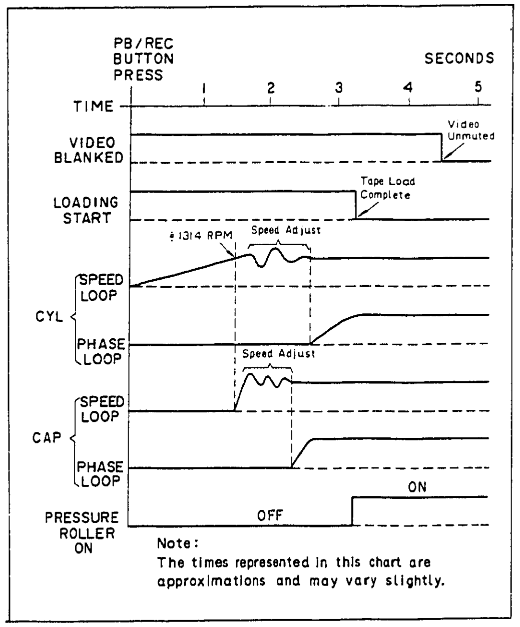
Fig. 3-14 Simplified Tape Speed Select Circuit Diagram

3-3-6 Start-up timing

Fig. 3-15 shows the timing chart for both playback and record operations. When either the PLAY or RECORD button is pressed, the loading motor immediately starts to load the tape and the video output is muted. At the same time, the cylinder speed loop is activated and the cylinder starts to rotate. Once the cylinder speed reaches approximately 1314 rpm, the capstan speed loop is turned on. At approximately the same time that the capstan speed loop is turned on, the cylinder speed loop adjusts the free-running cylinder speed. The capstan is brought up to speed very quickly and performs the same free-running speed adjustment.

Once the cylinder speed loop has stabilized, the cylinder phase loop is turned on. (The cylinder phase loop is turned on approximately 2.5 seconds after the start of the loading sequence while the capstan phase loop is turned on after approximately 2.25 seconds. After three seconds the pressure roller is activated and starts moving the tape. After approximately 3.5 seconds, both the cylinder and capstan speed and phase loops are stabilized. After approximately 4.5 seconds, the video is unblanked).

In earlier servo systems, the free-running speed was obtained by the use of potentiometers and the speed varied depending upon such factors as humidity, temperature, age of the machine and mechanical friction, etc. To eliminate these variables, the servo system calculates the amount of drive required to obtain the free-running speed. Such as a cylinder speed of 1800 rpm. At the start of playback or record operation, a new free-running speed calculation is performed.



Note:
The times represented in this chart are approximations and may vary slightly.

Fig. 3-15 Capstan and Cylinder Motor Startup Timing Chart

3-4 Assemble Control

3-4-1 General

When pause is instructed during recording and new audio/video signals are recorded on the previously recorded audio/video tracks, the assemble control minimizes noise when this section is played back.

Noise appears for the following reasons.

1. There is a non-recorded section between the end of the previously recorded section and the start of the newly recorded section.
2. The previously recorded video track and newly recorded track are not the same.
3. The cylinder speed and tape speed do not match at the start of newly recorded section.
4. Since the chroma level is high, the signal is not erased sufficiently.

To minimize noise, the following controls are performed.

1. Interrupts recording just after the pause mode is enetred and runs the tape in reverse for approx. 1.3 seconds (approx. 86 video tracks), then the compression between the capstan and pressure roller is released. After the pause mode is released, the pressure roller is compressed against the capstan and the tape runs. Recording is not done for approx. 0.9 seconds (approx. 54 video tracks: Assemble period) after the tape starts running and the control is performed to match the phases between the previouly recorded video track and the sync signal in the incoming video signal to be recorded.

These controls cause the following:

1. Since approx. 32 previously recorded video tracks are newly recorded (overlap recording), noise occurring due to cause 1 does not appear.
2. Since the phases of the previously recorded signal and incoming signal to be recorded are matched for approx. 0.9 seconds just after the pause mode is released, noise occurring due to causes 2 and 3 is reduced.

To reduce noise occurring due to cause 4, the recording current of the video signal to be recorded is increased for approx. 3 seconds (actually, 3 - 0.9 = 2.1 seconds) after the pause mode is released and the previously recorded chroma signal is erased sufficiently. Fig. 3-17 is a timing chart related to the amount of tape rewound and assemble control. The system control µP generates the loading/capstan motor control, pause, mute and current up signals for the assemble control. The ASBL signal is supplied from the servo circuit.

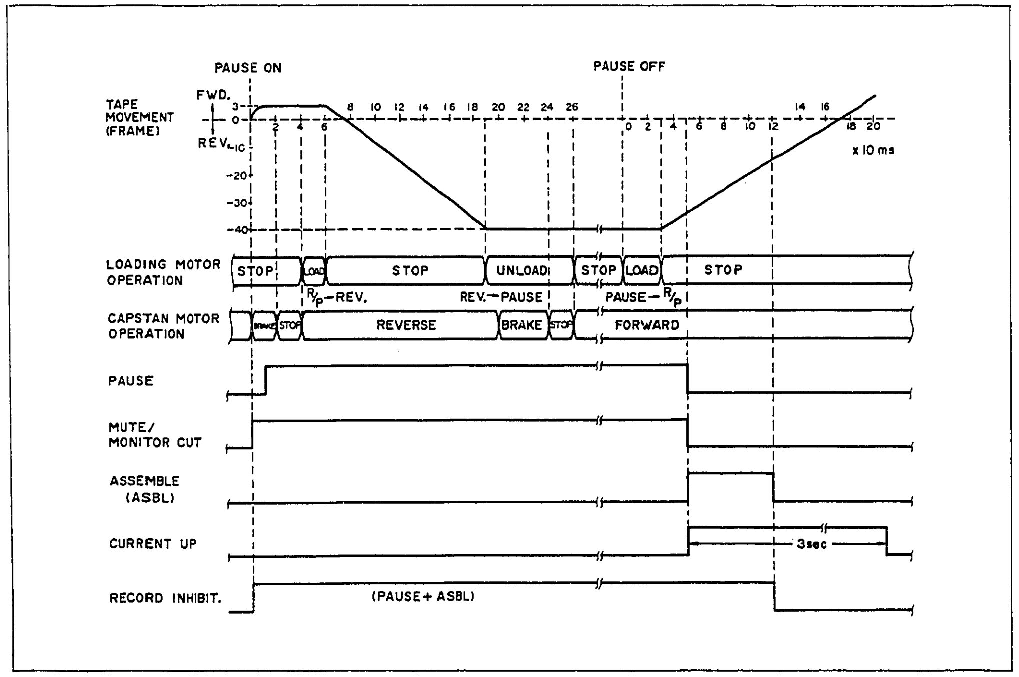


Fig. 3-17 Timing of Assemble Operation

- o The loading motor switches the mechanism state in the order, REC/PB - REVERSE - REC PAUSE - REC/PB as shown in Fig. 3-17.
- o The capstan motor runs the tape in reverse for approx. 1.3 seconds.
- o The "PAUSE" signal sets the servo circuit to the pause mode.
- o The "MUTE" signal inhibits the output of the REC 9V generator (Q416, Q407). It also inhibits recording of the control signal.
- o The "CURRENT UP" signal lowers the feedback amount of recording video current and increases the recording current level of the video signal to be recorded.
- o The "ASBL" signal has the same effects as the "MUTE" output.

3-4-2 Assemble operation in servo circuit

The servo circuit determines the assemble period and outputs the ASBL signal. In this period, the servo circuit plays back the previously recorded video tracks which are reversed just after the pause mode is entered, and synchronizes this with the phase (1/2 V. sync) of incoming video signal. Fig. 3-19 is a simplified diagram of the assemble control circuit and Fig. 3-20 is a timing chart of the assemble operation. The assemble period is determined by the ASBL MM in the main servo processing IC601. The ASBL MM is triggered when both voltages of "REC" applied to pin 54 and "PAUSE" to pin 23 reach 2.5V from 0V and generates a pulse with the period of approx. 0.7 seconds determined by the time constant (C654, R672) at pin 51. This pulse is used for the internal functioning of IC601 and is also derived from pin 55.

The control to synchronize the previously recorded video track with the phase of incoming video signal is performed in the main servo processing IC601. Fig. 3-18 shows an overview of cylinder and capstan phase control in the assemble mode. In the assemble mode, the video heads are phase-locked to the SYNC 30 signal in the incoming video signal via the TACH signal. The video track is phase locked to the REF 30 signal via the CTL 30 (control pulse) signal. Since the video

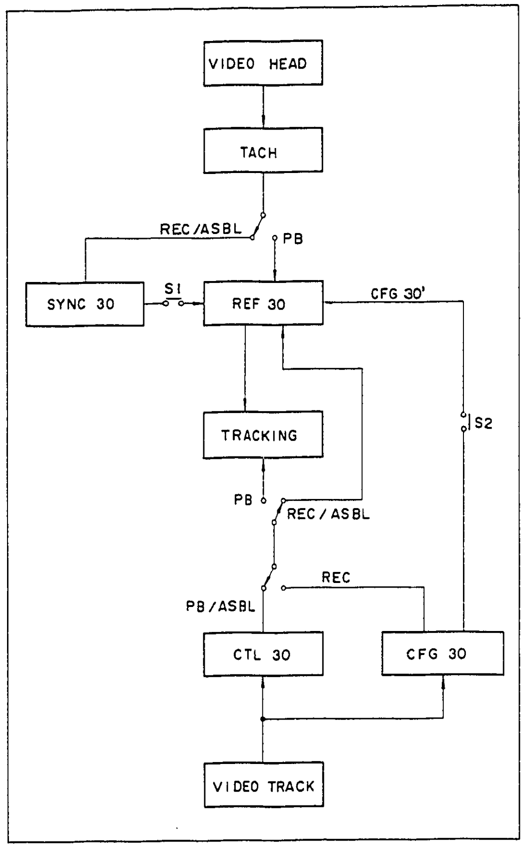


Fig. 3-18 Cylinder/Capstan Phase Control in Record Pause Mode

track must be phase locked to the video head, it is necessary to synchronize the phases of both reference signals (REF 30 and SYNC 30) for the video track and video head. To synchronize these phases, the phase of REF 30 signal is synchronized to the phase of SYNC signal and a preset value which sets the duty cycle of REF 30 signal to 93% ((525H-36H)/525H) is preset to the REF 30 counter generating the REF 30 signal. This causes the same effect as delaying the REF signal by an optimum amount with the tracking control during playback. When the assemble mode is released, the comparison signal of the capstan phase control loop is changed from CTL 30 to CFG 30, not changing the comparison signal of the cylinder phase control loop (Fig. 19). The preset command by the SYNC signal to the REF 30 counter via S1 is stopped. The phase of the CFG 30 signal is not synchronized with that of the CTL 30 signal, however, since the CTL 30 signal is phase-locked to the REF 30 signal in the assemble mode, the constant phase relationship is maintained between both signals. To minimize phase error when switching the comparison signal, one cycle of the CFG 30' signal the phase of which advances from the CFG 30 signal by approx. 36H is supplied to the REF 30 counter to reset it just after the assemble mode is released. The REF 30 counter generates a digital trapezoid wave for capstan phase control just after being reset, and when approx. 36H is reached, the data near the center slope of the digital trapezoid wave is sampled by the CFG 30 signal. Since the sampling data before and after the assemble mode is released are approximately aligned, a large phase error does not occur.

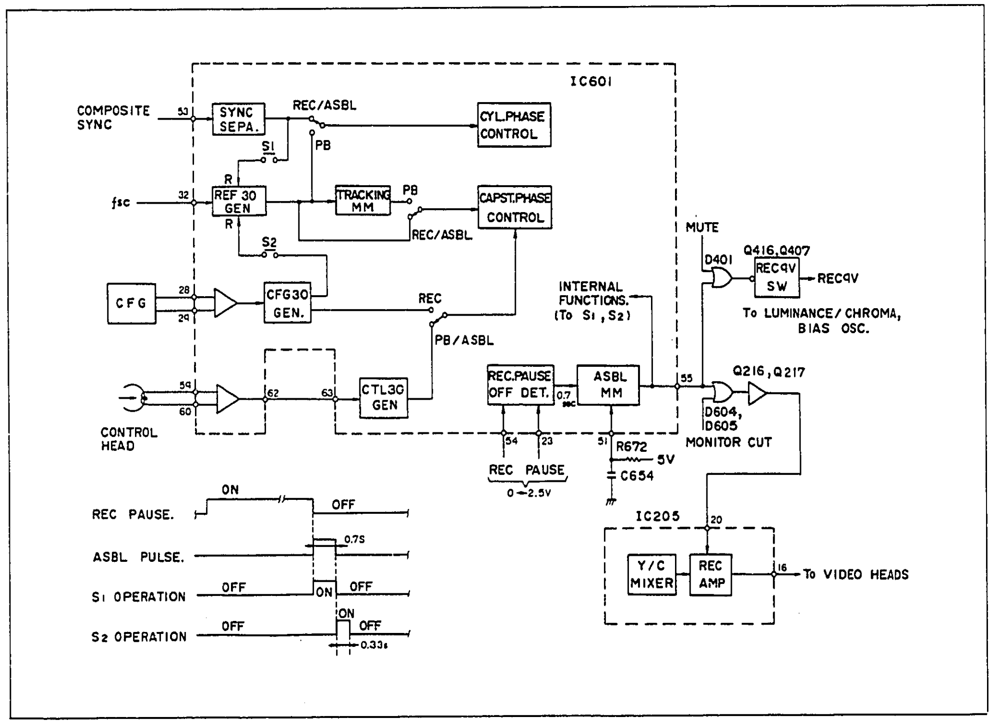

IC601
COMPOSITE SYNC
53
SYNC SEPA.
REC/ASBL
CYL.PHASE CONTROL
S1
PB
R
fsc
32
REF 30 GEN
TRACKING MM
PB
CAPST.PHASE CONTROL
REC/ASBL
S2
CFG
28
29
CFG30 GEN.
REC
PB/ASBL
59
60
62
63
CTL30 GEN
CONTROL HEAD
REC.PAUSE OFF DET.
0.7 sec
ASBL MM
INTERNAL FUNCTIONS. (To S1, S2)
55
54
23
51
REC PAUSE
0→2.5V
R672
5V
C654
MUTE
D401
Q416,Q407
REC9V SW
REC9V
To LUMINANCE/CHROMA, BIAS OSC.
Q216,Q217
D604, D605
MONITOR CUT
IC205
20
Y/C MIXER
REC AMP
16
To VIDEO HEADS
REC PAUSE.
ON
OFF
ASBL PULSE.
0.7S
S1 OPERATION
OFF
ON
OFF
S2 OPERATION
OFF
ON
OFF
0.33s

Fig. 3-19 Simplified Assemble Control Circuit Diagram

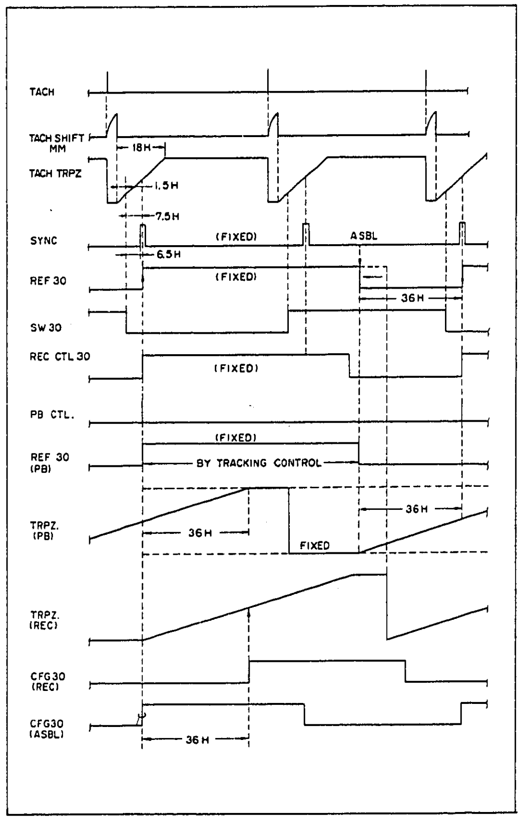

TACH
TACH SHIFT MM
18H
TACH TRPZ
1.5H
7.5H
SYNC
(FIXED)
ASBL
6.5H
REF 30
(FIXED)
36H
SW 30
REC CTL 30
(FIXED)
PB CTL.
(FIXED)
REF 30 (PB)
BY TRACKING CONTROL
36H
TRPZ. (PB)
36H
FIXED
TRPZ. (REC)
CFG30 (REC)
CFG30 (ASBL)
36H

Fig. 3-20 Timing of Servo Circuit During Assemble Mode

3-5 Still/(Frame Advance/Slow) Operations (for VT-1310A/1305A)

3-5-1 General

The VT-1310A/1305A have field still play, frame advance and slow motion play functions. When the PAUSE button is pressed during play, the VTR enters the field still mode. The unit stops tape at one CH-2 video track aligning it with the scanning period of the video heads and plays it back. When the F. ADV button is pressed in the still mode, the VTR enters the frame advance mode and pulse-drives the motor to advance the frames while this button is held down. When the button is released, the VTR enters the still mode. When the SLOW button is pressed during play, the VTR enters slow motion mode and advances frames at approx. 1/10 the normal play speed automatically. When the PLAY button is pressed in the slow motion mode, this mode is released. The slow motion play is the same as when the F. ADV button is held down but different in setting and release methods. It is necessary to locate a CH-2 video track within the scanning period of the video heads and to minimize noise in the still, frame advance and slow motion modes. To do this control, the video track (tape) is stopped just before an optimum stop position, then the position in which the PB horizontal sync signal starts to be missing (this is assumed to be the tape stop position) and the optimum stop position are compared and the motor are pulse-driven until both positions are aligned. This optimum stop position is set to each edge of the head switching (SW30) signal.

3-5-2 Circuit composition and operations

Fig. 3-21 is a simplified diagram of the still/frame advance/slow control circuit. This circuit consists of the brake pulse generator, stop position error detector, fine advance pulse generator, driving timer, horizontal jitter canceler, capstan motor driver, still head selector, speed selector, speed up/down pulse generator and artificial sync generator. The following describes the main controls of these circuits.

Brake Pulse Generator:

Generates a brake pulse to stop the CH-2 video track (tape) at the optimum stop position instantaneously when pause is commanded. This circuit is triggered by the "PAUSE" mode setting signal which is synchronized with the phase of head switching signal by S-μP and generates a brake pulse whose phase (position) and width are set to optimum values and applies it to the speed/direction control inputs of the capstan motor driver. The capstan motor driver enters the reverse mode while this pulse is being applied. However, since the pulse width is short, the capstan motor stops just before it turns in reverse. This has the same effect as when braking is applied. The braking force is determined by the motor drive voltage of capstan servo in this braking period. After the braking period is passed, since the capstan motor driver enetrs the play mode, the brake pulse generator sets the capstan motor drive voltage to 0V and holds the capstan motor at the stop state.

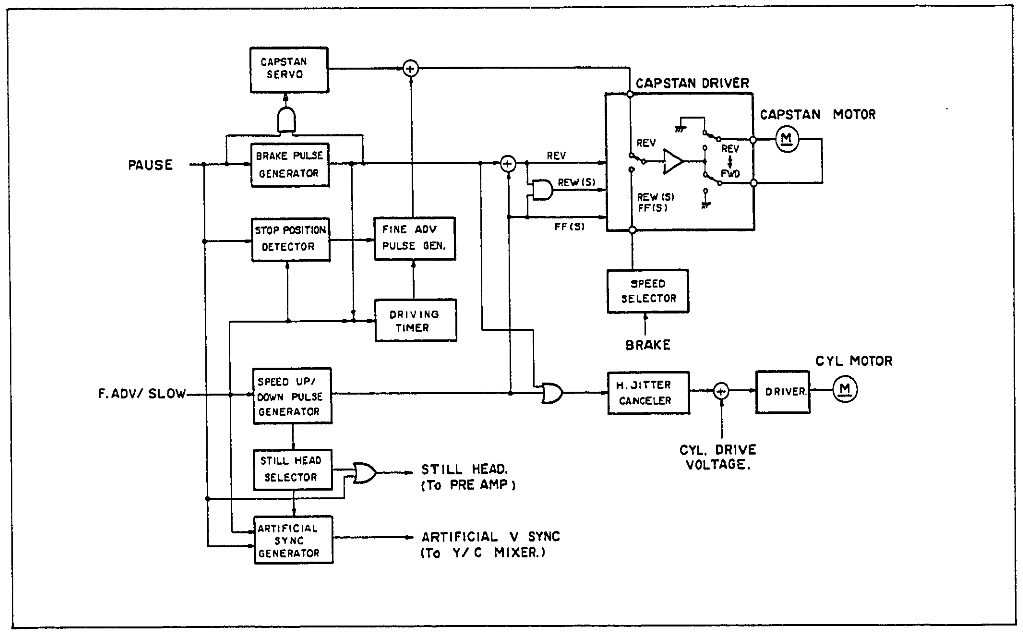


Fig. 3-21 Simplified Still/F.ADV/Slow Control Block Diagram

Stop Position Error Detector:

As soon as the tape is stopped by the brake pulse or speed down pulse in the still, frame advance and slow modes, this circuit detects the phase difference between the stopped video track (tape) position and optimum stop position. The video track stop position is determined by whether the PB horizontal sync signal starts to be missing or not. The optimum stop position is set to each edge of the head switching (SW30) signal. This detector output is applied to the fine advance pulse generator to trigger it.

Fine Advance Pulse Generator:

Generates a drive pulse to pulse-drive the capstan motor until the position error between the video track stop position and optimum stop position is eliminated. This output is applied to the REC/PB speed control input of the capstan motor driver. The capstan motor driver is set to the REC/PB mode by S-μP in the still mode, however, since the REC/PB speed control input is set to 0V, the tape is stopped. When the fine advance pulse is applied to the REC/PB speed control input, the capstan motor starts and advances the tape.

Driving Timer:

Limits the tape stop position fine advance period to a maximum of 4 seconds. Since a tape recorded by a VTR with 30 μm-width video heads in the SP mode has a non-recorded portion of approx. 30 μm width, the noise becomes wider than the stop position detection inhibit period of the stop position error detector and the stop position error output would always be output. This causes the tape fine advance operation not to be completed. To prevent this, the driving timer limits the fine advance period to a maximum of 4 seconds. This output is applied to the frame advance pulse generator to make it active.

Horizontal Jitter Canceler:

Cancels horizontal jitter occurring because the tape is tightly wound onto the upper cylinder when braking is applied to the capstan motor in the still, frame advance or slow mode. This circuit is triggered by both outputs of the brake pulse generator and speed up/down pulse generator and generates a cylinder speed correction pulse which has appropriate width and output. This pulse is added to the cylinder drive voltage to correct the cylinder speed.

Capstan Motor Driver:

Pulse-drives the capstan motor to stop or accelerate the tape. The pulse driving period is determined by both outputs of the brake pulse generator and speed up/down pulse generator. The capstan speed during the pulse-drive period is determined by the voltage selected by the capstan servo and speed selector. See the explanation given in the brake pulse generator and speed selector for details.

Still Head Selector:

Selects the head exclusively for still play which has the same azimuth as the CH-2 video head when still-playing a CH-2 video track for field still play. This output is applied to the head switch control input of the video preamplifier circuit and artificial sync generator. The video preamplifier circuit selects the still video head and the artificial generator shifts the phase of artificial sync signal to correct it because the still video head is installed 2H before the CH-1 video head.

Speed Selector:

Selects the voltage for speed up or down in the frame advance and slow modes and the start speed setting voltage during fast forward according to the operation mode, and then applies it to the capstan motor. See the speed up/down pulse generator for deteils.

Speed Up/Down Pulse Generator:

Generates a speed up/down signal which is necessary to advance or stop the video track (tape) instantaneously in the frame advance and slow modes. The generator becomes active when receiving the "F.ADV" mode setting signal (Hi) applied from S-µP and generates the speed up or down signal every 450 ms. This output is applied to the horizontal jitter canceler and capstan motor driver. The horizontal jitter canceler is triggered by the speed down signal and generates a cylinder speed correction pulse. The speed up/down signal supplied to the capstan motor driver is converted to code "FF(S)" during the speed up period and to code "REW(S)" during the down period and is applied to the speed/direction control input. The rotation direction of the capstan motor is switched to forward with code "FF(S)" and to reverse with code "REW(S)", and the speed is determined by the capstan speed control voltage selected by the speed selector.

Artificial Sync Generator:

Artificially generates the vertical sync signal which is missing in the still play mode. This circuit becomes active when receiving the "STILL", "F.ADV" and "SEARCH" mode setting signals from S-µP, and the phase of artificial sync signal in each field is determined so the horizontal scanning frequency becomes 15.734kHz. This output is applied to the Y/C mixer in the luminance/chroma circuit.

4. AUDIO/VIDEO PROCESSING

4-1. General

Fig. 4-1 is a simplified diagram of the audio/video processing loop showing the route from the inputs to outputs and the relation between each µP. The audio/video processing circuit consists of the tuner/IF, input selector, audio/video processor, RF converter and output selector.

Tuner/IF:

Tunes the one of 107 programs receivable in the VHF and UHF bands using the voltage synthesis tuning system and supplies the tuned audio and video signals to the input selector. The controls necessary for tuning (4-band switching, tuning voltage control, defeat control, 80-channel list, auto frequency control) are performed by the tuning µP (TU-µP).

Input Selector:

Selects the audio and video signals applied to the audio/video processing circuit, commanded by the operator, from those supplied by the tuner/IF and line input jack, and supplies them to the audio/video processor. This switching is controlled by the timer µP (T-µP).

Audio/Video Processor:

Signal processing is different between the audio and video processor loops. The following tables show the main processing details of each processor loop.

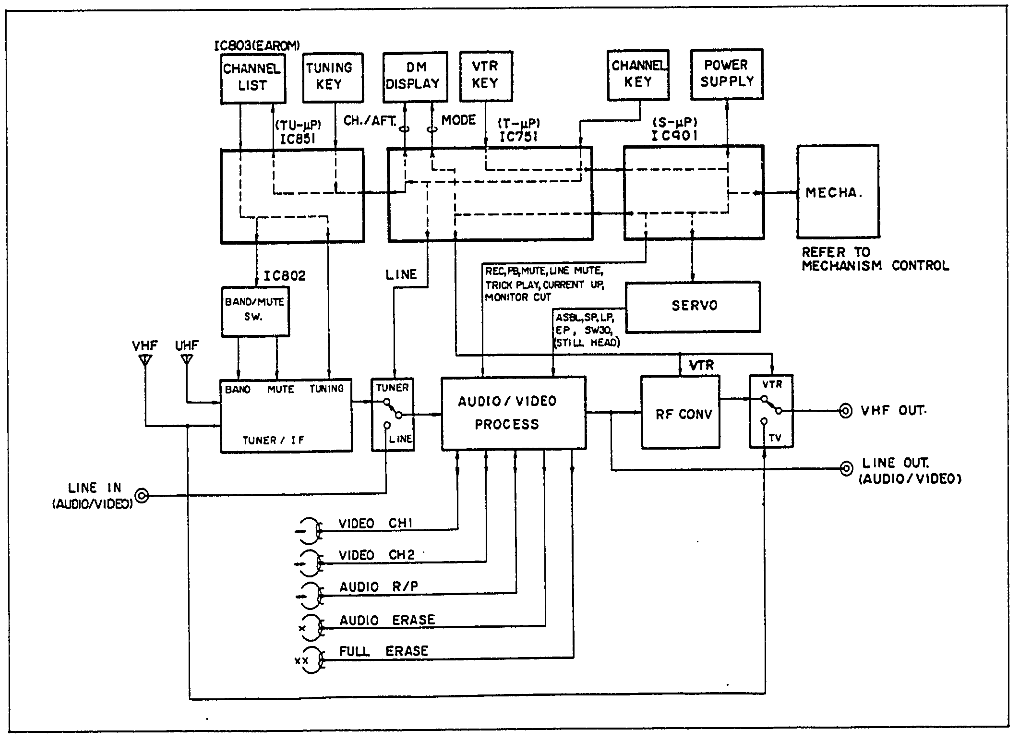

IC803(EAROM)
CHANNEL LIST
TUNING KEY
DM DISPLAY
VTR KEY
CHANNEL KEY
POWER SUPPLY
(TU-µP) IC851
CH./AFT.
MODE
(T-µP) IC751
(S-µP) IC901
MECHA.
REFER TO MECHANISM CONTROL
IC802
BAND/MUTE SW.
LINE
REC,PB,MUTE,LINE MUTE, TRICK PLAY, CURRENT UP, MONITOR CUT
SERVO
ASBL,SP,LP, EP, SW30, (STILL HEAD)
VTR
VHF
UHF
BAND
MUTE
TUNING
TUNER / IF
TUNER
LINE
AUDIO / VIDEO PROCESS
RF CONV
VTR
TV
VHF OUT.
LINE OUT. (AUDIO/VIDEO)
LINE IN (AUDIO/VIDEO)
VIDEO CH1
VIDEO CH2
AUDIO R/P
AUDIO ERASE
FULL ERASE

Fig. 4-1 AUDIO/VIDEO Control Block Diagram

The controls (mode change, muting, monitor cut, etc.) necessary for the above signal processing are performed by the system control μP (S-μP) and servo circuit.

RF Converter: Converts the monitor or playback audio and video signals to the RF signals in the exclusive VHF channel 3 or 4 band and supplies the RF-converted output to the output selector. The power supply for the RF converter is controlled by T-μP and becomes active when the VTR/TV switch is set to "VTR".

Output Selector: Selects the output from the VHF antenna or RF converter as a VHF output. This selection is controlled by T-μP in the same way as for the RF converter. When the VTR/TV switch is set to "VTR", the RF converter output is selected, and when the switch is set to "TV", the VHF antenna output is selected.

Audio Processor

Mode	Processing Details
REC	1. Adjusts the input signal to an optimum input level for the processing circuit. 2. Frequency-compensates the signal matching the tape speed to make the overall frequency characteristics flat in combination with the playback loop. 3. Adjusts the signal to an optimum recording current to be supplied to the audio record/playback head. 4. Amplifies the signal until it becomes the optimum monitor output and supplies it to the line output jack and RF converter.
PLAY	1. Amplifies the playback signal until it becomes an optimum level for the processing circuit. 2. Frequency-compensates the signal matching the tape speed to make the overall frequency character-istics flat. 3. Amplifies the signal until it becomes the optimum monitor output and supplies it to the line output and RF converter.

Video Processor

Mode	Signal	Processing Details
REC	LUMINANCE	The luminance signal is separated and the processing below is performed. 1. Adjusts the input signal to an optimum input level for the processing circuit. 2. Frequency-compensates the signal matching the tape speed in combination with the playback loop. 3. FM-modulates the signal to settle it in the specified frequency range. 4. Superimposes the down-converted chroma signal on the signal and adjusts it to an optimum recording current to supply it to the video heads. 5. Amplifies the signal until it becomes the optimum monitor output and supplies it to the line output and RF converter.
	CHROMA	The chrominance signal is separated and the processing below is performed. 1. Adjusts the input chroma signal to an optimum input level for the processing circuit. 2. Preemphasizes the chroma burst level by 6 dB in the SP and EP tape speeds. 3. Shifts the phase by 90° for every 1H and down-converts the chroma subcarrier frequency to 629kHz from 3.58MHz. 4. Adjusts the signal to an optimum recording current and superimposes the signal on the luminance signal. 5. Amplifies it until it becomes the optimum monitor output and supplies it to the line output and RF converter.
PLAY	LUMINANCE	1. Amplifies the playback signal to an optimum lever for the circuit. 2. Selects the preamplifier output and compensates the dropout to produce a continuous FM playback signal. 3. FM-demodulates the FM playback signal to return it to a video signal. 4. Frequency-compensates the signal matching the tape speed to make the overall frequency characteristics flat. 5. Amplifies the signal until it becomes the optimum monitor output to supply it to the line output and RF converter.
	CHROMA	The chrominance signal is separated from the FM playback signal and the processing below is performed. 1. Shifts the phase by 90° for every 1H and converts the chroma subcarrier frequency correctly to 3.58MHz from 629kHz to return it to the original frequency. 2. Amplifies the signal to an optimum level for the processing circuit. 3. Amplifies the chroma burst level by -6 dB to the original level in the SP and EP modes. 4. Eliminates the chroma crosstalk components.

4-2. Detailed Circuit Operations

4-2-1 Tuner/IF

The VT-1100A/1105A generate a digital signal representing the tuning voltage which is stored in an EAROM (Electrically Alterable Read Only Memory) instead of presetting the tuning voltage by a potentiometer. In the same way, the band and AFC information are converted to a digital code which is stored in the EAROM instetad of using mechanical switches.

Fig. 4-2 is a block diagram of the tuning system, TU-µP acts as the central controller in the voltage synthesis tuning system. The front panel tuning controls are input via the matrix switch to TU-µP together with the output of the infrared receiver. The EAROM acts as the storage medium for the digital code that represents the tuning voltage, the band, and AFC information. A 3-bit unidirectional bus from TU-µP is used to transmit address and command data to the EAROM. A single bidirectional bus is utilized to transfer the tuning data itself into and out of the EAROM. T-µP data is also input to TU-µP in order to accommodate timer recording functions where a preselected channel has been programmed into the VTR.

TU-µP outputs a muting signal coupled through switch circuit to the tuner/IF in order to blank video and audio during channel selection.

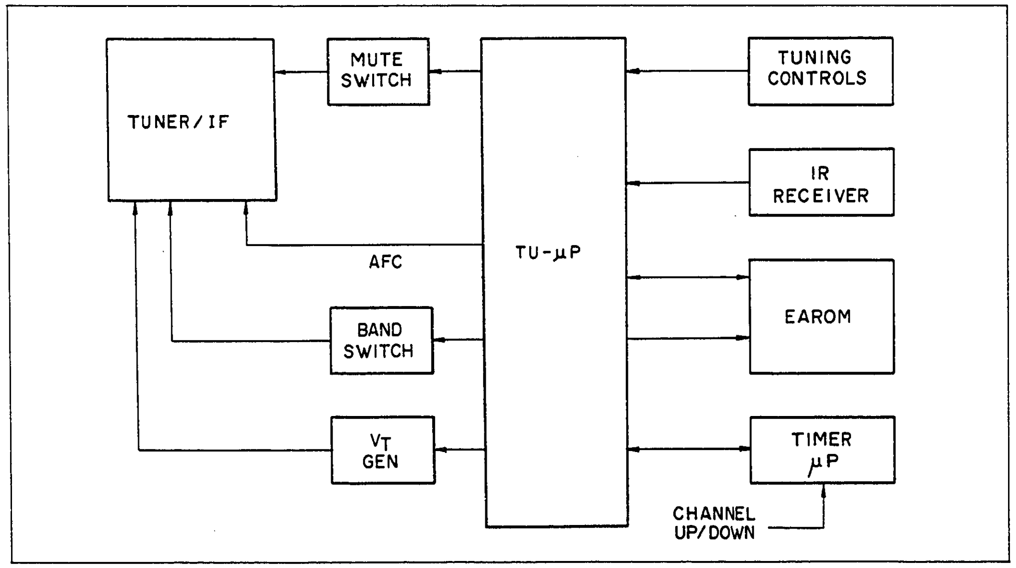


Fig. 4-2 Voltage Synthesis (VS) Tuning System Block Diagram

As shown in the simplified block diagram, TU-µP generates the band switching signal for the tuner and also generates the actual tuning voltage via the VT generator.

Tuning Voltage Generator

Fig. 4-3 is a simplified diagram of the tuning voltage generator circuit.
The tuning voltage output from pin 20 of TU-µP is a pulse width modulated (PWM) signal generated in TU-µP by utilizing the 13 bits of tuning data from the EAROM. The tuning data is then applied to a 7.8kHz PWM generator within the IC along with a 122Hz oscillator signal. The PWM output representing the DC voltage required by the tuner is applied to the base of Q802. The collector of Q802 is coupled directly to a lowpass filter allowing a DC voltage to be generated at pin 14 of PG802.

When TU-µP is tuning to higher frequencies, the "on" time of the pulse width modulated signal output from pin 20 becomes narrower, allowing more of the 33V DC supply to be supplied through the lowpass filter (LPF) to pin 14. This causes the DC voltage that is applied to the demodulator circuit board to increase. Conversely, when TU-µP is tuning to lower frequencies, the "on" time of the PWM signal output from pin 20 becomes wider, causing Q802 to be "on" longer and the voltage at pin 14 to decrease.

Fig. 4-4 shows the tuning voltage gradient when the tuning up button is pressed which is very shallow for approximately 1.5 seconds (fine tuning). After 1.5 seconds, the tuning voltage starts rising faster (coarse tuning). The band selected determines the per step voltage that is output from TU-µP.

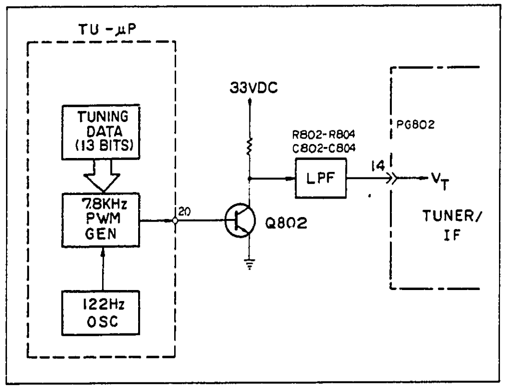


Fig. 4-3 Tuning Voltage (VT) Generator Circuit

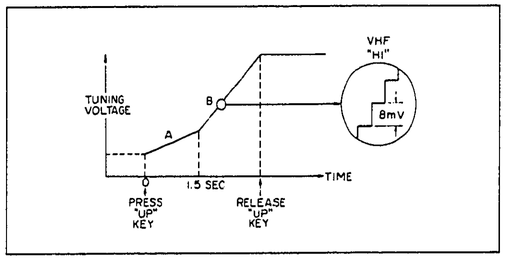


Fig. 4-4 Tuning Voltage Preamp

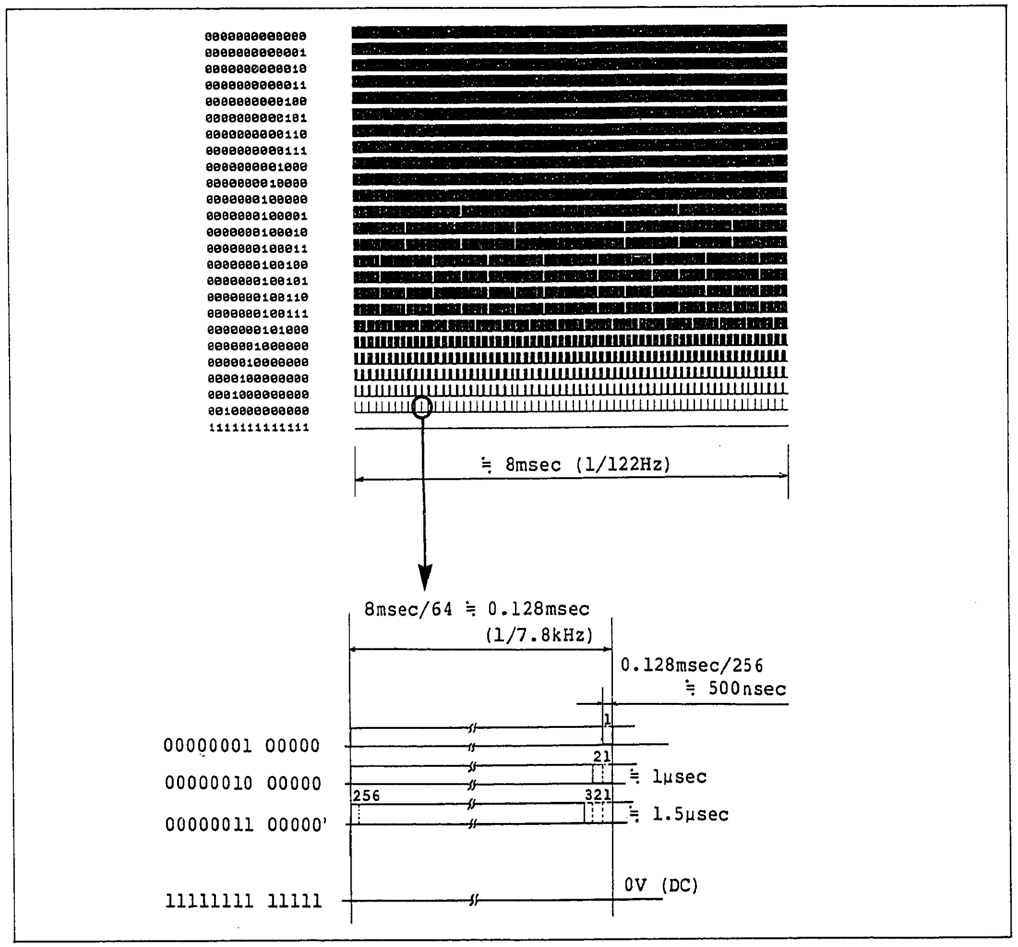
Table 4-1 shows the voltage synthesis tuning speed chart. When the tuner is searching the VHF "Lo" band, the PWM output of TU-µP changes approximately 15 times per second during the fine tuning operation. The PWM output changes 133 times per second during a coarse tune operation (approximately 12 mV per step). During VHF "Hi" and "Midband" operations, the tuner steps at approximately 10 times per second during fine tuning and 88 times per second during coarse tuning. This relates to approximately an 8mV change per step in the DC output of the lowpass filter.

Table 4-1 Voltage Synthesis Tuning Speed Chart

BAND	FING TUNING SPEED FIRST 1.5 SEC	COARSE TUNING SPEED	VOLTAGE PER STEP
VHF "Lo"	15/SEC*	133/SEC*	12mV
VHF "HI" and "MID"	10/SEC	88/SEC	8mV
SUPER	10/SEC	88/SEC	8mV
UHF	12/SEC	100/SEC	4mV

* STEPS PER SECOND

PWM GEN. OUTPUT (IC851 PIN 20)


0000000000000
0000000000001
0000000000010
0000000000011
0000000000100
0000000000101
0000000000110
0000000000111
0000000001000
0000000010000
0000000100000
0000000100001
0000000100010
0000000100011
0000000100100
0000000100101
0000000100110
0000000100111
0000000101000
0000001000000
0000010000000
0000100000000
0001000000000
0010000000000
1111111111111
≒ 8msec (1/122Hz)
8msec/64 ≒ 0.128msec
(1/7.8kHz)
0.128msec/256
≒ 500nsec
00000001 00000
00000010 00000
00000011 00000'
11111111 11111
1
21
321
256
≒ 1µsec
≒ 1.5µsec
0V (DC)

Tuning Microprocessor-to-EAROM Communications

Fig. 4-5 shows the connections between TU-µP and EAROM. As mentioned before, TU-µP is responsible for the recovery of tuning information from the EAROM and also for writing information to the EAROM. To accomplish this, TU-µP outputs command data (3-bits) via pins 3, 2 and 1. These are referred to as command 1, 2 and 3 and are applied to pins 7, 8 and 9 of the EAROM, IC803. As shown in Table 4-2. Mode Command Chart, the commands output over the 3-bit (parallel) data bus consist of such commands as ERASE, ADDRESS SET, READ, DATA LOAD, WRITE, DATA STORE, etc. These commands instruct the EAROM as to whether information is being written to it (stored) or read from it (output) TU-µP over the data in/out (I/O) line. A clock signal is also output from pin 4 of TU-µP and input, to pin 6 of IC803 in order to synchronize communications between TU-µP and the EAROM. The data I/O line between pin 12 of IC803 and pin 13 of TU-µP first transmits the address of the data that is either being written to or read from the EAROM and then transmits the data itself.

A good example of normal operation is in the mode where a tuning voltage has already been input to the EAROM and the operator selects the channel. TU-µP first outputs the proper command on the command bus and then transfers the address of the data on the data I/O line.

This is the actual address within the EAROM where the tuning data is located. TU-µP then transmits the necessary code over the command bus that instructs the EAROM to transmit the tuning data (13 bits) back to the TU-µP via the data I/O port. Fig. 4-6 and 4-7 show transfer timing to and from EAROM.

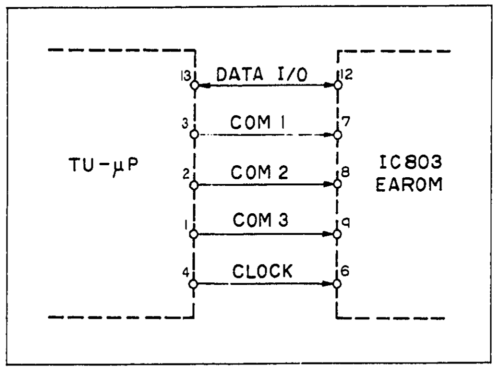
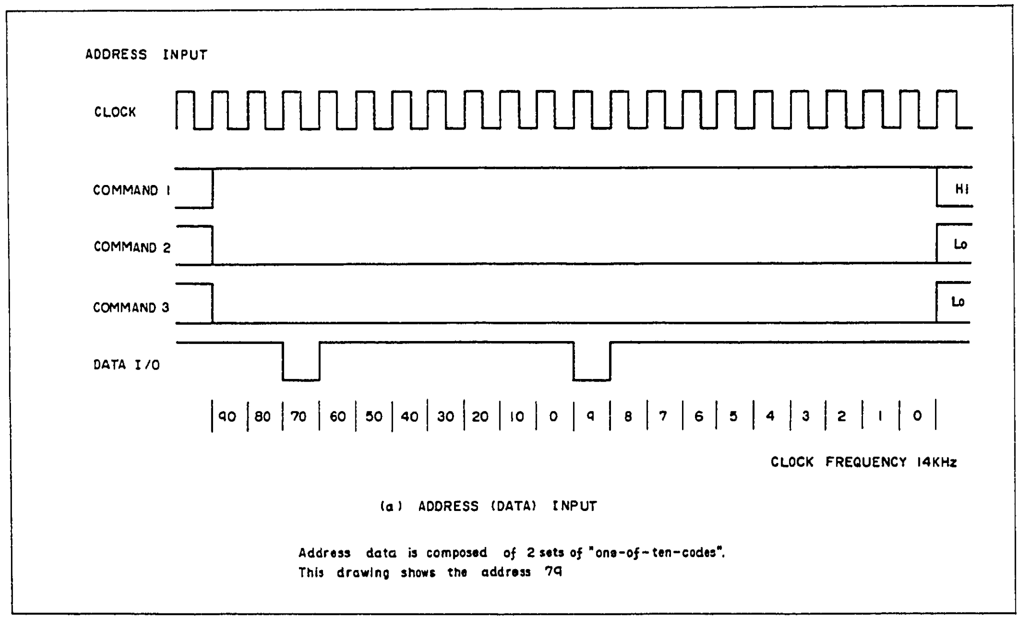

TU-µP
13
DATA I/O
12
3
COM 1
7
2
COM 2
8
1
COM 3
9
4
CLOCK
6
IC803
EAROM

Fig. 4-5 Tuning µP EAROM Communication Bus

Table 4-2 Tuning µP to EAROM Mode Commands

COMMAND			FUNCTION
1	2	3	
H	H	H	STANDBY
H	H	L	NOT USED
H	L	H	ERASE
H	L	L	ADDRESS SET
L	H	H	READ
L	H	L	DATA LOAD
L	L	H	WRITE
L	L	L	DATA STORE


ADDRESS INPUT
CLOCK
COMMAND 1
COMMAND 2
COMMAND 3
DATA I/O
HI
Lo
Lo
90 | 80 | 70 | 60 | 50 | 40 | 30 | 20 | 10 | 0 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0
CLOCK FREQUENCY 14KHz

(a) ADDRESS (DATA) INPUT

Address data is composed of 2 sets of "one-of-ten-codes".
This drawing shows the address 79

Fig. 4-6 Transfer Timing to/from EAROM

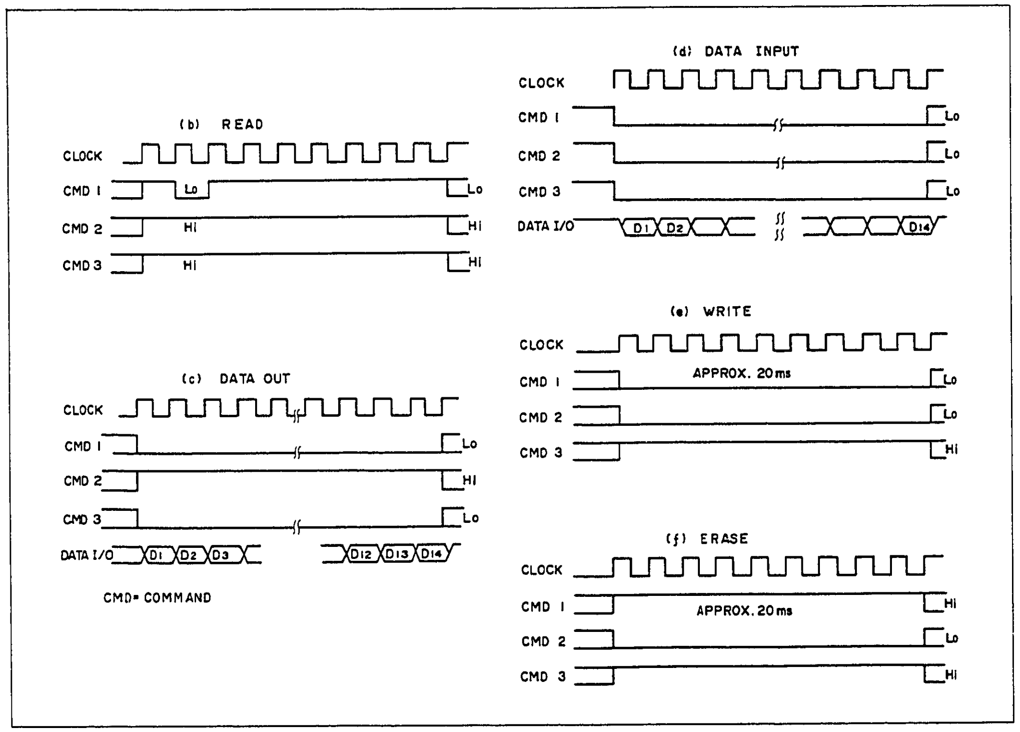

(b) READ
CLOCK
CMD 1
CMD 2
CMD 3
Lo
Lo
HI
HI
HI
HI
(c) DATA OUT
CLOCK
CMD 1
CMD 2
CMD 3
DATA I/O
D1 D2 D3
D12 D13 D14
Lo
HI
Lo
CMD= COMMAND
(d) DATA INPUT
CLOCK
CMD 1
CMD 2
CMD 3
DATA I/O
D1 D2
D14
Lo
Lo
Lo
(e) WRITE
CLOCK
CMD 1
CMD 2
CMD 3
APPROX. 20ms
Lo
Lo
HI
(f) ERASE
CLOCK
CMD 1
CMD 2
CMD 3
APPROX. 20ms
HI
Lo
HI

Fig. 4-7 Data Transfer Timing to/from EAROM

EAROM (Electrically Alterable Read Only Memory)

Fig. 4-8 shows a simplified block diagram of the EAROM. The tuning data information and the address of that information is applied to pin 12 of IC803 and fed into a buffer within the IC. The output of the buffer is applied to the appropriate register (data register or address register). The command information is input to the mode control circuit in IC803. The mode control circuit decodes the signal and applies the proper instructions to the memory section of the IC which has a READ, WRITE and ERASE configuration. As shown in the block diagram, the clock signal from TU-µP is also input to the mode control circuit in order to synchronize the read, write and erase functions. During the mode when the EAROM is being accessed for tuning data information, tuning data is output from the internal memory of the IC, first through the data register, then through the buffer, leaving the IC at pin 12 where it is then transmitted to the TU-µP via pin 13.

The total memory capacity of IC803 is 14 bits x 100 words, which allows a total of 80 channels to be stored in memory. The block diagram of the EAROM also shows two sections (or blocks) of address locations in the IC. These consist of address locations 0 through 79 and 80 through 99 - making up the 100 locations or words. The reason the memory is divided into two separate areas is described in the next section.

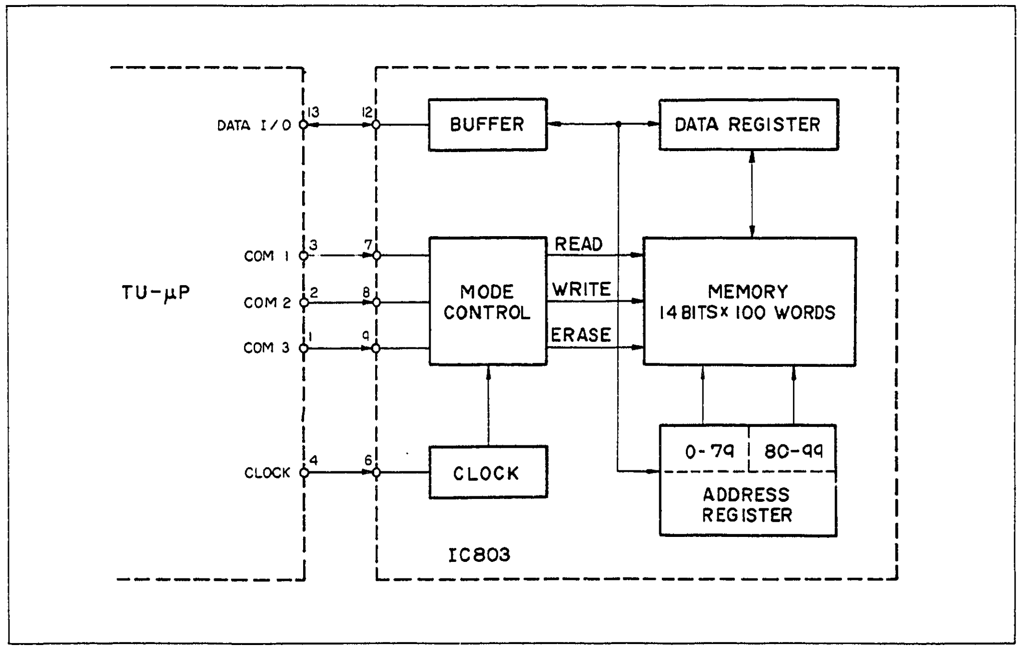

TU-µP
DATA I/O
COM 1
COM 2
COM 3
CLOCK
13
12
3
7
2
8
1
9
4
6
BUFFER
DATA REGISTER
MODE CONTROL
READ
WRITE
ERASE
MEMORY 14 BITS x 100 WORDS
CLOCK
0-79
80-99
ADDRESS REGISTER
IC803

Fig. 4-8 Simplified EAROM Block Diagram

Fig. 4-9 is an EAROM memory map. Although there are 100 words in the EAROM, data only 80 channels can be stored, this is because band data and AFC data have also to be stored. At the top of the chart, for example, address 0 is designated as channel 1. The storage capacity of each address location is actually 14 bits, but only 13 bits of this is used for the tuning data itself and the last bit of the word is used to store the skip data. The skip data bit is required to allow the operator the option of programming out a channel he no longer wishes the tuner to stop at.

Once a channel (digital tuning data) has been stored in an address location, it cannot be erased except by writing over it with new channel information. For this reason, a skip command is needed in order to reprogram the tuner when the operator wishes to skip a channel that has been stored in the memory.

As the chart shows, there are 80 memory locations, 0 through 79, for tuning data. Memory locations 80 through 99 are allocated for the band data and AFC information. The exploded view of address location 80 shows the 14-bit word broken into four sections with 3 bits in each section (totaling 12 bits). The first 2 bits of locations 80 through 99 are not used. For example, when channel 41 is selected, the tuning data is first output from the EAROM. TU-μP automatically selects the proper 3 bits at address 80 that corresponds to channel 41. Again, this consists of 3 bits of information, 2 bits of which are the band where the channel is located and one whether the AFC is on or off.

Fig. 4-10(a) shows the data store sequence and Fig. 4-10(b) shows the data read sequence. A data store sequence occurs during initial setup of the VTR when the operator wishes to store an additional channel and place it in memory.

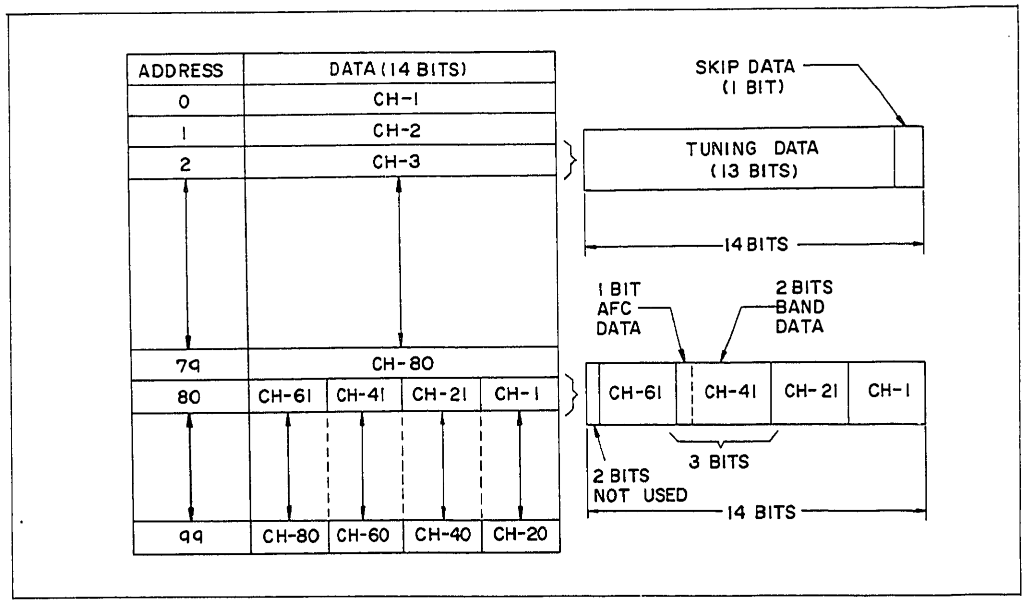

ADDRESS
DATA (14 BITS)
0
CH-1
1
CH-2
2
CH-3
79
CH-80
80
CH-61
CH-41
CH-21
CH-1
99
CH-80
CH-60
CH-40
CH-20
SKIP DATA (1 BIT)
TUNING DATA (13 BITS)
14 BITS
1 BIT AFC DATA
2 BITS BAND DATA
CH-61
CH-41
CH-21
CH-1
3 BITS
2 BITS NOT USED
14 BITS

Fig. 4-9 EAROM Memory Map

Starting at the "address set" block, the address or location of the tuning and skip data are placed in the EAROM. Moving next to the "erase" portion of the flowchart, the address location in the EAROM is automatically erased internally before storing the new tuning and skip data in this location. The data (tuning and skip) is next stored in the selected address location.

TU-μP now inputs the address where the band and AFC information is to be stored for the channel being stored in memory. Again, before the new information is stored in that particular memory location, any previous data is erased to ensure that the correct data is stored. Once the band and AFC data are stored in the EAROM, along with the tuning data, this information may now be recalled later.

The "data read" sequence is similar to the "data store" sequence. Instead of writing to the EAROM, TU-μP instructs the EAROM to read information out of the designated address into the TU-μP where it is converted to a DC tuning voltage. For example, the location or address of the tuning data of the desired channel is first placed in the EAROM. The EAROM reads the information from its memory, then loads this tuning data into its registers, and transfers the data to TU-μP. Next, TU-μP places the address of the band and AFC data into the EAROM. The EAROM reads the appropriate 3 bits of the band/AFC data into TU-μP where the band information is decoded. This allows TU-μp to switch the tuner to the proper band.

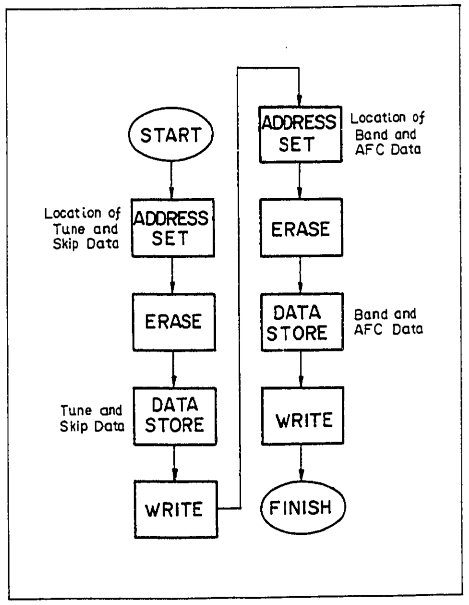

START
Location of Tune and Skip Data
ADDRESS SET
ERASE
Tune and Skip Data
DATA STORE
WRITE
ADDRESS SET
Location of Band and AFC Data
ERASE
DATA STORE
Band and AFC Data
WRITE
FINISH

Fig. 4-10(a) Data Store Sequence

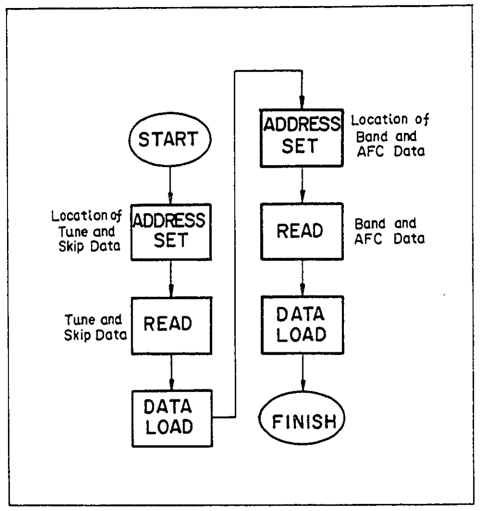

START
Location of Tune and Skip Data
ADDRESS SET
Tune and Skip Data
READ
DATA LOAD
ADDRESS SET
Location of Band and AFC Data
READ
Band and AFC Data
DATA LOAD
FINISH

Fig. 4-10(b) Data Read Sequence

Band switching

Fig. 4-10(c) shows a simplified band switching diagram.

The circuit is very similar to that in other VTRs. TU-µP transmits a two-digit code to band decoder IC802 via pins 17 and 18. The two-bit output from TU-µP is decoded by IC802 and output as a 4-bit band switching singal at pins 17, 19, 18 and 20. They are applied via PG802 to the tuner/IF circuit board.

IC802 BAND DECODER	BAND			
	"Lo" VHF	"Hi" VHF	SUPER	UHF
B0 (Pin 5)	0	1	0	1
B1 (Pin 4)	0	0	1	1
D0 (Pin 17)	1	0	0	0
D1 (Pin 19)	0	0	1	0
D2 (PIN 18)	0	1	0	0
D3 (Pin 20)	0	0	0	1

Sandswitching Code Chart

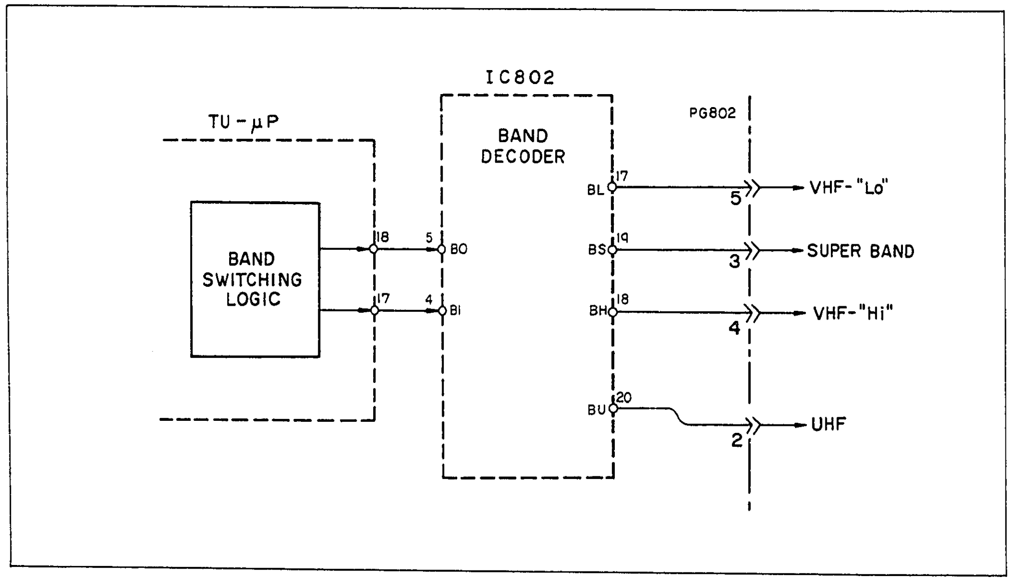

IC802
BAND DECODER
TU-µP
PG802
BAND SWITCHING LOGIC
18
5
BO
17
4
BI
BL
17
5
VHF-"Lo"
BS
19
3
SUPER BAND
BH
18
4
VHF-"Hi"
BU
20
2
UHF

Fig. 4-10(c) Band Switching Circuit

4-2-2 Input Selector

Fig. 4-10(d) is a simplified diagram of the input selector circuit. TU-µP receives the LINE/TUNER information from T-µP via the communications lines, and every time TU-µP inputs the data, it determines LINE/TUNER signal output voltage at pin 9 to "Hi" (LINE mode) and "Lo" (TUNER mode) alternately. This output is applied to two input selectors. One is the video input selector IC501 at pin 3. IC501 inputs the video signal from the video input jack at pin 2 and the video signal from the tuner/IF at pin 7, and selects the video signal at pin 2 when pin 3 is "Hi" and the video signal at pin 7 when pin 3 is "Lo". The selected video signal is supplied to the luminance/chroma processing circuit. The other is the audio input selector/audio processor IC401 at pin 15. IC401 inputs the audio signal from the audio input jack at pin 14 and the audio signal from the tuner/IF at pin 16, and selects the audio signal at pin 14 when pin 15 is "Hi" and the audio signal at pin 16 when pin 15 is "Lo". The selected audio signal is supplied to the audio processor in IC401.

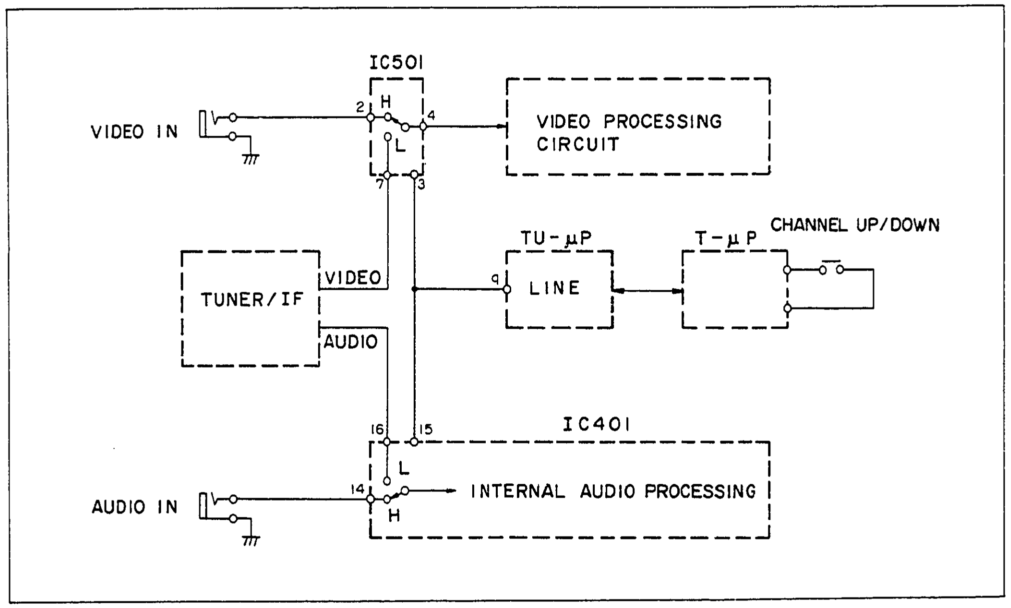

IC501
VIDEO IN
2
H
4
L
7
3
VIDEO PROCESSING CIRCUIT
TU-µP
T-µP
CHANNEL UP/DOWN
TUNER/IF
VIDEO
AUDIO
9
LINE
IC401
16
15
L
14
H
INTERNAL AUDIO PROCESSING
AUDIO IN

Fig. 4-10(d) Simplified Input Selector Circuit Diagram

4-2-3 Audio Processing Circuit

Fig. 4-10(e) is a block diagram of the audio circuit. One audio processing IC, IC401, controls the audio record processing, audio playback processing, bias ON/OFF operation and head operation.

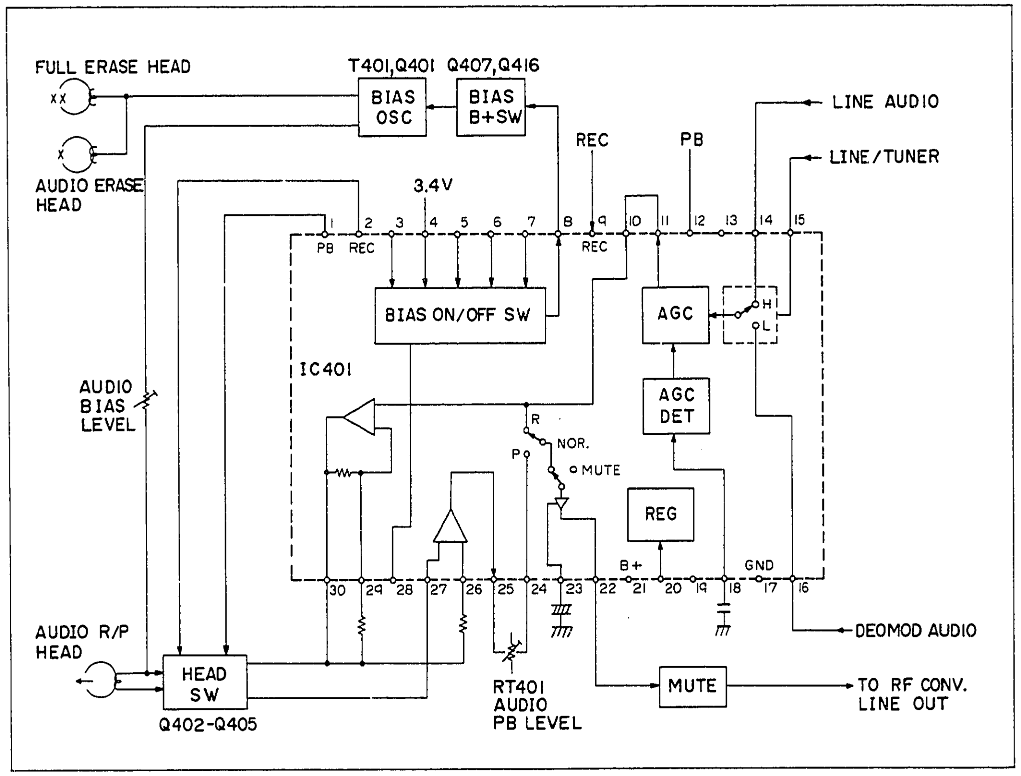

FULL ERASE HEAD
T401,Q401
Q407,Q416
BIAS OSC
BIAS B+SW
LINE AUDIO
REC
PB
LINE/TUNER
AUDIO ERASE HEAD
3.4V
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
PB
REC
REC
BIAS ON/OFF SW
AGC
H
L
IC401
AGC DET
AUDIO BIAS LEVEL
R
NOR.
P
MUTE
REG
B+
GND
30
29
28
27
26
25
24
23
22
21
20
19
18
17
16
AUDIO R/P HEAD
HEAD SW
Q402-Q405
RT401 AUDIO PB LEVEL
MUTE
DEOMOD AUDIO
TO RF CONV. LINE OUT

Fig. 4-10(e) Block Diagram of Audio Circuit

Audio record processing

Fig. 4-10(f) is a simplified diagram of the audio record processing circuit. When the VTR enters the record mode, the record mode setting input at pin 9 of IC401 goes "Hi". The "Hi" input at pin 9 changes over the REC/PB switches (S1/S2) in IC401 to "REC" and makes the bias oscillation controller active. The "Hi" input at pin 9 is also amplified and output at pin 2 to make the record head switch Q405 active. The audio signal supplied from the input selector descrived previously is amplified by the Line amplifier and leaves IC401 via pin 11. The signal reenters IC401 via pin 10 and is branched into two parts.

One is applied to the EE amplifier via S5 and is amplified. The output from the EE amplifier is applied to the AGC detector and EE/monitor output at pin 22. The audio signal at 22 is applied to the RF converter and audio output jack. The AGC detector rectifies the audio signal and filters it via capacitor C412 at pin 18, then applies it to the gain control input of the Line amplifier to determine the gain of the Line amplifier.

The other branched part is applied to the record amplifier. The record amplifier amplifies the audio signal matching the tape speed (SP, LP or EP) using the equalizer circuit at pin 29. The amplified audio signal is output at pin 30 and is applied to the bias signal from the bias oscillator circuit and is then supplied to the audio record/playback head to be recorded on the audio track.

The power voltage and the voltage supply time for the bias oscillator is controlled by IC401. IC401 sets the internal bias ON/OFF switch active when pin 9 goes "Hi" and determines the power voltage (approx. 10.7V) for the bias oscillator at pin 8. This voltage is determined by the voltage applied to pin 4 and is set to approx. 3.4V. The output at pin 8 is applied to the base of the bias oscillator B+ switch Q407 to set the power voltage of the bias oscillator to approx. 10V. The base voltage of Q407 becomes zero when the "MUTE" signal supplied from S-μP or the "ASBL" signal from the servo circuit goes "Hi" to switch off the bias oscillator in the record pause and assemble modes. The "MUTE" or "ASBL" signal turns Q416 on and drops the base voltage of Q407 to zero. The bias oscillator output is derived via pins 5 and 6 of T401. The bias signal at pin 5 of T401 is supplied to the full erase head and audio erase head. Meantime, the bias signal at pin 6 of T401 is applied to the recording audio signal via RT402. RT402 adjusts the bias current flowing to the audio record/playback head to the optimum level.

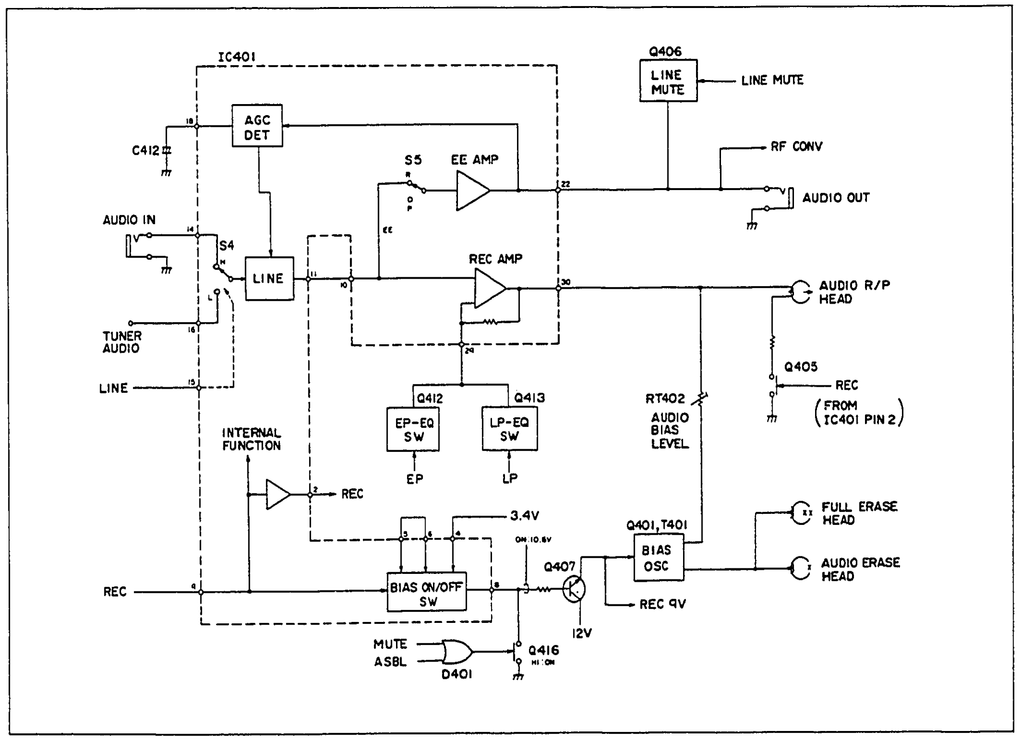

IC401
Q406
LINE MUTE
LINE MUTE
18
AGC DET
C412
S5
R
P
EE AMP
RF CONV
22
AUDIO OUT
AUDIO IN
14
S4
H
L
LINE
11
10
EE
REC AMP
30
AUDIO R/P HEAD
TUNER AUDIO
16
29
LINE
15
Q412
Q413
EP-EQ SW
LP-EQ SW
EP
LP
RT402
AUDIO BIAS LEVEL
Q405
REC
(FROM IC401 PIN 2)
INTERNAL FUNCTION
2
REC
3.4V
3
5
4
ON:10.6V
Q401,T401
BIAS OSC
FULL ERASE HEAD
AUDIO ERASE HEAD
REC
9
BIAS ON/OFF SW
8
Q407
REC 9V
12V
MUTE
ASBL
D401
Q416
HI:ON

Fig. 4-10(f) Simplified Audio Record Processing Circuit Diagram

Audio playback processing

Fig. 4-10(g) is a simplified diagram of the audio playback processing circuit. When the VTR enters the playback mode, the playback mode setting input at pin 12 of IC401 goes "Hi". The "Hi" input at pin 12 changes over the REC/PB switch S1 in IC401 to "PB" and is also inverted by the internal inverter and is output at pin 1. The output ("Lo") at pin 1 is applied to inverter Q402 and is inverted to be "Hi" and is applied to the head switches (Q403, Q404). This causes Q403 and Q404 to be active and one terminal of the audio record/playback head is grounded. The audio signal picked up by the audio record/playback head is supplied to the preamplifier via the audio PB input at pin 27. The preamplifier amplifies the playback audio signal with very low level and also determines the amount of deemphasis matching the tape speed (SP or LP) using the equalizer circuit at pins 26 and 25. The amplified and emphasized audio signal is output at pin 25 and is supplied to the PB amplifier in IC401 via RT401, pin 24 and S1. RT401 adjusts the input level of the PB amplifier so it becomes the same level as in the record/E-E modes or the specified level. The PB amplifier amplifies the playback audio signal up to the level required for the RF converter and audio output jack. The amplified audio siganl is output at pin 22 and is supplied to the RF converter and audio output jack via line mute switch Q406. Q406 is switched on and off by the "LINE MUTE" signal supplied from S-μP and mutes the audio signal during trick play and loading modes.

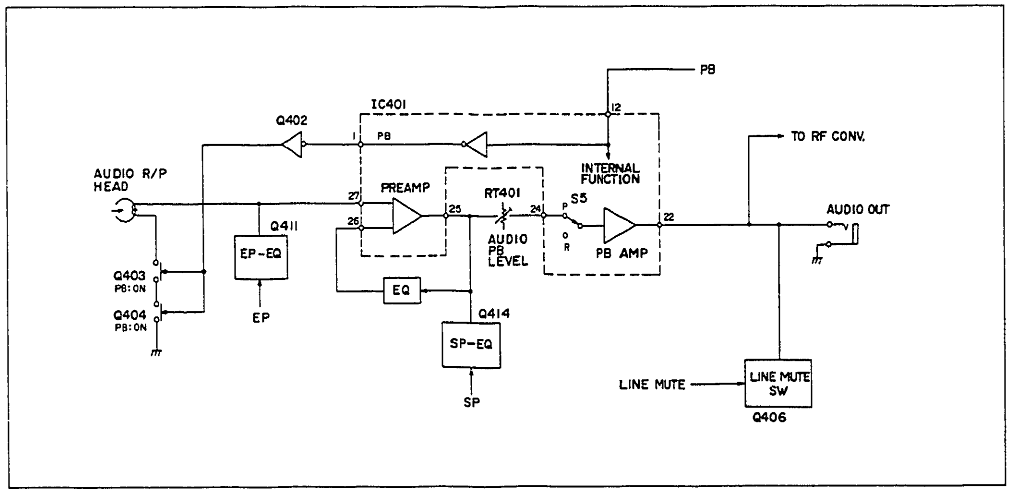

PB
IC401
12
Q402
1
PB
TO RF CONV.
INTERNAL FUNCTION
AUDIO R/P HEAD
27
PREAMP
RT401
25
24
P
S5
26
AUDIO PB LEVEL
R
PB AMP
22
AUDIO OUT
Q411
EP-EQ
Q403 PB:ON
Q404 PB:ON
EP
EQ
Q414
SP-EQ
SP
LINE MUTE
LINE MUTE SW
Q406

Fig. 4-10(g) Simplified Audio Playback Processing Circuit Diagram

4-2-4. VIDEO PROCESSING

(1) VHS HQ SYSTEM (Figs. 4-11, 4-12)

The VHS HQ (High Quality) system has been employed from this series of models VT-1100A, VT-1400A, etc. VHS HQ VTRs are compatible with conventional VHS VTRs. A VHS HQ VTR must satisfy two or more of the following conditions.

- White clip level up 20% * (SP, LP, EP)
- Detail enhancer (SP)
- Luminance vertical processor
- Chrominance vertical processor (This is not used in the VT-1100A/1105A.) EP only.

* This item must definitely be provided.

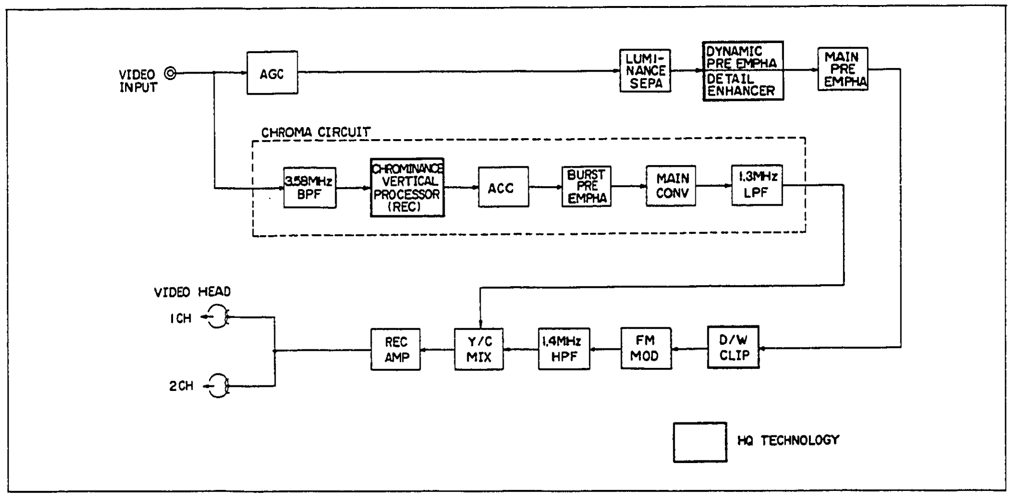

VIDEO INPUT
AGC
LUMI-NANCE SEPA
DYNAMIC PRE EMPHA
DETAIL ENHANCER
MAIN PRE EMPHA
CHROMA CIRCUIT
3.58MHz BPF
CHROMINANCE VERTICAL PROCESSOR (REC)
ACC
BURST PRE EMPHA
MAIN CONV
1.3MHz LPF
VIDEO HEAD
1CH
2CH
REC AMP
Y/C MIX
1.4MHz HPF
FM MOD
D/W CLIP
HQ TECHNOLOGY

Fig. 4-11 VHS HQ System (Record)

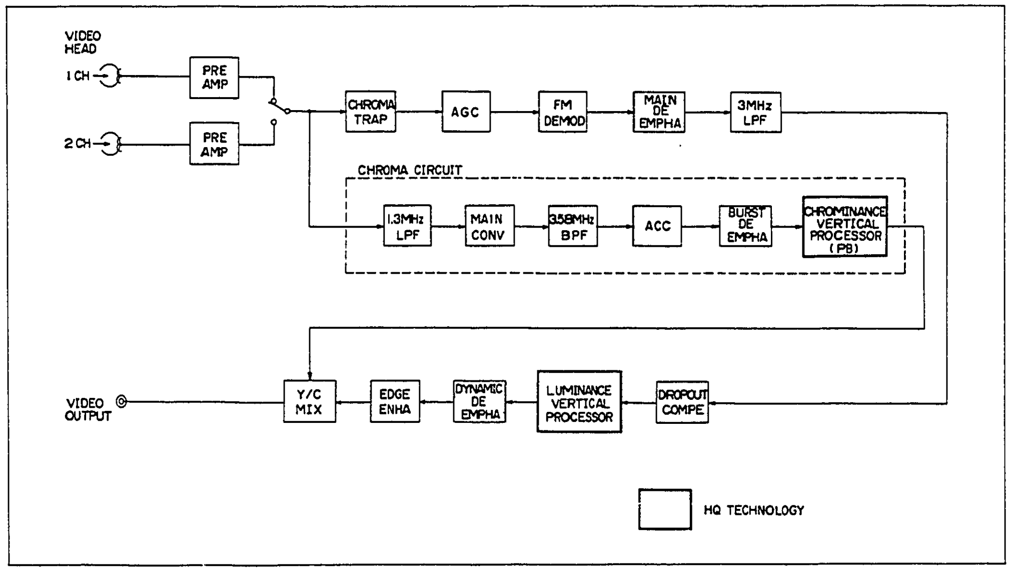

VIDEO HEAD
1CH
2CH
PRE AMP
PRE AMP
CHROMA TRAP
AGC
FM DEMOD
MAIN DE EMPHA
3MHz LPF
CHROMA CIRCUIT
1.3MHz LPF
MAIN CONV
3.58MHz BPF
ACC
BURST DE EMPHA
CHROMINANCE VERTICAL PROCESSOR (PB)
VIDEO OUTPUT
Y/C MIX
EDGE ENHA
DYNAMIC DE EMPHA
LUMINANCE VERTICAL PROCESSOR
DROPOUT COMPE
HQ TECHNOLOGY

Fig. 4-12 VHS HQ System (Playback)

1) White clip level up 20% (Fig. 4-13)

Before the luminance signal is recorded, it is FM-modulated and mixed with the chroma signal and is then applied to the video heads. If noise occurring in the recording and playback loops enters the FM-modulated signal and the signal is FM-demodulated without any processing, the noise level becomes higher as the frequency is higher. Therefore, in a VHS VTR, the high-frequency components of the video signal are preemphasized by the preemphasis circuit before the signal is FM-modulated, and the high-frequency components are deemphasized by the deemphasis circuit after the signal is FM-demodulated.

When the high-frequency components are emphasized by the preemphasis circuit, overshoots are superimposed on the signal waveform as shown in Fig. 4-13 (c), and when the signal is FM-modulated, overmodulation occurs at the peak of the white peak level (shown by B in Fig. 4-13 (c)) and this may cause the picture quality to be degraded (black/white inversion). To prevent this, a white clip circuit was provided for the input of the FM modulator in previous VTRs. Since the characteristics of VTRs and video tape have improved recently, the clip level has been increased by 20% as shown in Fig. 4-13 (d) to improve the pulse response characteristics. As a result, the leading edges of the waveform (the edges in picture) where the black changes to white on the TV screen are played back more clearly.

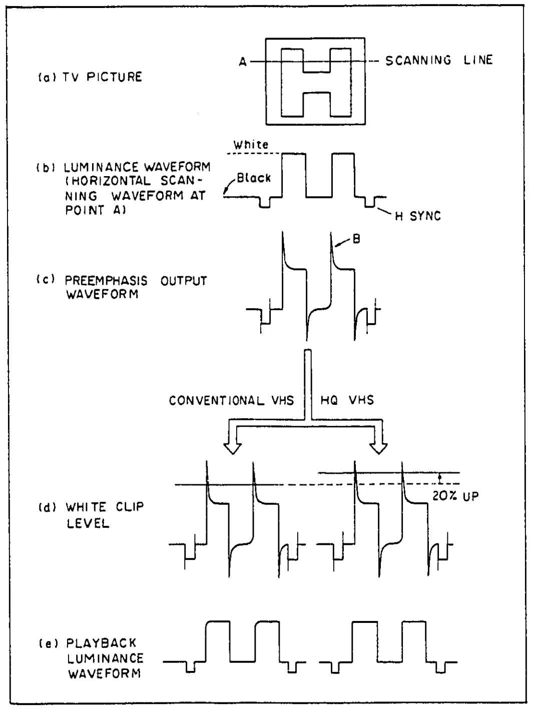
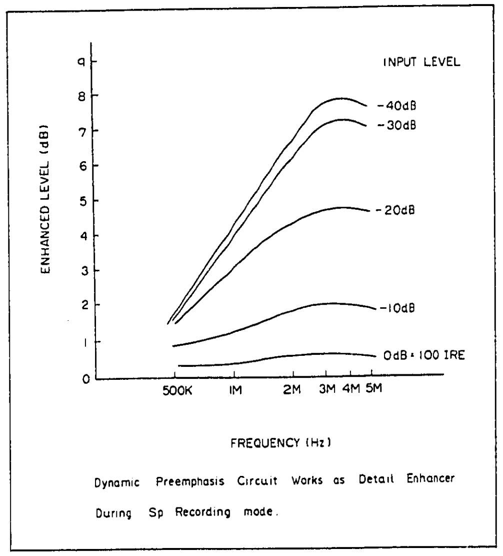

(a) TV PICTURE
A
SCANNING LINE
(b) LUMINANCE WAVEFORM (HORIZONTAL SCANNING WAVEFORM AT POINT A)
White
Black
H SYNC
(c) PREEMPHASIS OUTPUT WAVEFORM
B
CONVENTIONAL VHS
HQ VHS
(d) WHITE CLIP LEVEL
20% UP
(e) PLAYBACK LUMINANCE WAVEFORM

Fig. 4-13 White Clip Circuit

2) Detail Enhancer (Fig. 4-14)

When the video signal is recorded in the EP mode, dynamic preemphasis is applied to the video signal according to the signal input level to boost the medium frequencies (near 1 MHz) during recording in a conventional VTR. (Dynamic deemphasis is applied to the signal during playback.) This improves the S/N when the video signal level is low because the medium frequencies are boosted.

A detail enhancer changes the constants of the circuit using the dynamic emphasis circuit in the SP mode and enhances the high-frequencies of 3 - 4 MHz according to the input level of the video signal. Doing this during recording, the detail enhancer enhances the overall high-frequency response during playback as well as in recording. Therefore, when the signal is played back, an object with fine lines (such as a lawn, hair, etc.) can be seen more clearly. (This enhancer does not process the signal during playback.)



Dynamic Preemphasis Circuit Works as Detail Enhancer During Sp Recording mode.

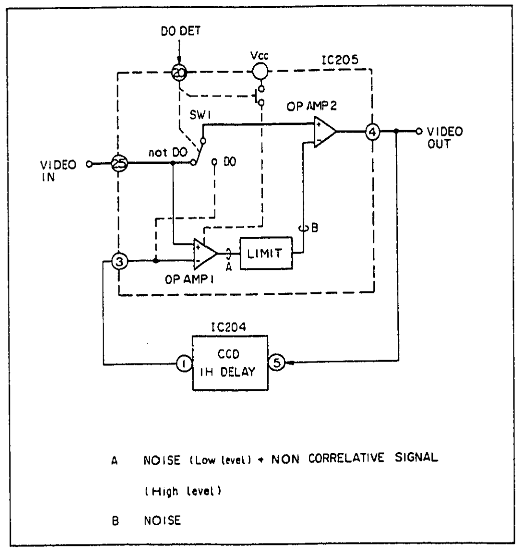
Fig. 4-14 SP Detail Enhancer

3) Luminance Vertical Processor (Fig. 4-15)

To improve S/N of the luminance signal, the line correlative noise canceler using a 1H glass delay line is employed in model VT-62A. This noise canceler averages the addition of the main playback signal and 1H delay playback signal and reduces the non-correlative noise such as white noise occurring during recording and playback to improve the S/N. To delay the FM signal by 1H by this method, another demodulator and deemphasis circuits were required as well as those for the main signal.

This new line correlative noise canceler (called as a vertical processor) uses a 1H delay circuit with a CCD and delays the signal by 1H in the base band (video signal) and comprises a feedback type noise canceler circuit. With this noise canceler, the S/N is improved, and a demodulator, deemphasis circuit and a control adjusting the level between the main and delay signals can be eliminated.

Fig. 4-15 shows the configuration of this vertical processor circuit. (This circuit also works as a dropout compensator and operates in all tape speed modes, SP, LP and EP.) The video signal demodulated by the FM demodulator enters IC205 via pin 25 and is output at pin 4 through SW1 and OP AMP 2. Part of this output signal is 1H-delayed by the CCD 1H DELAY circuit, IC204, and reenters IC205 via pin 3. The OP AMP 1 outputs the difference between the main signal and 1H-delayed signal. This difference signal A consists of the non-correlative



A NOISE (Low level) + NON CORRELATIVE SIGNAL (High level)

B NOISE

Fig. 4-15 Luminance Vertical Processor

noise component (white noise with low level) and the signal without vertical correlation in the video signal (generally, the signal with high level). Signal B is produced by applying signal A to the limiter which derives correlative noise with low level (white noise). The OP AMP 2 removes noise B from the video signal to improve the S/N.
As can be seen in Fig. 4-15, the vertical processor forms a feedback circuit. By circulating the signal twice and three times, the vertical processor overlaps the signals 2H before and 3H before to enhance the noise reduction effect. (The dropout compensation will be described separately.)

4) Chrominance Vertical Processor (Fig. 4-16, 4-17)

This circuit improves the chroma S/N in the EP (LP) mode and its basic principle is very similar to that of the luminance vertical processor. Fig. 4-16 is a basic principle diagram of this circuit during playback. The input signal (a) and 1H-delayed signal (b) are applied to the processor-2. Since the chroma subcarrier signal fsc has the phase shifted by 180° for every 1H, the processor-2 output in a picture with vertical correlation is only noise component (c) because two fsc signals cancel each other. Since the fsc component (with the level higher than the noise component generally) appears in the processor-2 output in a picture with no vertical correlation, the non-correlative component is eliminated by the limiter circuit in the next stage and the noise component (d) is derived, then this noise component (d) (limiter output) is subtracted from the original input signal (a) to improve the S/N.
In this principle diagram, no feedback circuit is present in the 1H delay circuit and a feed-forward circuit is formed so the signal used for noise canceling is only the signal 1H before. The circuit actually used is a feedback type as shown in Fig. 4-17, and feedback is applied with weighting of 1/K (approx. 0.7). The noise cancel effect is enhanced by making the weighting less in sequence also using the signals 2H and 3H before. When this system is employed, color smears occur slightly in the non-correlative section but this does not affect compatibility. To prevent this, the polarities of the limiter output shown in Fig. 4-17 are inverted and the signal in the non-correlative section is added in the processor-3 during recording to previously correct the distortion occurring during playback (a sort of preemphasis is applied).

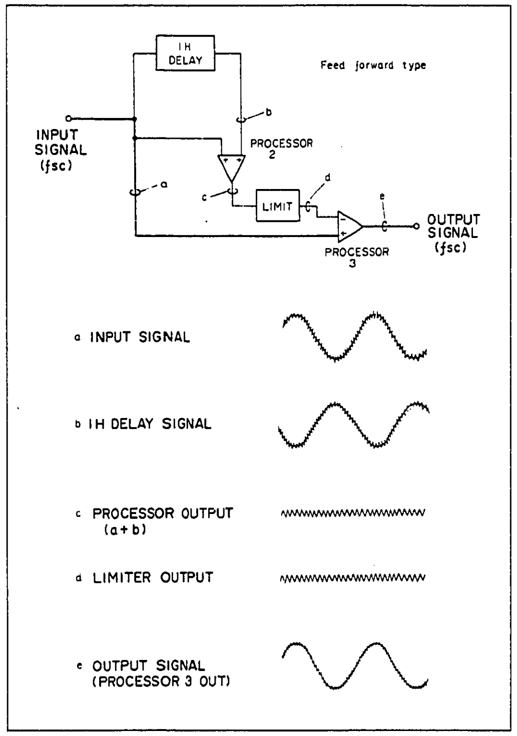

1H DELAY
Feed forward type
b
INPUT SIGNAL (fsc)
PROCESSOR 2
a
c
LIMIT
d
e
OUTPUT SIGNAL (fsc)
PROCESSOR 3
a INPUT SIGNAL
b 1H DELAY SIGNAL
c PROCESSOR OUTPUT (a+b)
d LIMITER OUTPUT
e OUTPUT SIGNAL (PROCESSOR 3 OUT)

Fig. 4-16 EP Chrominance Vertical Processor (Ideal)

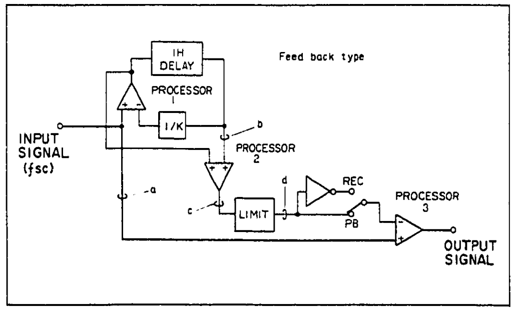

1H DELAY
Feed back type
PROCESSOR 1
1/K
b
INPUT SIGNAL (fsc)
PROCESSOR 2
a
c
d
LIMIT
REC
PB
PROCESSOR 3
OUTPUT SIGNAL

Fig. 4-17 EP Chrominance Vertical Processor (Actual)

2) GENERAL

The video signal input to the video processing circuit is a composite video signal consisting of the luminance, chroma and sync components.

This circuit separates the composite video signal into the luminance signal (including the sync signal) and the chroma signal. Then the circuit FM-modulates the luminance signal to convert it to high-frequency components and converts the chroma signal to low-frequency components, then mixes the converted luminance and chroma signals to supply them to the video heads.

1) Overview of Luminance Record Processing Circuit (Fig. 4-19)

(a) AGC circuit
This circuit controls the input video signal so its output level is always constant regardless of level fluctuations in the input video signal supplied from the video input jack or RF converter circuit.

(b) Luminance separator circuit
This circuit extracts only the luminance signal components from the composite video signal. Using a lowpass filter and comb filter, the circuit separates the luminance signal and chroma signal.

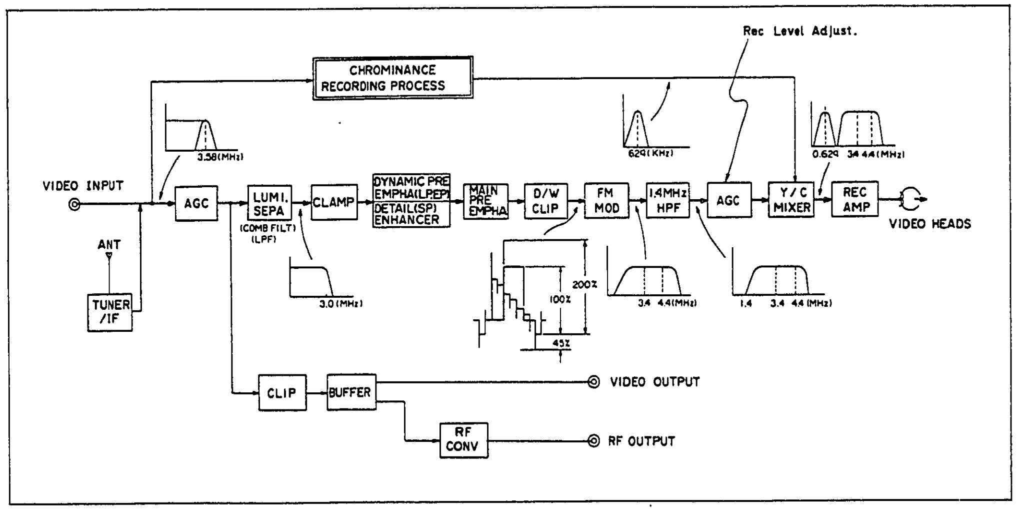

Rec Level Adjust.
CHROMINANCE RECORDING PROCESS
3.58(MHz)
629(KHz)
0.629 3.4 4.4(MHz)
VIDEO INPUT
AGC
LUMI. SEPA
(COMB FILT)
(LPF)
CLAMP
DYNAMIC PRE EMPHA(LP,EP)
DETAIL(SP) ENHANCER
MAIN PRE EMPHA
D/W CLIP
FM MOD
1.4MHz HPF
AGC
Y/C MIXER
REC AMP
VIDEO HEADS
ANT
TUNER /IF
3.0(MHz)
200%
100%
45%
3.4 4.4(MHz)
1.4 3.4 4.4(MHz)
CLIP
BUFFER
VIDEO OUTPUT
RF CONV
RF OUTPUT

Fig. 4-19 Luminance Record Block Diagram

(c) Clamp circuit
This circuit fixes the DC voltage at the sync tip so it does not change due to the variation in the contents of the video signal. This is necessary for the dark/white clip circuit and FM modulator circuit in the later stage to operate normally.

(d) Dynamic preemphasis circuit
This varies the gain of frequencies centering near 1 MHz according to the input level of the video signal (picture components). When the input signal level is low (picture is dark), this circuit raises the video signal level centering near 1 MHz to improve the S/N. When the signal is passed through a circuit with the reverse characteristics (dynamic deemphasis circuit) during playback, the overall frequency characteristics become flat. This circuit works in the SP and EP tape speed modes.

(e) Detail enhancer circuit
This circuit boosts the high-frequencies of 3 - 4 MHz for recording when the input level of the video signal is low so that a lawn, hair, etc. with fine lines is seen clearly. This circuit works only in the SP mode.

(f) Main preemphasis circuit
As the frequencies of noise in the signal having passed through the FM modulator circuit are higher, its level becomes higher. This circuit emphasizes the high-frequency components of the signal previously during recording. During playback, the signal is passed through a circuit with the reverse characteristics (main deemphasis circuit) and the levels of high-frequency components are lowered, thus the S/N is improved.

(g) Dark/white clip circuit
When the video signal is preemphasized by the preemphasis circuit in the former stage, overshoots occur on the leading and trailing edges of the video signal. When it is fed to the next FM modulator as it is, overmodulation occurs; to prevent this, this circuit clips overshoots of the specified level or more.

(h) FM modulator circuit
The FM modulator circuit FM-modulates the video signal described above so that its sync tip is 3.4 MHz and the white peak is 4.4 MHz. However, this carrier frequency is shifted by approx. 1/2 fH (7.87 kHz) in CH-2 during the SP, LP and EP modes, to reduce beats interference due to crosstalk during play.

(i) 1.4 MHz HPF circuit
The HPF circuit attenuates the chrominance signal in the down-converted chroma signal band (629 kHz ± 500 kHz) to avoid color beats interference in the playback mode.

(j) AGC, Y/C mixer, recording amplifier circuits
The AGC circuit controls the luminance signal (FM modulated wave) output from the highpass filter so its recording current becomes constant, and the Y/C mixer mixes this AGC-controlled luminance signal with the chroma signal. The mixed signal is amplified by the recording amplifier and is then supplied to the video heads.

(k) E-E monitor circuit
After passing through the AGC circuit, the video signal is output via the clip circuit as an E-E monitor signal.

2) Overview of Luminance Playback Processing Circuit (Fig. 4-20)

Fig. 4-20 shows the main route and processing of the luminance signal in the playback mode.

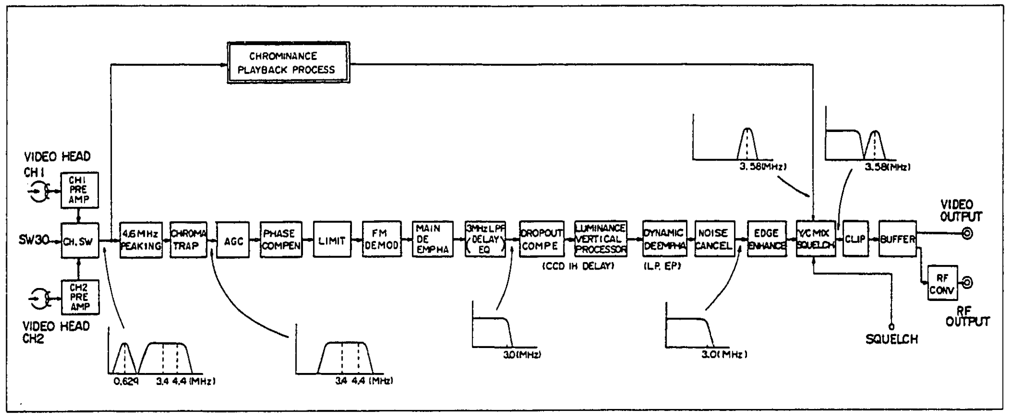


Fig. 4-20 Luminance Playback Block Diagram

(a) Preamplifier
CH1 and CH2 preamplifiers fully amplify the weak play signal picked up from the magnetic tape via the CH-1 and CH-2 video heads, and in addition, feed back the output of the preamplifier circuit to provide flat characteristics.
The same frequency compensation as in "60" Line models is performed by the equalizer circuit in the next stage.

(b) Channel Switch Circuit
The channel switch circuit switches the CH-1 or CH-2 signal using the SW30 signal to obtain a continuous signal.

(c) 4.6 MHz Peaking Circuit
As the frequency response of the preamplifiers in the previous stage is flat, the 4.6 MHz peaking circuit performs the same frequency compensation as in conventional models. That is, the 4.6 MHz peaking circuit compensates the head playback characteristics so that the total playback characteristics from the video heads until the 4.6 MHz peaking circuit are flat.

(d) Chroma Trap Circuit
This circuit removes the playback chroma signal (629 kHz) and supplies only the luminance

signal to the AGC circuit in the next stage.

(e) AGC Circuit
The AGC circuit operates so that the output level is always constant regardless of input level fluctuations, to prevent flickering due to the deviation and output level differences in the FM signal.

(f) Phase Compensation Circuit
The phase compensation circuit corrects the phase drift occurring in the 4.6 MHz peaking circuit described previously so that the video signal is not distorted during FM demodulation.

(g) Limiter Circuit
The limiter circuit removes amplitude variations in the FM signal. The limiter also limits the amplitude of the FM signal after boosting the FM high-frequency components to prevent black and white from being inverted. That is, the FM carrier output level becomes smaller than the low-frequency sideband level in the high modulation section of the played back FM signal causing distortion; when it is demodulated via the FM demodulator as it is, black/white inversion occurs. The limiter circuit prevents this.

(h) FM Demodulator Circuit
The video signal has been FM-modulated so that its sync tip is 3.4 MHz and its white peak is 4.4 MHz during recording, so the FM demodulator circuit demodulates it to the original video signal during play.

(i) Main Deemphasis Circuit
The main deemphasis circuit has reverse characteristics to the main preemphasis circuit used during recording; this circuit improves the S/N ratio while returning the high-frequency components emphasized by the preemphasis circuit during recording to its original value.

(j) 3 MHz LPF Circuit (Delay Equalizer)
The 3 MHz LPF circuit eliminates the FM carrier with its frequency 3.0 MHz or more remaining in the video signal demodulated in the previous stage. The delay equalizer circuit is also used for delay to match the luminance phase with the chroma signal, the same as in recording.

(k) Dropout Compensation Circuit
The dropout compensation circuit corrects dropout in the FM signal caused by either dust or dirt on the tape, poor or irregular tape coating and prevents picture noise from occurring.
This circuit utilizes the 1H delay circuit in the video signal band using a CCD to compensate for dropout.

(l) Luminance vertical processor
This is a noise canceler circuit which uses 1H correlation of the video signal.
This noise canceler uses a 1H delay circuit with a CCD (used in common with the circuit operated in the dropout compensation circuit described previously) and delays the signal by 1H in the base band (video signal) to comprise a feedback type noise canceler circuit.

(m) Dynamic Deemphasis Circuit
As described in the item "Luminance Recording Process", the dynamic preemphasis circuit varies the amount of emphasis according to the record signal level. The dynamic deemphasis circuit is provided with the characteristics in reverse to that of the dynamic preemphasis circuit; this varies the attenuation of the high-frequency component according to the playback signal level and returns the high frequency component amplitude boosted by the dynamic preemphasis circuit to the original amplitude.
This circuit works in the LP and EP modes.

(n) Noise Cancel Circuit
The noise cancel circuit eliminates snow noise remaining in the video signal to produce a video signal with clear edges.

(o) Edge enhancer circuit
This circuit forms a second differentiation type enhancer which emphasizes edges in the picture during playback.

(p) Y/C mixer, clip, buffer circuits
The Y/C mixer mixes the luminance signal output from the edge enhancer and the chroma signal converted to 3.58 MHz.

The mixed signal is passed through the clip and buffer circuits and is output as a playback signal.
This Y/C mixer also works as a squelch circuit.

3) Overview of Chrominance Record Processing Circuit (Fig. 4-21)

Fig. 4-21 shows the main route and processing of the chroma signal in the record mode.

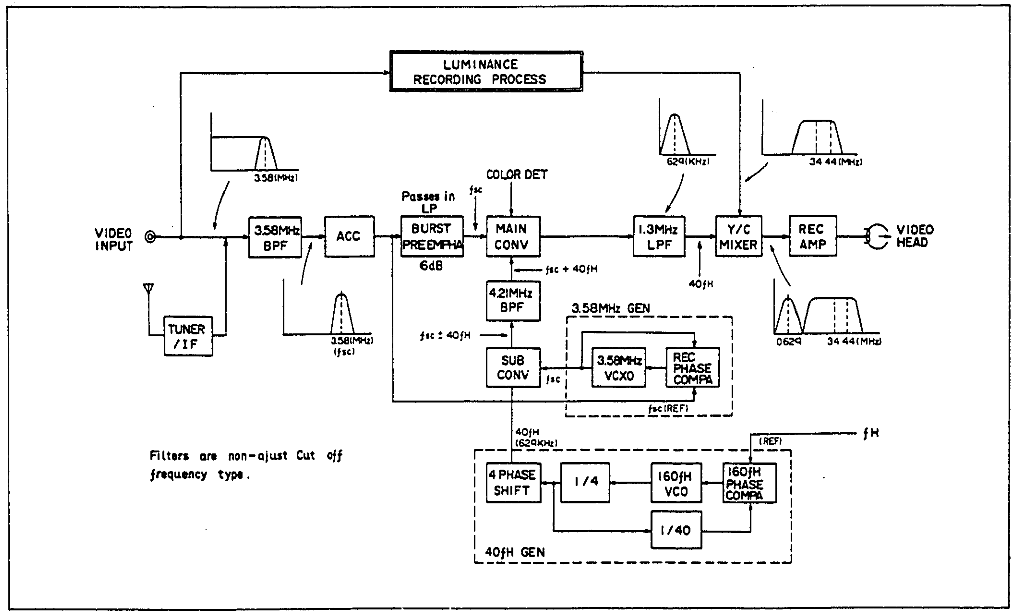


Fig. 4-21 Chroma Record Block Diagram

(a) 3.58 MHz BPF Circuit
The 3.56 MHz bandpass filter circuit selects and passes only the chroma signal (3.58 MHz ± 500 kHz) in the video signal supplied from the video input jack or RF converter circuit.

(b) ACC Circuit
The ACC circuit is provided so that the output level is always constant regardless of input level fluctuations of the chroma signal.

(c) Burst Preemphasis Circuit
The burst preemphasis circuit emphasizes only the burst signal by 6 dB in the SP and EP modes to prevent deterioration of the S/N of the burst signal. In the LP mode, the signal passes this circuit without being controlled.

(d) Record Main Converter Circuit
The record main converter circuit mixes the chroma signal (3.58 MHz ± 500 kHz) fed from the circuit in the previous stage and the precise and stabilized 4.21 MHz carrier signal (fsc + 40 fH) synchronized with the input video signal (H SYNC signal and burst signal). Then it selects the down-converted chroma signal (629 kHz ± 500 kHz) via the 1.3 MHz LPF circuit described later.

(e) 1.3 MHz LPF Circuit
The LPF circuit selects and passes the chroma signal (629 kHz ± 500 kHz) obtained by down-converting the output signal (((3.58 MHz ± 500 kHz)) ± ((3.58 MHz + 629 kHz))) mixed via the record main converter circuit in the previous stage. The chroma signal is adjusted to the optimum level by RT202 and mixed with the FM-modulated luminance signal in the Y/C mixer circuit described in the item "Luminance Record Processing" to become the video recording signal and flows along the same route as described for the luminance signal.

(f) Y/C Mixer / REC Amp Circuit
Same as in Luminance Record Processing Circuit.

(g) 3.58 MHz Generator
The 3.58 GEN circuit during recording oscillates to produce the precise and stable 3.58 MHz signal (fsc) which is synchronized with the burst signal, and this output is sent to the 4.21 MHz sub converter circuit, 3.58 MHz record phase comparator circuit and the color killer detector circuit.

(h) 40fH Generator
During recording the 40fH GEN circuit oscillates the precise and stable 629 kHz signal (40fH) synchronized with the horizontal sync signal, and in addition, this phase advances by 90° every 1H in CH-1 recording, synchronizing with the H.SYNC signal, and in CH-2, it is delayed by 90° every 1H, in reverse. During play, the crosstalk of the chroma signal is removed by reverse processing and making it pass through the 1H delay line.

(i) Sub Converter Circuit
The 4.21 MHz sub converter circuit mixes the output signal (3.58 MHz: fsc) from the 3.58 MHz VCO circuit and the output signal (6.29 kHz: 40 fH) from the 40 fH GEN described previously, and then selects and passes the mixed 4.21 MHz (3.58 MHz + 629 kHz) signal using the next 4.21 MHz BPF circuit, and supplies it to the record main converter circuit.

(j) 4.21 MHz BPF Circuit
The 4.21 MHz BPF circuit selects and passes the mixed 4.21 MHz (3.58 MHz + 629 kHz) signal and then supplies this output to the record main converter.

4) Overview of Chrominance Playback Processing Circuit (Fig. 4-22)

Fig. 4-22 shows the main route and processing of the chroma signal during playback.

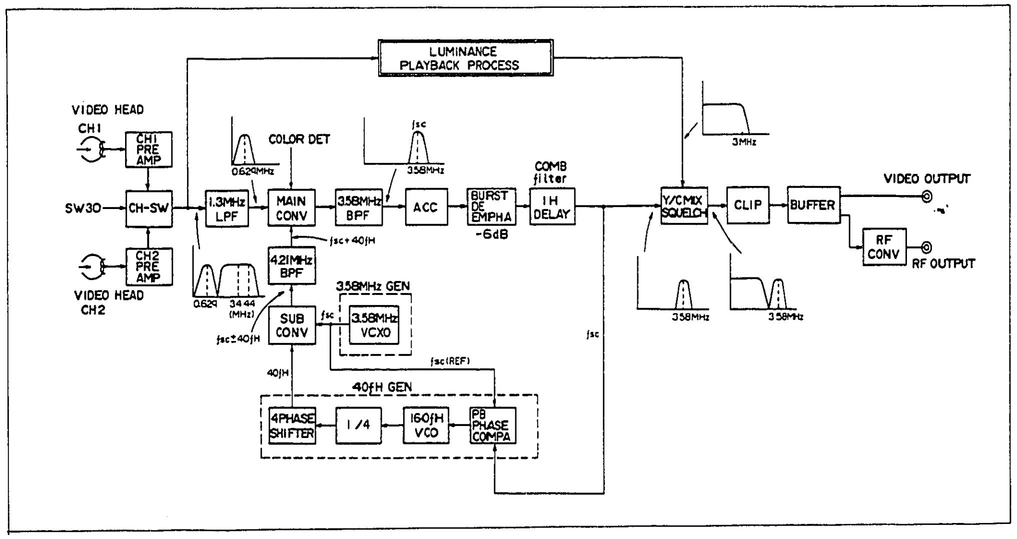


Fig. 4-22 Chrominance Playback Block Diagram

(a) Preamplifier/Channel Switch Circuits
Described previously in "Luminance Playback Processing Circuit".

(b) 1.3 MHz LPF Circuits
The 1.3 MHz LPF circuit selects and passes the chroma signal down-converted to 629 kHz ± 500 kHz from the played back video signal supplied from the channel switch circuit in the previous stage.

(c) Playback Main Converter Circuit
The PB main converter circuit mixes the chroma signal (629 kHz ± 500 kHz) fed from the circuit in the previous stage and the 4.21 MHz carrier (fsc + 40 fH) which is synchronized with the 3.58 MHz crystal oscillator, and then selects the original chroma signal (3.58 MHz ± 500 kHz) via the 3.58 MHz BPF circuit described later. A closed loop is formed among PB MAIN CONV., 3.58 MHz BPF, ACC, BURST

DEEMPHA, 1H DELAY LINE, 40 fH GEN, 4.21 MHz SUB CONV., 3.58 MHz OSC and 4.21 MHz BPF to cancel the frequency variation of the chroma signal caused by the servo fluctuation.

(d) 3.58 MHz BPF Circuit
The 3.58 MHz BPF circuit selects the chroma signal up-converted from the output signal (((629 kHz ± 500 kHz)) ± ((3.58 MHz ± 629 kHz))) of the playback main converter circuit and allows it to pass.

(e) ACC Circuit
Same as in recording.

(f) Burst Deemphasis Circuit
The burst signal is emphasized by 6dB in the SP and EP modes during recording to prevent deterioration of the S/N, so this circuit attenuates it by 6dB in reverse to return the burst signal to its original level.

(g) 1H Delay Line Circuit
The 1H delay line circuit is a filter to eliminate crosstalk in the chroma signal. That is, when the phase of the chroma signal is advanced by 90° every 1H in CH-1 and delayed by 90° every 1H in CH-2 during recording, and it is played back with the crosstalk contained and the phase is returned to the original phase by the reverse process. But the phase of the crosstalk contained in the main signal is reversed every 1H by the reverse process. Then these signals are routed to the 1H delay line which is composed of a direct path and a 1H delay path.
The signals from the delay and the direct paths are added together in the delay line, and the crosstalk components cancel each other because the phases are opposite to each other depending on the paths the signals have passed.

(h) Y/C Mixer/Clip/Buffer Circuit
Same as in Luminance Playback Processing Circuit.

(i) 3.58 MHz VCXO Circuit
The 3.58 MHz VCXO operates as a fixed crystal oscillator during play, generates the precise and stable 3.58 MHz signal, and supplies it to the 4.21 MHz sub converter, color killer detector and PB APC phase comparator.

(j) 40 fH Generator Circuit
The 40 fH GEN circuit produces the 629 kHz which contains frequency variation and phase rotation, to reproduce original chroma signal in the playback main converter. The frequency variation components are needed to cancel frequency fluctuations in the reproduced chroma signal caused by the servo fluctuations. The phase rotation is required for the playback main converter to retrieve the original 3.58 MHz chroma signal which has no phase rotation from the reproduced 629 kHz chroma signal of which the phase changes by 90° every 1H.

(k) 4.21 MHz Sub Converter
The 4.21 MHz sub converter circuit mixes the output signal (3.58 MHz: fsc) from the 3.58 MHz VCXO and output signal (629 kHz: 40 fH) from the 40 fH GEN, and then creates the mixed 4.21 MHz (3.58 MHz + 629 kHz) signal, and supplies it to the 4.21 MHz BPF circuit.

(l) 4.21 MHz Bandpass Filter
Same as in recording.
The 4.21 MHz BPF circuit selects and passes the mixed 4.21 MHz (3.58 MHz + 629 kHz) signal and then supplies this output to the playback main converter.

(3) LUMINANCE RECORDING PROCESS (Fig. 4-33a)

1) General

The luminance recording loop consists of IC201 and IC205 for main controls and peripheral IC202 and IC208. These ICs have been developed for these "1000" series VTRs which use the HQ circuit.

2) Input Select Switch

The line input video or tuner video is selcted by switch IC501 and is supplied to the luminance/chrominance circuit IC201 via pin 1. This switching is performed by the operator operating the channel select switch (S772/S773) on the front of the VTR. The switching output is applied to IC501 via IC751 (timer μP) and IC801 (tuning μP) to switch IC501.

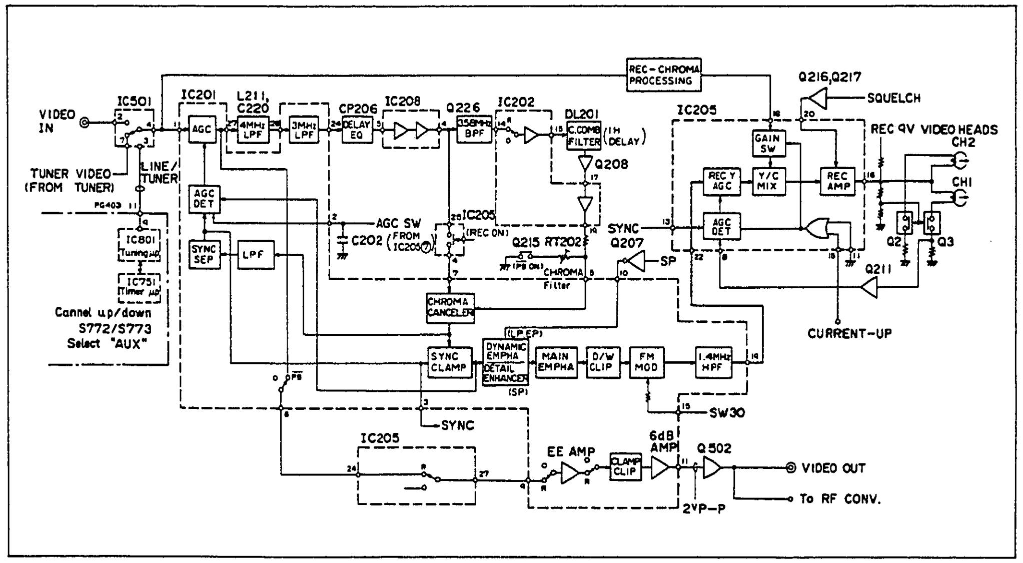

VIDEO IN
IC501
TUNER VIDEO (FROM TUNER)
LINE/TUNER
PG403
IC801 Tuning μP
IC751 Timer μP
Cannel up/down S772/S773 Select "AUX"
IC201
AGC
L211, C220
4MHz LPF
3MHz LPF
CP206
DELAY EQ
IC208
Q226
3.58MHz BPF
IC202
DL201
C.COMB FILTER
(1H DELAY)
Q208
AGC DET
SYNC SEP
LPF
AGC SW
C202 (FROM IC205⑦)
IC205
(REC ON)
Q215 RT202
(PB ON)
CHROMA Filter
CHROMA CANCELER
(LP,EP)
SYNC CLAMP
DYNAMIC EMPHA
DETAIL ENHANCER
(SP)
MAIN EMPHA
D/W CLIP
FM MOD
1.4MHz HPF
SW30
PB
SYNC
IC205
EE AMP
CLAMP CLIP
6dB AMP
Q502
2VP-P
VIDEO OUT
To RF CONV.
REC-CHROMA PROCESSING
Q216,Q217
SQUELCH
IC205
GAIN SW
REC Y AGC
Y/C MIX
REC AMP
AGC DET
SYNC
Q207
SP
REC 9V
VIDEO HEADS
CH2
CH1
Q2
Q3
Q211
CURRENT-UP

Fig. 4-33a Simplified Luminance Record Circuit

3) AGC (Automatic Gain Control) (Fig. 4-23, 4-24)

The Tuner/IF output video or external input video is selcted by video input selector IC501 and is supplied via pin 1 to the AGC circuit video processing IC201. The AGC circuit is a variable amplifier the gain of which is controlled so the output passing through this circuit is always constsnt (approx. 1 Vp-p) using the detection output of the AGC detector. The AGC detector feeds back the output of the AGC circuit to determine the gain control voltage of the AGC circuit. The video signal fed back to the AGC detector is derived from the output of the chroma canceler and is branched into two circuits. Part is applied to the AGC detector via the clamp circuit. The clamp circuit fixes the sync tip level because the average voltage of the video signal changes according to the picture content. The other is applied to the AGC detector via the lowpass filter (LPF) and sync separator. The LPF filters the video signal and passes only the composite sync signal. The sync separator separates the horizontal sync (H. SYNC) signal from the composite sync signal. The AGC detector delays the H. SYNC signal to the back porch portion, sets the pulse width appropriately and produces a key pulse the voltage of which is determined to 85% white level, then the detector applies the key pulse to the video signal passing through the clamp circuit. Then, the AGC detector detects the peak-to-peak value of the video signal with the key pulse (between the 85% key pulse and sync tip) and charges capacitor C202 at pin 2 with the detected voltage to average it. The voltage charging C202 is applied to the AGC circuit to determine its gain.

The AGC circuit loop described here is the same as in conventional VTRs. However, the AGC circuit in "1000" series VTRs (VT-1100A/1400A) amplifies video signals with a low-luminance level by approx. 15% as shown in Fig. 4-24 to improve the S/N in the low luminance level (the video signal level is less than 1 Vp-p). To do this amplification, the white level of the key pulse is changed to 85% from 100%. Since this causes the control voltage of the AGC circuit to decrease by approx. 15%, the gain is raised by 15%.

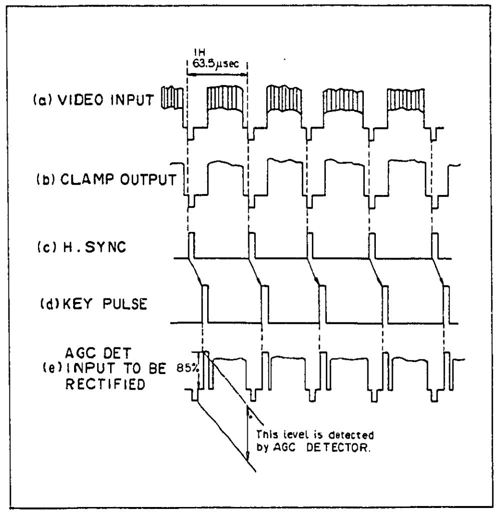


Fig. 4-23 AGC Detector Waveforms

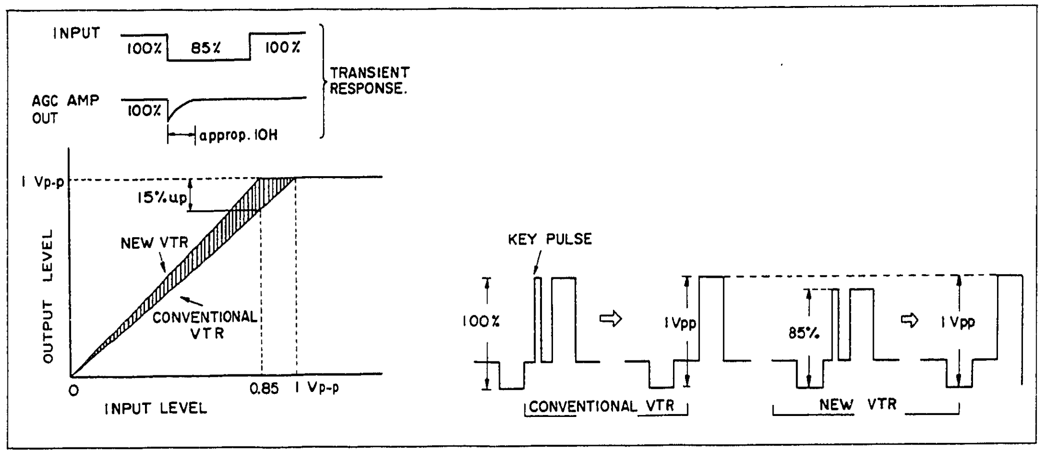


Fig. 4-24 AGC Characteristics

4) Luminance Separation Circuit (Fig. 4-25, 4-26)

This circuit separates the luminance signal using an LPF and comb filter (1H Delay Line). The signal at the AGC output (IC201 pin 27) with the luminance and chrominance components mixed is passed through two stages of the LPF and almost only the luminance signal is derived. However, since this luminance signal contains a little of the chroma component (approx. -15 dB), the remaining chroma is eliminated by the chroma canceler in the next stage. (See Fig. 4-26 for details.) The delay equalizer in Fig. 4-25 not only delays the signal to correspond to the delay in the chroma signal processing loop but compensates the phase chracteristics of the two LPFs. Fig. 4-26 shows the operation of the chroma canceler circuit. The input video signal (A) contains the mixed luminance and chroma components. (Actually, the chroma

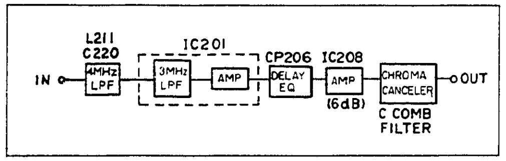


Fig. 4-25 Luminance Separation Circuit

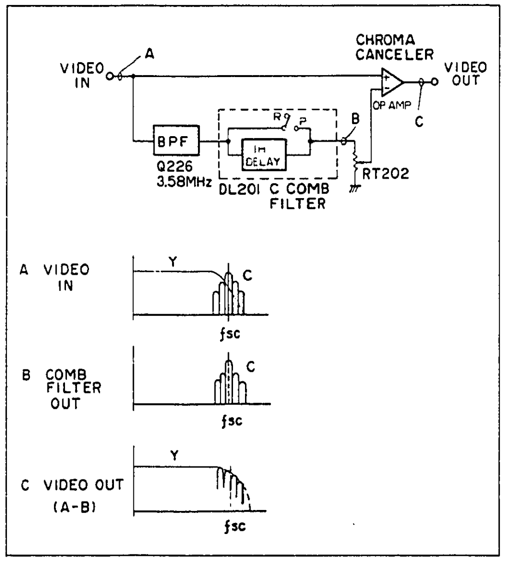


Fig. 4-26 Chroma Canceler Circuit

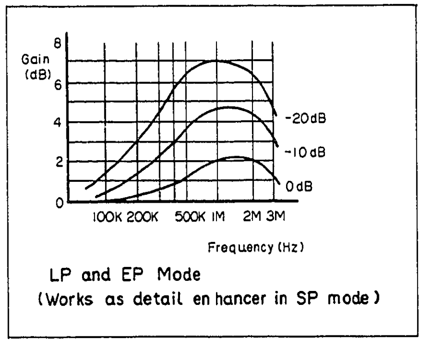
level is lower than the luminance level, but it is described at the same level as the luminance level so it can be seen more easily.)
The chroma signal (3.58 ±1 MHz) passing through the BPF enters C COMB filter DL201. The input signal is added to the signal passing through the 1H delay circuit. Only the chroma signal is derived at the comb filter output (B) and it is subtracted from the original signal at the operational amplifier (chroma canceler in IC201) and only the luminance signal after the chroma signal is eliminated appears at the output as shown by (C).
RT202 in the former stage of the chroma canceler is a variable resistor which balances the input level of OP AMP 2. The chroma canceler circuit acts the same as the 3.58 MHz trap in "60" series VTRs and before. This expands the frequency response of the luminance signal (approx. 3 dB up at 3 MHz) and reduces the crosstalk of the chroma signal more than in previous VTRs.

5) Sync Clamp Circuit

Since the DC component of the video signal is not supplied through capacitors, the sync tip level of a bright picture is not the same as the sync tip level of a dark picture. For the FM modulator, it is necessary to equalize the sync tip levels. This circuit equalizes the sync tip levels. The output of the clamp circuit is sent to the emphasis circuit.

6) Dynamic Preemphasis Circuit (Fig. 4-27)

The dynamic (nonlinear) preemphasis circuit performs the emphasis operation shown in Fig. 4-27 corresponding to the video signal input level and tape speed. This selection of the emphasis characteristic at each tape speed is performed by applying "SP Lo" to IC201 pin 10.
The output of the dynamic (nonlinear) emphasis circuit is supplied to the main preemphasis circuit.



LP and EP Mode
(Works as detail enhancer in SP mode)

Fig. 4-27 Dynamic Emphasis

7) Detail Enhancer

This circuit is the result of HQ technology and operates in place of dynamic emphasis in the SP mode. (See "VHS HQ SYSTEM" for details.)

8) Main Preemphasis Circuit (Fig. 4-28)

The dynamically emphasized luminance signal is now supplied to the main preemphasis circuit where the high-frequency components of the signal are boosted more than the low-frequency components. The frequency response for the preemphasis is shown in Fig. 4-28. The boosting action is required for the high-frequency components because in the FM recording system, the noise of the playback signal increases in proportion to the modulated signal frequency. In the playback process, the emphasized signal is deemphasized to resume the original signal. By the dynamic emphasis and the main preemphasis operation, the total S/N ratio increases.

The output of the main preemphasis circuit is supplied to the dark and white clip circuit.

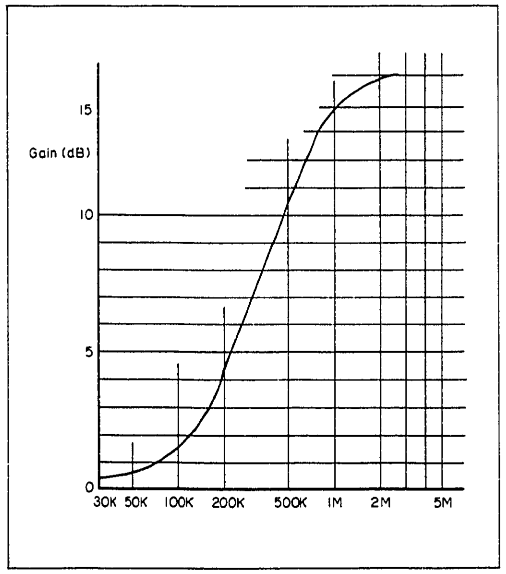


Fig. 4-28 Preemphasis

9) Dark and White Clip Circuit (Fig. 4-29)

After emphasis is performed, any unusually large overshoots and undershoots in the luminance signal are cut off at an specified level. This is done to avoid FM over-modulation. The overshoot levels are controlled by the white clip circuit and the undershoot levels are controlled by the dark clip circuit. Every clip level has been adjusted to the optimum value in IC201. The output of the dark and white clip circuit is supplied to the FM modulator circuit. The head switching pulse is added to this output to apply FM interleaving.

The white clip level is increased by approx. 20% by one HQ technology.

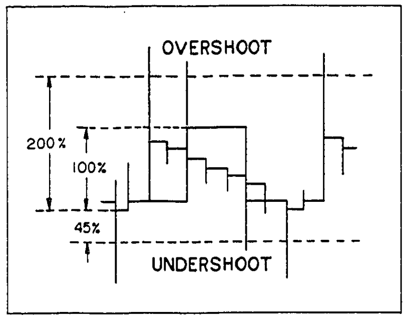


Fig. 4-29 Dark/White Clip

10) FM interleaving

The video signal of the adjacent channel is recorded overlapping the main channel. When recording/play is done as it is, beats occur between the main channel and adjacent channels, so CH1 is left as it is and only for CH2 the carrier frequency of the FM modulator is lowered by 1/2 fH. The head switching pulse (SW30) is applied to the video input main line of the FM modulator from the servo circuit via IC201 pin 15. By this, the carrier frequency drifts by 1/2 fH when SW30 is "Hi" (CH2).

11) FM Modulator Circuit (Fig. 4-30)

The actual device which constitutes the FM modulator is an astable multivibrator. This multivibrator generates a variable frequency square wave. The frequency of the square wave is governed by the level of the processed video signal at any given moment. Therefore, the processed signal varies the frequency of the square wave, which is frequency modulation, or FM.

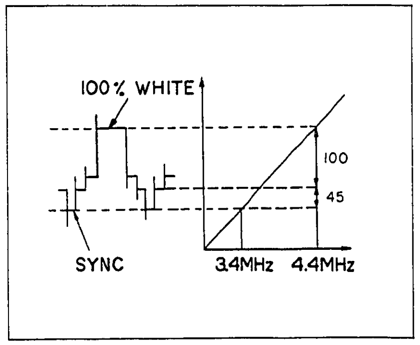


Fig. 4-30 FM Modulation

12) 1.4 MHz HPF Circuit (Fig. 4-31)

When the carrier of the FM modulator swings from 3.4 MHz to 4.4 MHz, sidebands are also produced.
The lower sideband extends down to (and below) 500 kHz. When recording the chroma signal, the lower FM sideband must be removed to prevent chroma beats during playback.

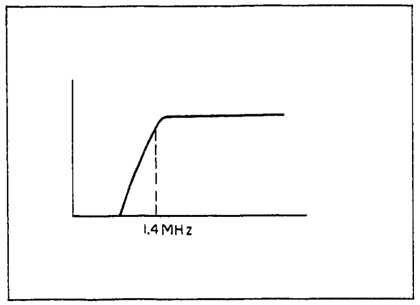


Fig. 4-31 Band Response of HPF

13) Y/C Mixer and Recording Amplifier (Fig. 4-32)

The FM-modulated luminance signal and the chroma signal, the frequency of which is down-converted (to 629 kHz) by the chroma processing circuit, are mixed by the Y/C mixer and the mixed signal is amplified by the recording amplifier to be the specified level and is then supplied to the video heads. Pin 20 of IC205 inhibits recording.
When pin 20 goes "Hi" (SQUELCH signal "Hi"), it stops the operation of the recording amplifier to inhibit recording. The SQUELCH signal is "Hi" during loading (for approx. 2.5 seconds), pause and phase match edit operation (for approx. 1.2 seconds).

Transistors Q2 and Q3 turn "on" receiving REC 9V in the record mode and ground one end of the winding of the video head (actually, the winding of the rotary transformer) via the resistor with low resistance (10 ohms).

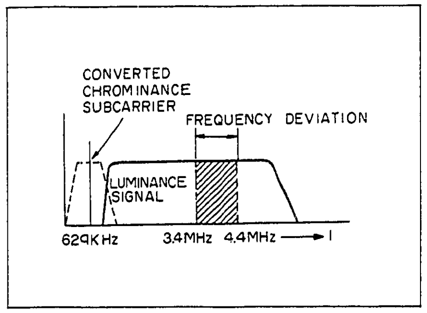


Fig. 4-32 Spectrum of FM Signal

14) Recording AGC Circuit (Fig. 4-32a)

The FM recording current flowing to the video heads must be aligned with the optimum recording current matching the characteristics of the video heads. In conventional VTRs (until "60" series VTRs), this was adjusted by an externally attached control, however, in "1000" series VTRs, by employing the recording AGC, no adjustment is required.

Fig. 4-32a shows the operation of this circuit. The FM signal enters IC205 via pin 22 and passes through the AGC amplifier (gain control amp), Y/C mixer and the recording amplifier and is then supplied to the video heads via pin 16. The voltage across resistor R5 (10 ohms) is changed by the recording current level. This change component is amplified by Q211 and enters IC205 via pin 8 and passes through the amplifier and OP AMP and is then fed back to the AGC amplifier. If the recording current is large, the voltage across R5 becomes high and the voltage at pin 8 is high. This lowers the gain of the AGC amplifier to control it so the recording current becomes constant.
IC205 pin 13 is the SYNC input which closes the switch only the sync signal is present to form an AGC loop. This eliminates the affect of fluctuations in the chroma signal which is superimposed in the Y/C mixer.
The output at pin 28 (CURRENT UP) of system control microprocessor IC901 is connected to pin 15 of IC205. This output increases the recording current for the time of overlap-recording on the tape (for approx. 3 seconds) and improves the picture quality (reduction of chroma beats) in the overlap-recorded section.

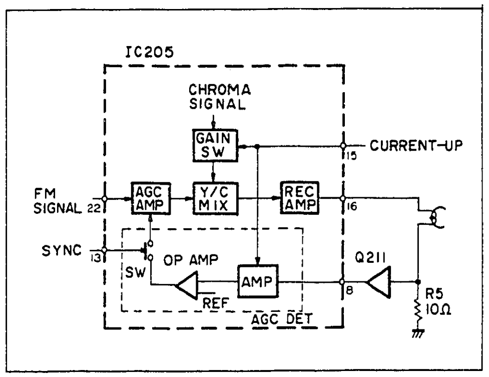


Fig. 4-32a Recording AGC Circuit

15) E-E Monitor Circuit

Part of the AGC output is derived from IC201 pin 8 as an E-E monitor signal. The monitor signal from pin

8 is supplied to IC205 pin 24 and is directly output at pin 27. This output is applied to pin 9 of IC201 and is clipped by the clip circuit so the white peak is 125% and is then amplified and output from pin 11 with the level of approx. 2 Vp-p. This output is converted by Q502 on the main P.C.B to low impedance and is applied to the video output jack and RF converter.

16) Luminance Filter (Fig. 4-33)

A new system is employed to comprise three filters in IC201 - a 3 MHz LPF, an LPF for sync separation and a 1.4 MHz HPF so no ajustment is required when manufacturing ICs in the factory.

It is very difficult to suppress variations in elements (resistance values of resistors and capacitances of capacitors) when manufacturing ICs. However, even though the variations of the absolute values are great, the variations of the relative values between the elements are small (this is called a high relative accuracy). Using this fact, a new system with three filters has been designed. The operation principle is shown in Fig. 4-33.

The input reference frequency (2fsc) signal is attenuated to a specified level by resistors Ra and Rb with high relative accuracy to become a reference level. This reference level and the output level of a quasi-filter consisting of integrated elements Rl and Cl are compared in the operational amplifier, and negative feedback is applied to the voltage applied to varicap Cl so both levels are aligned.

Meantime, using elements R2 - R4 and C2 - C4 which are related to the quasi-filter elements Rl and Cl with high-relative accurcy, the necessary filters are provided.

When variations occur in the values of the integrated elements (Rl/Cl) and this causes the quasi-filter output level to fluctuate between points A and C as shown in Fig. 4-33, the automatic adjustment function works to control the varicap Cl so point B can be obtained.

Since this control voltage applied to C2 - C4, the respective LPFs and HPF are adjusted to the required frequencies with high precision.

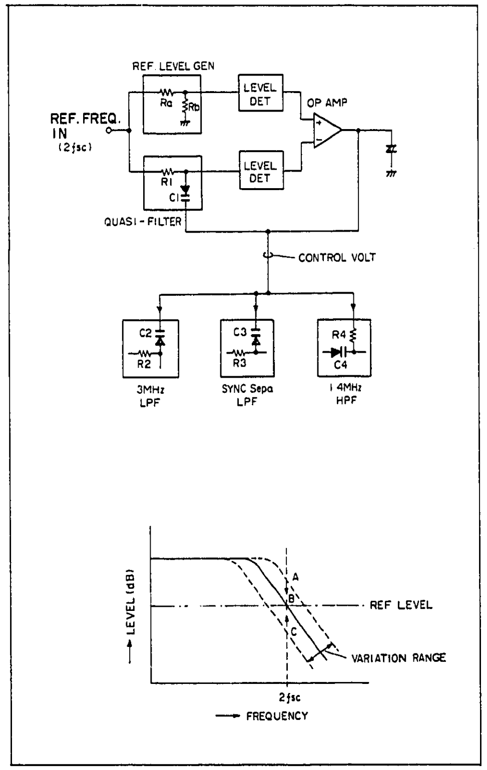

REF LEVEL GEN
Ra
Rb
LEVEL DET
OP AMP
REF. FREQ. IN (2fsc)
R1
C1
LEVEL DET
QUASI-FILTER
CONTROL VOLT
C2
R2
3MHz LPF
C3
R3
SYNC Sepa LPF
R4
C4
1.4MHz HPF
LEVEL (dB)
A
B
C
REF LEVEL
VARIATION RANGE
2fsc
FREQUENCY

Fig. 4-33 Filter Principle Diagram (Luminance)

(4) LUMINANCE PLAYBACK PROCESS (Fig. 4-37a)

1) General

The luminance playback loop consists of IC201 and IC205 at the center and IC204/IC207/IC208 on the luminance/chroma P.C.B and IC1 on the preamplifier P.C.B connected directly to the cylinder.

2) CH1 and CH2 Preamplifier Circuits

The Playback signals input to IC1 pins 12 and 14 are fed to the CH1 and CH2 preamplifier circuits. The preamplifier circuits feed back the output signal to the input side to make the characteristics flat. The conventional play equalization is performed via the 4.6 MHz peaking circuit (CP203) provided after the channel switch circuit.

Q1 is turned "on" by the PB 5V power source and grounds one end of the windings of the CH1 and CH2 video heads. The STILL head has the same azimuth as the CH2 head. The CH1 head is switched to the STILL head by the STILL signal input to pin 3 of IC1 in the still play mode.

3) Channel Switch Circuit

The channel switch circuit produces a continuous playback signal while switching the outputs of CH-1 and CH-2 preamplifier circuits using the head switching pulse (SW30).

The head switching pulse (SW30) generated in the servo circuit is supplied to the channel switch circuit via IC1 pin 4, and selects the output of CH-1 preamplifier which amplifies the video signal picked up by the CH-1 video head when the head switching pulse level is set to "Lo", and selects the output of the CH-2 preamplifier which amplifies the video signal picked up by the CH-2 video head when the pulse level is set to "Hi".

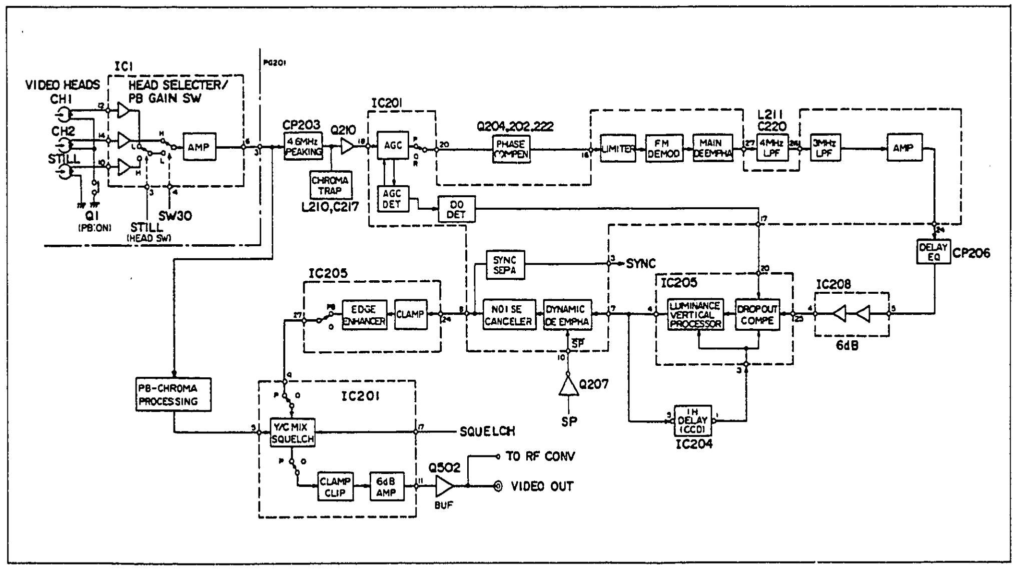

IC1
VIDEO HEADS
CH1
CH2
STILL
HEAD SELECTER/ PB GAIN SW
AMP
Q1 (PB:ON)
STILL (HEAD SW)
SW30
PG201
CP203 4.6MHz PEAKING
CHROMA TRAP
L210,C217
Q210
IC201
AGC
AGC DET
DO DET
Q204,202,222
PHASE COMPEN
LIMITER
FM DEMOD
MAIN DEEMPHA
L211 C220
4MHz LPF
3MHz LPF
AMP
DELAY EQ
CP206
SYNC SEPA
SYNC
IC205
EDGE ENHANCER
CLAMP
NOISE CANCELER
DYNAMIC DE EMPHA
SP
Q207
SP
IC205
LUMINANCE VERTICAL PROCESSOR
DROPOUT COMPE
IC208
6dB
1H DELAY (CCD)
IC204
PB-CHROMA PROCESSING
IC201
Y/C MIX SQUELCH
SQUELCH
CLAMP CLIP
6dB AMP
Q502
BUF
TO RF CONV
VIDEO OUT

Fig. 4-37a Simplified Luminance Playback Circuit

The output of the channel switch circuit is applied to the 4.6 MHz peaking circuit via amplifier and IC1 pin 6.

4) 4.6 MHz Peaking Circuit, Chroma Trap Circuit (Fig. 4-34)

The preamplifier circuit in the previous stage does not apply playback compensation to the signal and has flat characteristics, so the 4.6 MHz peaking circuit performs playback compensation. The playback characteristics of the video signal picked up by the CH-1 and CH-2 video heads are as shown by curve (A) in Fig. 4-34.

The characteristics of the preamplifier circuit are as shown by curve (B) and are flat. The characteristics of the 4.6 MHz peaking circuit (CP203) should be made as shown by curve (D) so that the integrated characteristics shown by curve (C) are obtained finally.

Components around the 4.6 MHz which is the upper limit of the FM carrier signal are boosted by the 4.6 MHz peaking circuit (CP203) to obtain the characteristics shown by curve (D).

The output of the 4.6 MHz peaking circuit is supplied to the AGC circuit via 629 kHz (chroma) trap, buffer and IC201 pin 18.

The 629 kHz (chroma) trap circuit (L210, C217) eliminates the 629 kHz playback chroma components.
Q210 is a buffer amplifier to change the impedance.

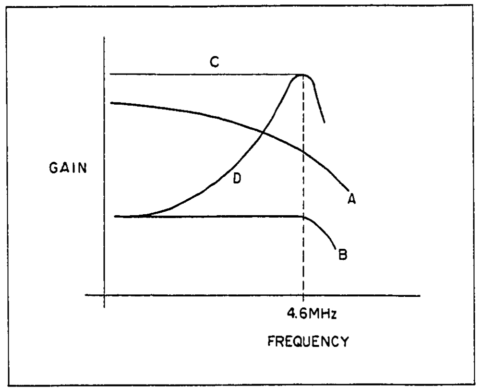


Fig. 4-34 Frequency Characteristics

5) AGC Circuit

The output from the 4.6 MHz peaking circuit is applied to the AGC amplifier stage where the RF output (FM) signals from the two video heads are automatically balanced.

One of the AGC circuit outputs is fed to the AGC detector circuit which detects signal level fluctuations. This is fed back to the AGC circuit to control so that the AGC circuit output is constant.

The AGC circuit output is derived from pin 20 of IC201 and is applied to the phase compensator circuit in the next stage. The other AGC circuit output is applied to the dropout detector circuit to detect missing of the FM signal due to dust or dirt on the tape, poor or irregular tape coating, etc. The detected output is derived from IC201 pin 17 which goes "Hi" when the FM signal is missing.

6) Phase Compensator Circuit (Q204, Q202, Q222)

The phase compensator circuit (Q204, Q202, Q222) corrects the phase distortion occurring in the 4.6 MHz peaking circuit (CP203) described previously.
The output of the phase compensator circuit is supplied to the FM demodulator circuit via IC201 pin 16 and highpass limiter circuit.

7) Limiter Circuit

The limiter circuit removes amplitude variations in the FM signal. The limiter also limits the amplitude of the FM signal after boosting the FM high-frequency components to prevent black and white from being inverted. That is, the FM carrier output level becomes smaller than the low-frequency sideband level in the high modulation section of the played back FM signal causing distortion; when it is demodulated via the FM demodulator as it is, black/white inversion occurs.
The limiter circuit prevents this.

8) FM Demodulator Circuit (Fig. 4-35)

This circuit uses the pulse delay system.
The FM demodulator circuit first converts the FM signal to a pulse the duty cycle of which is inversely proportional to the input FM signal frequency, that is, converts the FM signal to a pulse-width-modulated signal. Then the circuit smooths this PWM signal to demodulate the video signal.

The output of the FM demodulator circuit is applied to the main deemphasis circuit.

Fig. 4-35 shows the demodulator characteristics.

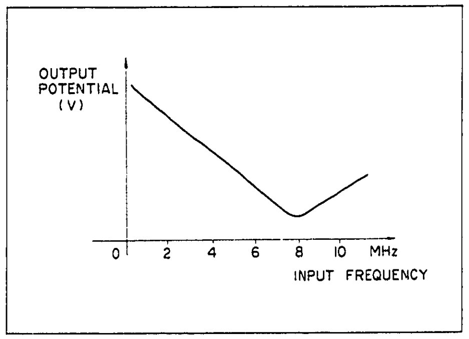


Fig. 4-35 Demodulator Characteristics

9) Main Deemphasis Circuit

The main deemphasis circuit attenuates the high frequency component, boosted by the main preemphasis circuit during recording, during play. That is, this circuit returns the high frequency component amplitude emphasized during recording to the original value.

The output from the main deemphasis circuit is sent to the 4 MHz LPF circuit via IC201 pin 27.

10) LPF Circuit, Delay Equalizer

The LPF circuit (4 MHz LPF + 3 MHz LPF) passes only the luminance signal of 3 MHz or less and the delay circuit (CP206) corrects the phase difference between the luminance signal and chroma signal.

The output of the AGC circuit also flows to this circuit during recording, and the same processing with the same characteristic is performed in the record and play modes.

11) Amplifier Circuit (IC208)

This circuit is between the output of delay equalizer and the dropout compensator circuit in the next stage and is an amplifier the gain of which is approx. 6 dB.

12) Dropout Compensator Circuit (Fig. 4-36)

This circuit compensates for missing parts of the FM signal due to dust or dirt on the tape, irregular tape coating, etc. and is used in common with the vertical processor circuit. Fig. 4-36 shows the dropout compensator circuit. (Compare this with Fig. 4-15 for easy understanding.)

The dropout detection output detected by IC201 is derived from pin 17 and is applied to pin 20 of IC205. The video signal input to pin 25 passes through SW1 and OP AMP 2 and is output from pin 4 normally. The 1H delay circuit (IC204) using a CCD is connected to the output at pin 4, and the output is fed back to pin 3 and is connected to the other terminal (b) of SW1. That is, the video signal 1H before the signal at terminal (a) is always supplied to the terminal (b). If missing parts of the FM signal (dropout) occur, IC205 pin 20 goes "Hi" and the contact of SW1 is switched to (b), so the output can be compensated by the signal 1H before while dropout occurs.

In conventional VTRs, dropout is compensated before FM demodulation, that is, in the FM signal stage. This dropout compensation system in the video signal circuit which is used from "1000" series VTRs can reduce switching noise.

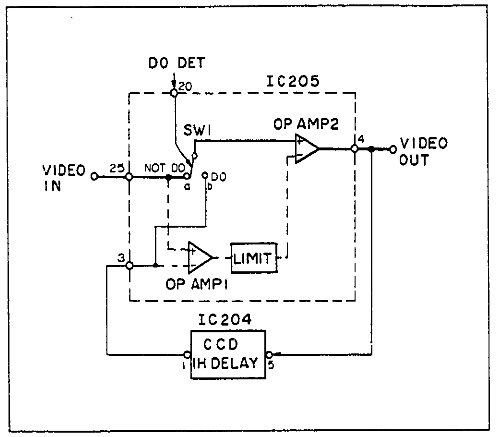


Fig. 4-36 Dropout Compensation Circuit

13) Luminance Vertical Processor

This circuit has been developed as one HQ technology to improve the S/N.

14) CCD 1H Delay Circuit (Fig. 4-36a)

This circuit consists of a hybrid IC in which a monolithic integrated circuit with 1H delay function using a CCD (Charge Coupled Device) and two externally attached LPFs. The clock frequency driving the monolithic IC is designed to be 2fsc.

The fsc (3.58 MHz), output from pin 41 of IC202, is applied to IC204 via pin 14 and is passed through the multiplier circuit (X2, 2fsc BPF) to produce 2fsc. This 2fsc is applied to the monolithic IC via the buffer amplifier to drive it.

Describing the signal flow, the video signal enters IC204 via pin 5 and is sampled at the period of 2fsc by the sampling circuit. The sampled pulse (455 bits per 1H) is 1H-delayed by the CCD in the next stage and is returned to an analog signal by the resampling circuit. CP204 is a lowpass filter which eliminates the clock frequency (2fsc). The LPF output is applied to pin 1 via the buffer amplifier.

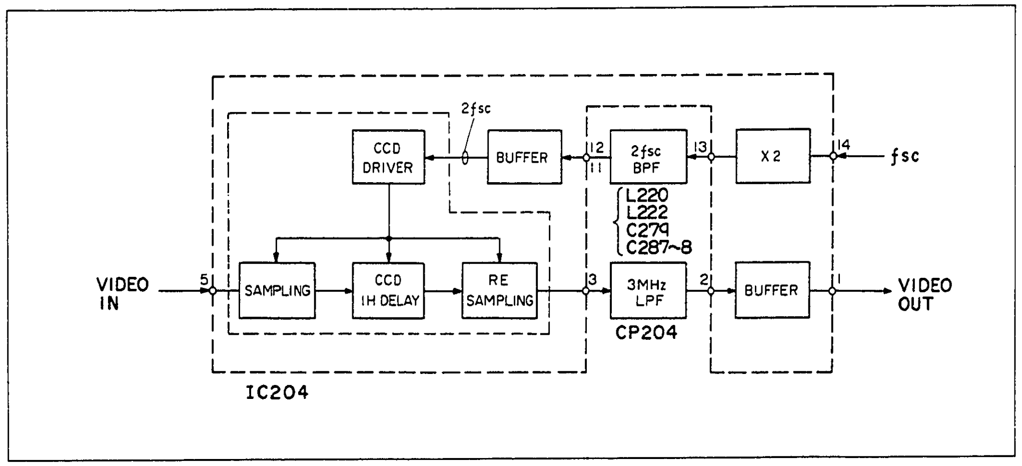


Fig. 4-36a CCD 1H Delay Circuit

15) Dynamic Deemphasis Circuit

This circuit forms a counterpart to the dynamic preemphasis circuit during recording. The characteristics are also reverse to those in recording. This circuit is activated by the $\overline{SP}$ signal at pin 10 of IC201.

16) Noise Cancel Circuit

The noise cancel circuit almost completely removes the high-frequency noise contained in the video signal which has passed through the dynamic deemphasis circuit.

The output of the noise cancel circuit is supplied to the clamp circuit via IC201 pin 8 and IC205 pin 24. The clamp circuit fixes the sync tip voltage of the video signal and applies it to the edge enhancer circuit in the next stage.

17) Edge Enhancer Circuit (Fig. 4-37)

This circuit emphasizes the edges of the picture and uses the second differential circuit as shown in Fig. 4-37.

The description assumes that a square wave as shown in (A) is applied to the input. The leading edge of the LPF output waveform is shallow as shown in (B). The other signal is supplied to the second differential circuit after its sync signal is eliminated. When the signal is differentiated once by the scond differential circuit, the differentiated waveform as shown in (C) is obtained and the signal is differentiated again, the second differentiated waveform appears as shown in (D). When this differentiated signal is controlled by the gain control circuit in the next stage to be set to the appropriate level and is subtracted from the signal (B) by the OP AMP, the waveform with its edges emphasized appears at the final output (E).
The gain of the gain control amplifier is controlled by the voltage at IC205 pin 23 to determine the amount of emphasis of the edges.

18) Y/C Mixer Circuit, Squelch Circuit

The Y/C mixer circuit mixes the luminance signal and the chroma signal supplied from IC201 pin 5. This circuit also has a squelch function.

The squelch circuit outputs a DC potential of which level is the same as sync-tip to black out the screen while pin 17 is "Hi". During loading, pin 17 is given a high potential, and the squelch circuit cuts the playback video signal.
In the trick play mode, when a positive pulse "ARTIFICIAL V.SYNC" of which pulse width is approx. 8H is applied to pin 17, the squelch circuit outputs the sync tip level potential to add the artificial V.sync to the playback video signal. The potential of pin 17 is supplied from the servo circuit.

The output of the Y/C mixer circuit is applied to the clamp circuit. The signal route thereafter is the same as that described in "LUMINANCE RECORDING PROCESS".

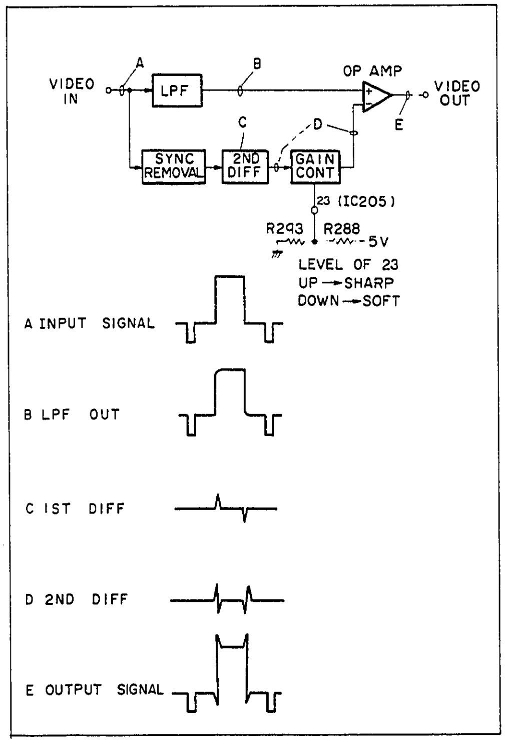

VIDEO IN
A
LPF
B
OP AMP
VIDEO OUT
C
D
E
SYNC REMOVAL
2ND DIFF
GAIN CONT
23 (IC205)
R293
R288
-5V
LEVEL OF 23
UP → SHARP
DOWN → SOFT
A INPUT SIGNAL
B LPF OUT
C 1ST DIFF
D 2ND DIFF
E OUTPUT SIGNAL

Fig. 4-37 Edge Enhancer

(5) CHROMINANCE RECORDING PROCESS
(Fig. 4-43a)

1) General

The chroma signal during recording is processed by IC202 in the luminance/chroma P.C.B. IC202 performs the chroma signal processing during play, the same as for the luminance signal, so it is required to switch over the signal routes. The switching command is given by the "PB5V" signal supplied via pin 18. This level is set to "Lo" during recording and the SW inside IC202 is set to the "PB" position and the signal route during recording is formed. Next, every circuit operation is described in order of the signal route as follows.

2) PB/$\overline{PB}$ SW

The video signal fed from the video input jack is supplied to the PB/$\overline{PB}$ switch via IC202 pin 25. The route from the 3.58 MHz BPF circuit (CP202) until the ACC circuit in IC202 is commonly used for recording and play, so the PB/$\overline{PB}$ SW circuit selects the signal input to this circuit. The PB/$\overline{PB}$ SW circuit is controlled by the PB5V signal fed from pin 18; this signal is set to "Lo" during recording, and the video signal at pin 25 is supplied to the 3.58 MHz PBF circuit via the PB/$\overline{PB}$ SW circuit and pin 23.

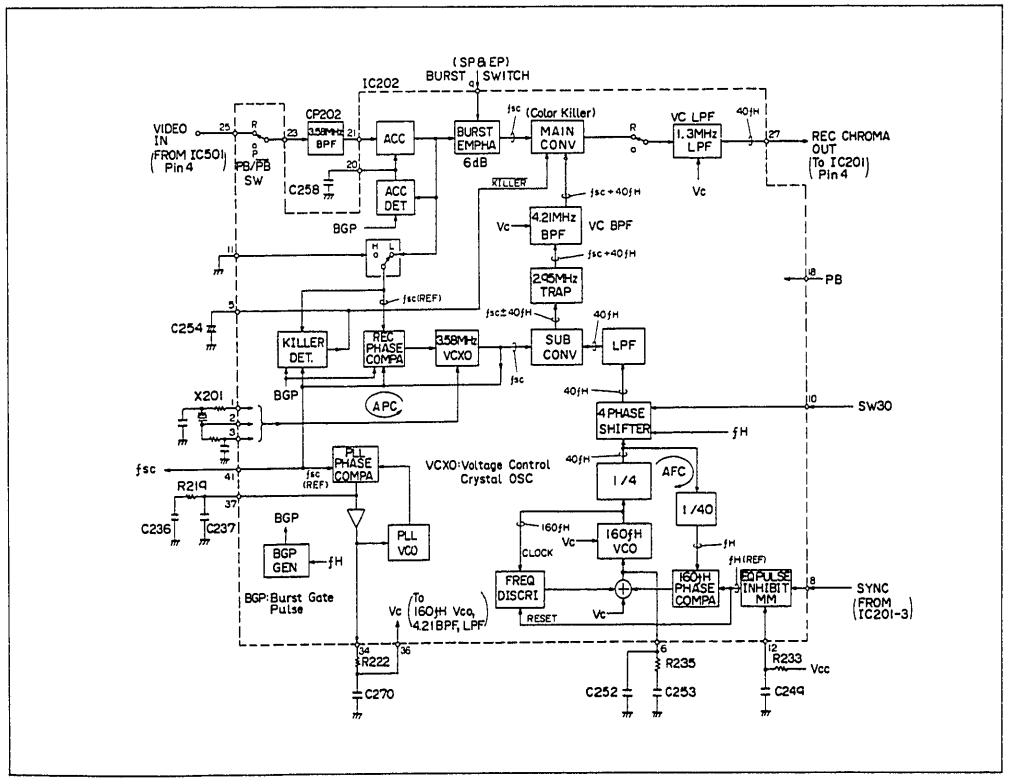

(SP&EP)
BURST SWITCH
IC202
VIDEO IN (FROM IC501 Pin 4)
25
R
P
PB/PB SW
23
CP202
3.58MHz BPF
21
20
C258
ACC
ACC DET
BGP
BURST EMPHA
6dB
fsc
(Color Killer)
MAIN CONV
KILLER
fsc+40fH
R
VC LPF
1.3MHz LPF
Vc
40fH
27
REC CHROMA OUT (To IC201 Pin 4)
4.21MHz BPF
VC BPF
2.95MHz TRAP
fsc±40fH
SUB CONV
LPF
11
H
L
fsc(REF)
5
C254
KILLER DET.
REC PHASE COMPA
3.58MHz VCXO
18
PB
X201
1
2
3
APC
4 PHASE SHIFTER
10
SW30
fH
PLL PHASE COMPA
fsc
41
fsc (REF)
R219
37
C236
C237
VCXO: Voltage Control Crystal OSC
1/4
AFC
1/40
PLL VCO
BGP GEN
160fH
CLOCK
160fH VCO
FREQ DISCRI
RESET
160fH PHASE COMPA
fH(REF)
EQPULSE INHIBIT MM
8
SYNC (FROM IC201-3)
BGP: Burst Gate Pulse
Vc (To 160fH Vco, 4.21BPF, LPF)
34
36
R222
C270
6
R235
C252
C253
12
R233
Vcc
C249

Fig. 4-43a Simplified Chrominance Record Circuit

3) 3.58 MHz Bandpass Filter Circuit

The 3.58 MHz bandpass filter circuit (CP202) selects only the chroma frequency band (3.58 MHz ± 500 kHz) from the input video signal and passes it.

The output of the BPF circuit is supplied to the ACC circuit via IC202 pin 21.

4) ACC (Automatic Color Gain Control) Circuit (Fig. 4-38)

The ACC circuit controls the output level to a constant value regardless of fluctuations of the chroma signal input level.

This control system is the burst ACC system. First, the ACC circuit output is supplied to the ACC detector circuit. Then the ACC detector circuit receives the burst gate pulse. The ACC detector circuit extracts the chroma burst signal by means of these 2 signals and detects the burst signal level. This charges C258 connected to pin 20 and is averaged. This voltage is fed back to the ACC circuit, and by this, the gain is controlled so that the output voltage of the ACC circuit is constant.

The output of the ACC circuit is fed to the burst preemphasis circuit.

The H.SYNC gate eliminates the equalizing pulse contained in the H.SYNC signal sent from IC202 pin 8, and triggers the burst gate pulse generator every 1H. The burst gate pulse is delayed from the H.SYNC signal so that only the burst signal is gated from the chroma signal, and moreover, it is provided with the pulse width of the burst signal period. (Refer to Fig. 4-38)

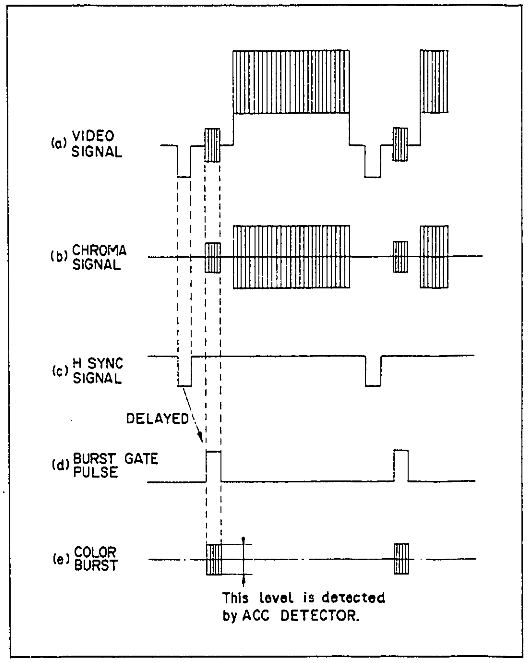


Fig. 4-38 ACC

5) Burst Preemphasis Circuit (Fig. 4-39)

The burst preemphasis circuit amplifies only the chroma burst signal by 6 dB using the burst gate pulse in the SP and EP modes. IC202 pin 9 is "Lo" in the LP mode, the burst gate pulse switch is "off" and the burst preemphasis function does not work. The output of the burst preemphasis circuit is transmitted to the record main converter circuit in the next stage.

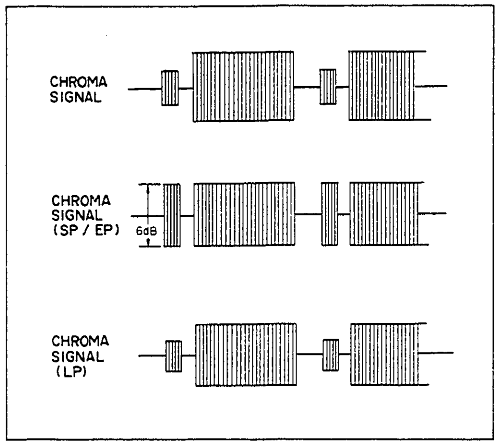


Fig. 4-39 Burst Preemphasis

6) Record Main Converter Circuit (Fig. 4-40)

The purpose of this record main converter is to produce a 629 kHz chroma signal with phase rotation.

This means that the second input to this main converter must have phase rotation, and must be such a frequency that the difference between the two input frequencies is the desired output frequency. Therefore, the second input is a 4.21 MHz rotational signal. The 4.21 MHz signal is a continuous sinewave signal which is phase-locked to the input horizontal sync.

The 4.21 MHz signal will change its phase by 90° every time a new horizontal sync signal is received. Because one of the inputs to the main converter has a phase rotational characteristic, the output signal will also have the same characteristic.
The output contains two bands of information. It contains the sum and difference frequency components of the two input signal frequencies.
The sum is the 7.8 MHz rotational chroma signal.
The difference is the necessary 629 kHz rotational chroma signal.
The output of the record main converter circuit is fed to the 1.3 MHz LPF in the next stage.

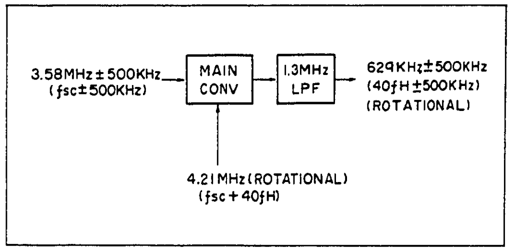

3.58MHz±500KHz (fsc±500KHz)
MAIN CONV
1.3MHz LPF
629KHz±500KHz (40fH±500KHz) (ROTATIONAL)
4.21MHz(ROTATIONAL) (fsc+40fH)

Fig. 4-40 Record Main Converter

7) Color Killer Detector Circuit

The killer detector circuit controls the record color killer so that the chroma signal is allowed to pass only when the chroma burst signal is contained in the video signal. The presence/absence of the chroma burst signal is detected by the color killer detector circuit. The color killer detector circuit inputs the following 3 signals and performs sync-detection to detect presence/absence of the chroma burst signal.

(1) Chroma signal:
This signal is supplied from the input side of the burst preemphasis circuit.

(2) Burst gate pulse:
This signal is produced in the burst gate pulse generator.

(3) 3.58 MHz signal:
This signal is supplied from the 3.58 MHz VCXO (Voltage Controlled Crystal Oscillator) and sync-detected with the chroma burst signal to detect the presence/absence of the burst signal.

The output of the killer detector circuit charges C254 connected to pin 5 where it is averaged and supplied to the record main converter (has a color killer function); this level is set to "Lo" when the chroma burst signal is present, and to "Hi" when the chroma burst signal is not present.

8) 1.3 MHz Lowpass Filter Circuit

The 1.3 MHz LPF circuit cuts off the sum component - 7.8 MHz rotational chroma signal - from the output of the record main converter circuit and selects only the difference component - 629 kHz rotational chroma signal - and passes it.

The output of the LPF is applied to the Y/C mixer circuit via IC205 pin 18 and mixed with the luminance signal. The signal route thereafter is the same as described in the item, "LUMINANCE RECORDING PROCESS".

9) Derivation of 4.21 MHz Rotational Signal

The 4.21 MHz rotational signal is generated in IC202. Since the 4.21 MHz signal is phase-locked to the incoming video signal, two comparator circuits, AFC and APC, are used as phase-locked loops. In brief, the AFC circuit produces a 160 fH (2.571 MHz) signal which is counted down and converted to a 629 kHz rotational signal. The APC circuit generates a 3.58 MHz signal which, when multiplied by the 629 kHz rotational signal inside a 4.21 MHz sub converter, will produce the desired 4.21 MHz rotational signal. This simplified description can be seen below. The AFC circuit locks to the incoming horizontal sync signal, and produces a 160 fH output signal. This signal is supplied to the 1/4 divider and then to the 4 phase shifter circuit which produces a 629 kHz rotational signal.

Again, "rotational" indicates a phase change of 90° per horizontal line. The APC circuit locks to the incoming burst signal and produces a continuous 3.58 MHz output signal. The 629 kHz rotational signal and the 3.58 MHz signal are combined in 4.21 MHz sub converter, and the output is a 4.21 MHz rotational signal. This 4.21 MHz rotational signal is the signal that is used in record main converter inside of IC202.

10) Recording AFC Circuit

The REC. AFC is composed of mainly the 160 fH VCO circuit, 1/4 divider, 1/40 divider and the record 160 fH phase comparator circuit. The 1/4 and 1/40 dividers divide the 2.517 MHz signal generated by the 160 fH VCO down to 15.734 kHz. The 15.734 kHz signal is supplied to the 160 fH phase comparator circuit.

The other input to the record 160 fH phase comparator is the H.SYNC pulse which is derived from the incoming video signal. Therefore, the 629 kHz signal is phase locked to the incoming video signal. The output of the record 160 fH phase comparator circuit is charged to C252/C253 connected to pin 6 and is averaged. Then this DC voltage is fed back to the 160 fH VCO circuit.

If the fH signal from the counted down 629 kHz signal does not phase-match the incoming horizontal sync, an error voltage will be generated and applied to the VCO so that phase matching does occur.

When the 160 fH VCO is providing the proper phase-locked 2.517 MHz signal, the 4 phase shifter outputs the 629 kHz rotational signal.

11) 4 Phase Shifter (Fig. 4-41, 4-42)

The 1/4 divider circuit divides the 160 fH (2.517 MHz) by 4 and supplies four 629 kHz pulses with different phases to the 4-phase shifter. The 4-phase shifter generates the phases rotational 629 kHz using 629 kHz signals and 4 enabling signals.
Fig. 4-41 is the equivalent block diagram of the 4-phase shifter.
The AND gates are fired in order to provide a phase rotating output.
The enabling signals can be obtained by applying the H.sync pulse selected by the H.sync gate circuit to the ring counter. The phases of the enabling signals are changed by the level of the SW30Hz signal applied via pin 10. Fig. 4-42 shows the phases of the enabling signals.

For the first field for video head "CH1" the firing order of gates is 1-2-3-4. This provides the desired 0°, 90°, 180°, 270°, etc. rotation.

For the second field for video head "CH2", the order is 1-4-3-2. This gives a 0°, 270°, 180°, 90° rotation, which is the same thing as 0°, minus 90°, minus 180°, minus 270° rotation, which is desired.

When the SW30 signal is set to "Lo", the 629 kHz signal with the phase 90° advanced every cycle of the fH signal is selected and when the SW30 signal is set to "Hi", the 629 kHz signal with the phase 90° delayed every cycle of the fH signal is selected. This control is processed digitally.

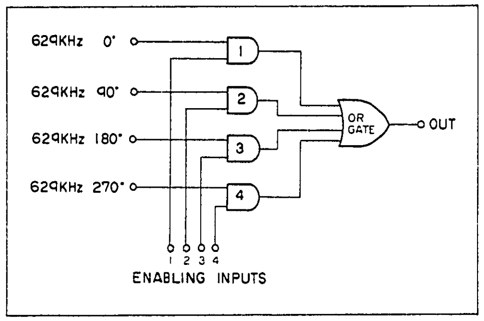


Fig. 4-41 4-Phase Shifter

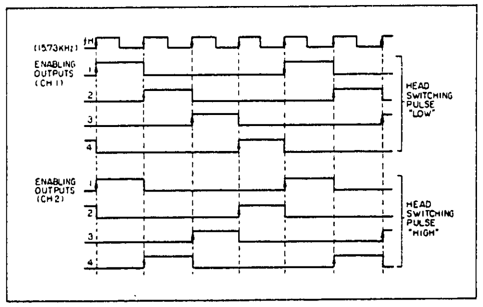


Fig. 4-42 Enabling for 4-Phase Shifter Gates

12) 3.58 MHz Generator

The 3.58 MHz GEN mainly consists of the 3.58 MHz VCXO and the record 3.58 MHz phase comparator. When recording, this circuit derives the chroma burst signal and locks the oscillation frequency of the 3.58 MHz VXCO to the frequency of this derived burst signal, then applies this output to the 4.21 MHz sub converter and the color killer detector circuits.

The 3.58 MHz VCXO circuit generates the 3.58 MHz signal while synchronized with the chroma burst signal.
The record 3.58 MHz phase comparator circuit inputs the following 3 signals and locks the 3.58 MHz VXCO oscillation frequency to the chroma burst signal frequency.

(1) 3.58 MHz signal:
This signal is supplied from the 3.58 MHz VCXO circuit.

(2) Chroma burst signal:
This signal is derived from the chroma signal output from the burst preemphasis circuit described previously using the burst gate signal.

(3) Burst gate pulse:
This signal is produced in the burst gate pulse generator.

The output of the phase comparator circuit charges C235 connected to pin 38 and is fed back to the 3.58 MHz VCXO circuit.

13) Chrominance Filter (Fig. 4-43)

These three circuits, 160fH VCO, 4.21 MHz BPF and 1.3 MHz LPF, in IC202 operate using a PLL VCO as a link so no adjustment is required when manufacturing ICs.

a) Using the 3.58 MHz VCXO output signal fsc as a reference signal and the PLL VCO output signal (3.58 MHz) as a comparison signal, both phases are compared by the PLL phase comparator and the error signal is fed back to the PLL VCO via the LPF and DC amplifier.

b) The feedback voltage (PLL control voltage) is reapplied via pin 36 to IC202 through the externally attached LPF. (Control voltage Vc)

c) This control voltage is applied to the VCO, LPF and the variable capacitor which determines the frequency of the LPF and the frequencies of the respective circuits are determined as 160 fH, 4.21 MHz and 1.3 MHz.

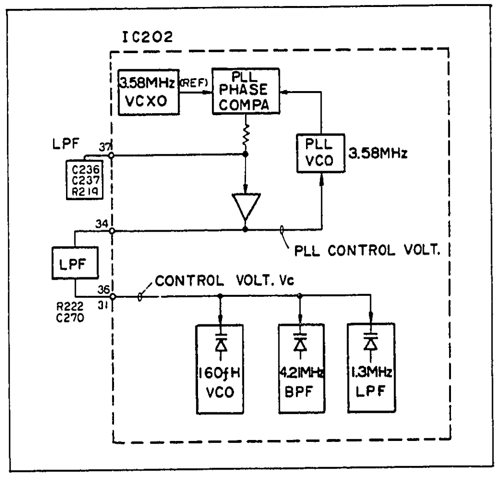

IC202
3.58MHz VCXO
(REF)
PLL PHASE COMPA
PLL VCO
3.58MHz
LPF
37
C236 C237 R219
34
LPF
36
31
R222 C270
PLL CONTROL VOLT.
CONTROL VOLT. Vc
160fH VCO
4.21MHz BPF
1.3MHz LPF

Fig. 4-43 Filter Principle Diagram (Chrominance)

(6) CHROMINANCE PLAYBACK PROCESS (Fig. 4-44a)

1) General

The chroma signal during playback is processed in IC202, the same as in recording. The "PB5V" signal goes "Hi" during play and this sets IC202 pin 18 to "Hi", so all switches in IC202 are changed over to the "PLAY" positions and the playback signal is routed as follows.

2) 1.3 MHz LPF Circuit

The chroma signal during playback is derived from the channel switch circuit output at IC1 pin 6 and fed to the 1.3 MHz LPF circuit.

The 1.3 MHz LPF circuit selects the chroma signal (629 kHz ± 500 kHz) mixed in the luminance FM signal and let it pass.

L297 and C290 connected to pin 28 form a trap tuned to approx. 1.5 MHz. This trap prevents the sideband of the luminance signal from entering the chroma frequency band.

L215 and C241 connected to IC202 pin 28 compose a 70 kHz audio bias trap. This eliminates the audio bias induced in the video heads in the audio dub mode. (This block is not provided in VT-1100A/1105A.)

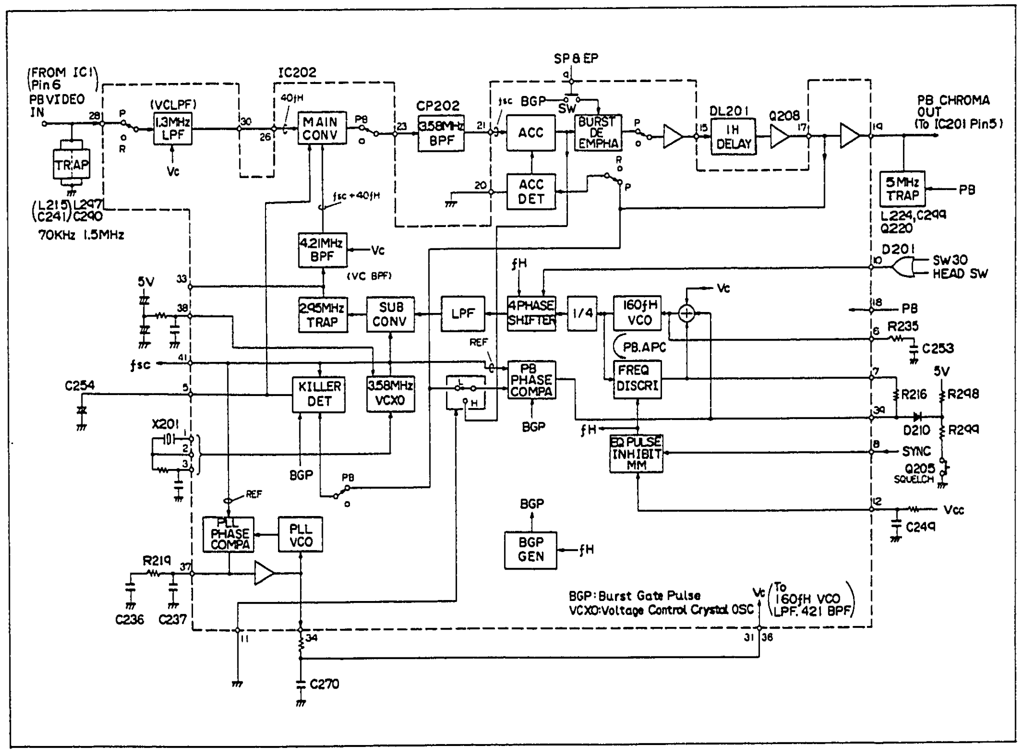

(FROM IC1 Pin6)
PBVIDEO IN
TRAP
(L215 L297 / C241 C290)
70KHz 1.5MHz
(VCLPF)
1.3MHz LPF
Vc
IC202
40fH
MAIN CONV
CP202
3.58MHz BPF
SP & EP
fsc BGP
SW
ACC
BURST DE EMPHA
ACC DET
DL201
1H DELAY
Q208
PB CHROMA OUT (To IC201 Pin5)
5MHz TRAP
PB
L224,C299 Q220
D201
SW30 HEAD SW
fsc+40fH
4.21MHz BPF
(VC BPF)
2.95MHz TRAP
SUB CONV
LPF
4PHASE SHIFTER
1/4
160fH VCO
PB.APC
FREQ DISCRI
PB PHASE COMPA
REF
KILLER DET
3.58MHz VCXO
fH
BGP
EQ PULSE INHIBIT MM
5V
fsc
C254
X201
PLL PHASE COMPA
PLL VCO
R219
C236 C237
C270
BGP GEN
R235
C253
R216
R298
D210
R299
SYNC
Q205 SQUELCH
Vcc
C249
BGP:Burst Gate Pulse
VCXO:Voltage Control Crystal OSC
Vc (To 160fH VCO LPF.421 BPF)

Fig. 4-44a Simplified Chrominance Playback Circuit

3) Playback Main Converter Circuit

Playback main converter converts the 629 kHz rotational unstable chroma signal from the tape to a 3.58 MHz non-rotational stable signal.

As it was explained in the general section, the two inputs to the modulator are the 629 kHz signal and a 4.21 MHz signal which has the same instability and rotation as the 629 kHz signal.

It is important that the rotation of the 4.21 MHz signal is the same direction as the 629 kHz playback chroma signal.

To obtain the 3.58 MHz non-rotational stable signal, the same direction rotational signal is mixed with the rotational chroma signal.

For this reason, after frequency conversion with the playback main converter, the subtracted signal is selected by the 4.21 MHz bandpass filter. Subtraction is performed between the 4.21 MHz and 629 kHz signals in terms of phase and frequency, so the rotation and delta factor which causes frequency fluctuations in the playback chroma signal are cancelled.

The output of the playback main converter circuit is applied to the 3.58 MHz bandpass filter circuit (CP202) via IC202 pin 23.

4) 3.58 MHz Bandpass Filter Circuit (CP202)

The 3.58 MHz BPF circuit (CP202) selects the difference component which is the chroma signal (3.58 MHz ± 500 kHz) from the output signal ((629 kHz ± 500 kHz ±Δ) ± (3.58 MHz + 629 kHz ±Δ)) of the playback main converter in the previous stage and lets it pass.

The output of the 3.58 MHz BPF circuit is applied to the ACC circuit via IC202 pin 21.

5) ACC Circuit

The role and basic operation of the ACC circuit are the same as in the record mode. The output of the ACC circuit is applied to the Burst Deemphasis circuit.

6) Burst Deemphasis Circuit

The chroma burst signal is emphasized by 6 dB in the SP and EP modes (not in the LP mode) during recording, so the burst deemphasis circuit halves the playback burst amplitude to demodulate the original amplitude.
In the SP and EP modes being applied with a high potential via pin 9, the switch turns "on" and applies the burst gate pulse to the burst deemphasis circuit. With the burst gate pulse given, the burst deemphasis circuit reduces the burst amplitude to half. In the LP mode the burst deemphasis circuit operates as an ordinary amplifier because pin 9 is "Lo", the switch is "off" and burst gate pulse is not applied to the burst deemphasis circuit.

The output of the burst deemphasis circuit is applied to the 1H Delay circuit via IC202 pin 15.

7) 1H Delay Line Filter circuit (Fig. 4-44)

In order to greatly reduce the chroma crosstalk which can occur during playback (especially in LP and EP modes), a 1H delay line filter is used.

The purpose of the 1H delay line filter is to add together the delayed and undelayed chroma signals, which doubles the desired chroma signal and eliminates the crosstalk.

The output of the 1H delay line filter circuit is applied to the Buffer amplifier circuit via IC202 pin 17 and to ACC detector circuit and color killer detector circuit.

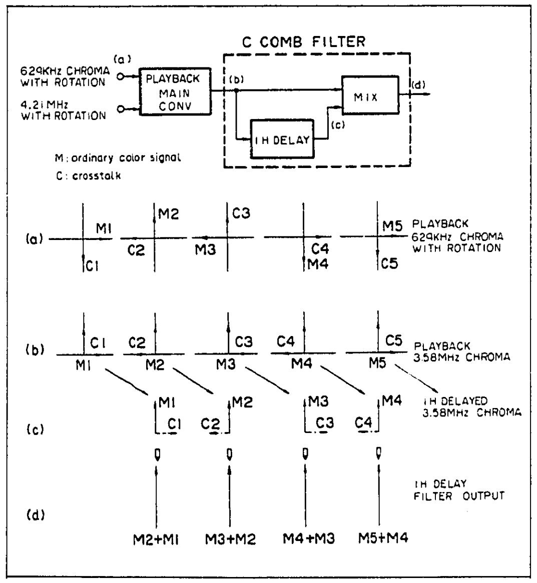


Fig. 4-44 Color Crosstalk Cancellation

8) 3.58 MHz VCXO

The oscillation frequency of this 3.58 MHz VCXO is synchronized with the burst signal in the video signal during recording. During playback, the 3.58 MHz VCXO generates a signal with a frequency determined by the crystal oscillator connected to pins 1 and 2, in the free-run mode.
The frequency of the chroma burst signal during playback is aligned with the oscillation frequency of this 3.58 MHz VCXO.

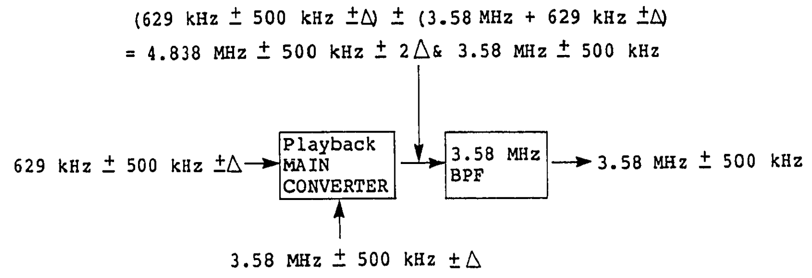
Frequency fluctuations of the chroma burst signal caused by jitter, etc. during playback are detected using the output frequency of the 3.58 MHz generator and removed in PB main converter.

9) 40 fH Generator

The role and basic operation of the 40 fH GEN are similar to those in recording, but the 160 fH VCO phase control loop differs from that in recording.

(a) 160 fH VCO control loop

The comparator output, obtained by comparing the 3.58 MHz VCXO phase with the chroma burst signal supplied from the 1H delay line circuit, is applied to the 160 fH VCO circuit. The 160 fH VCO oscillates to produce a frequency which contains same frequency fluctuations as those in the burst signal (±Δ), and supplies it to the playback main converter via 1/4 divider, 4-phase shifter, 4.21 MHz sub converter, 4.21 MHz BPF and cancels frequency fluctuations (±Δ) of the chroma signal caused by jitter, etc.


(629 kHz ± 500 kHz ±Δ) ± (3.58 MHz + 629 kHz ±Δ)
= 4.838 MHz ± 500 kHz ± 2Δ& 3.58 MHz ± 500 kHz
629 kHz ± 500 kHz ±Δ
Playback MAIN CONVERTER
3.58 MHz BPF
3.58 MHz ± 500 kHz
3.58 MHz ± 500 kHz ±Δ

(b) Frequency discriminator

The 160 fH VCO is controlled by the frequency discriminator as well as the PB APC phase comparator output in the play mode to remove the PB 3.58 MHz chroma frequency fluctuation. The 160 fH VCO has a wide variation range. The frequency may be drifted greatly from 2.52 MHz during transients such as when power is supplied. The frequency discriminator operates to set the frequency of the 160 fH VCO correctly to 2.52 MHz at this time. The frequency discriminator outputs until it is locked to the correct frequency (160 fH). The frequency discrimination is performed digitally for precision. When the 160 fH VCO oscillates at 160 fH correctly, the number of pulses output from the VCO in the 1H period is set to exactly 160. For example, when it oscillates at 164 fH, the number of the pulses is 164 increasing by 4. The oscillation frequency can be found correctly by counting the number of the pulses of the VCO for 1H period. The 1H period is the repetition period of the horizontal sync pulse itself, so it can be set very precisely.

Actually, the frequency discriminator discriminates the frequency variation when the frequency has deviated by more than +1/2 fH. The pulse count is done for the 4H period to discriminate the +1/2 fH deviation. For that purpose, the frequency discriminator output is applied to the 160 fH VCO to increase the frequency of the 160 fH VCO when the number of the pulses in the 4H period is 638 or less and to decrease the frequency of the 160 fH VCO when the number of pulses is 642 or more (160 x 4 = 640). The frequency discriminator is not shown in the schematic diagram because the schematic becomes complicated.

4-2-5 RF Converter/Output Selector

Fig. 4-10(h) is a simplified diagram of the RF converter /output selector circuits. These circuits are housed in one shielded case. The RF converter IC1 becomes active when the VTR5V B+ (produced by the TV/$\overline{\text{VTR}}$ mode setting output at pin 12 of T-μP and switch Q503: Not shown) is applied to the B+ input at pin 8 and generates the picture-RF signals (fp), AM-RF converts the video signal and FM-RF converts the audio signal. The fp signal has two frequencies aligned with channels 3 and 4 (61.25 MHz: Channel 3, 67.25 MHz: Channel 4), one of the frequencies can be selected by the operator. The fp signal is generated by the dual resonator (SAW) resonating with frequencies 61.25 MHz and 67.25 MHz and the fp oscillator in the IC. The 61.25 MHz resonator output of the SAW is applied to IC1 pin 9 and the 67.25 MHz resonator output is applied to pin 10. One of fp signals is selected by the RF channel setting voltage at pin 7 of IC1. The voltage at pin 7 is the RF channel switch input. When channel 3 is selected, pin 7 goes "Hi" and the resonant frequency at pin 9 is selected, and when channel 4 is selected, pin 7 goes "Lo" and the frequency at pin 10 is selected, then the selected frequency signal is connected to the fp oscillator.

The fp oscillator generates the fp signal corresponding to the selected channel and applies the output to the video amplitude modulator and FM audio RF mixer. The video signal from the video processing

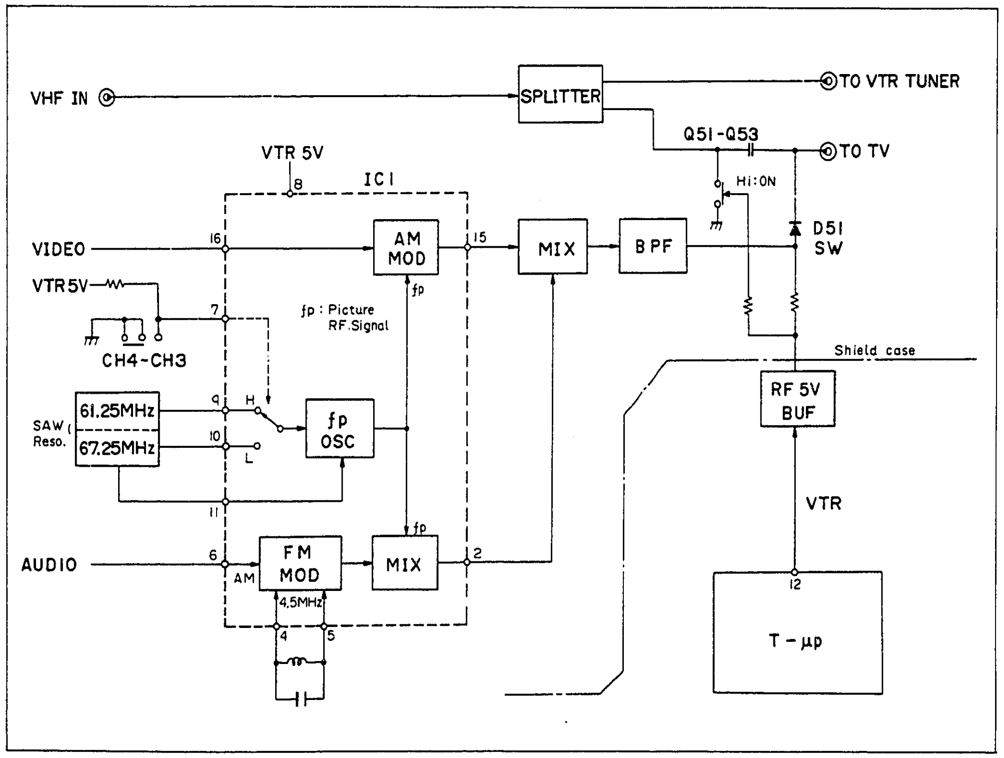

VHF IN
SPLITTER
TO VTR TUNER
Q51-Q53
TO TV
Hi:ON
VTR 5V
8
IC1
VIDEO
16
AM MOD
15
MIX
BPF
D51 SW
VTR5V
7
fp
fp : Picture RF.Signal
CH4-CH3
Shield case
SAW Reso.
61.25MHz
67.25MHz
9
10
H
L
fp OSC
RF 5V BUF
11
VTR
AUDIO
6
AM
FM MOD
fp
MIX
2
12
4.5MHz
4
5
T-μp

Fig. 4-10(h) Simplified RF Converter/Output Selector Circuit Diagram

circuit is supplied to the video amplitude modulator in IC1 via the video input at pin 16 and modulates the fp signal. The AM-RF converted video signal is output at pin 15 and is supplied to the video/audio mixer.

The audio signal from the audio processing circuit is supplied to the 4.5 MHz frequency modulator in IC1 via pin 6. The 4.5 MHz frequency modulator generates an audio signal with its frequency modulated in proportion to the amplitude of the audio signal centering the resonant frequency of the 4.5 MHz resonator circuit connected to pins 4 and 5, and applies the output to the audio RF mixer. The audio RF mixer mixes the previously described picture RF carrier signal and 4.5 MHz FM audio signal and outputs the resultant signal at pin 2. The FM-RF audio signal at pin 2 is supplied to the video/audio RF mixer. The video/audio RF mixer mixes the AM-RF video signal and FM-RF audio signal. The mixed channel 3 or 4 RF signal component is passed through the bandpass filter (BPF), set to the frequency of the channel 3 or 4 signal component, and switching diode D51 and is supplied to the VHF RF output. The VHF RF output also receives the antenna RF signal input from the VHF antenna input terminal. When the VTR/TV switch is set to "VTR", since the switching transistors and diode Q51 - Q53 and D51 are turned "on" by the VTR5V B+, the antenna RF signal is grounded via Q51 - Q53 and the RF signal from the RF converter is supplied to the VHF RF output via D51. When the VTR/TV switch is set to "TV" mode, since D51 and Q51 - Q53 turn "off", the antenna RF signal is supplied to the VHF RF output and the RF signal from the RF converter is interrupted by D51. The output at the VHF RF output terminal is applied to the monitor TV.

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5. MECHANISM DESCRIPTION

1. Overview

The basic operations and locations of components of the chassis used in "1000" series VTRs are the same as in X chassis in "60" series VTRs. The following items have been changed and improved.

1-1. The reel drive system has been changed to the gear drive from rubber tyre drive.

1-2. A guide pin has been added to the take-up side. (behind the capstan)

1-3. The front loading mechanism in this chassis is the same as that in the X chassis.

1-4. The capstan bearing is retained by three (3) screws not by caulking.

2. Operations of Each Section

2-1. Components Locations (Fig. 5-1)

The tension band is provided for the supply reel table to control the tension in supplying the tape and the supply sub-brake is installed to apply weak back torque to the supply reel disk during fast forward and rewind.

The impedance roller is next to the full erase (FE) head and absorbs variations in tension of the tape to reduce jitter.

The cylinder is the same type as in conventional VTRs, but a connection P.C.B is provided in the cylinder to prevent noise from entering the upper cylinder from outside.

The lead wires of the heads are not soldered but connectors are used.

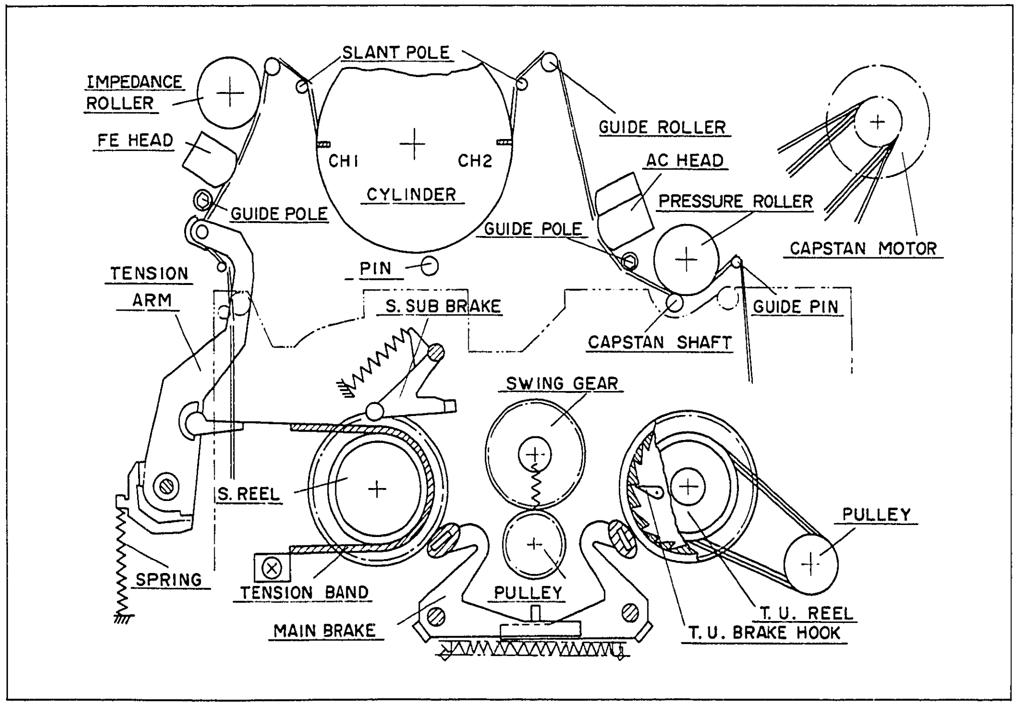


Fig. 5-1 Parts Arrangement

This simplifies replacement of the upper cylinder.

The A/C head consists of the audio head, control head and audio erase head as in conventional VTRs.

The tape guide is installed next to the A/C head and controls the height of the running tape.

The capstan and pressure roller have the same structures as conventional ones, but the flywheel bearing is tightened by three (3) screws, not by caulking.

The guide pin is provided beside the capstan to stabilize the tape transport.

The take-up brake hook is inside the take-up reel table to apply weak back torque in the search modes.

The pulley gear is in the middle of both reel tables, and torque is transmitted to this gear from the capstan motor to drive both reel tables via the swing gear.

Teeth are provided on the external circumference of this swing gear, and to mesh with these, both the reel tables have teeth in their circumferences.

The main brakes operate the same as before.

2-2. Loading Mode (Fig. 5-2)

When the loading motor at the left corner in the chassis turns clockwise, loading is performed.

When the PLAY button is pressed in the stop mode, first the loading motor turns in the loading direction (clockwise as viewed from the shaft axis) and the main brakes are released from both reel tables by the main brake drive mechanism

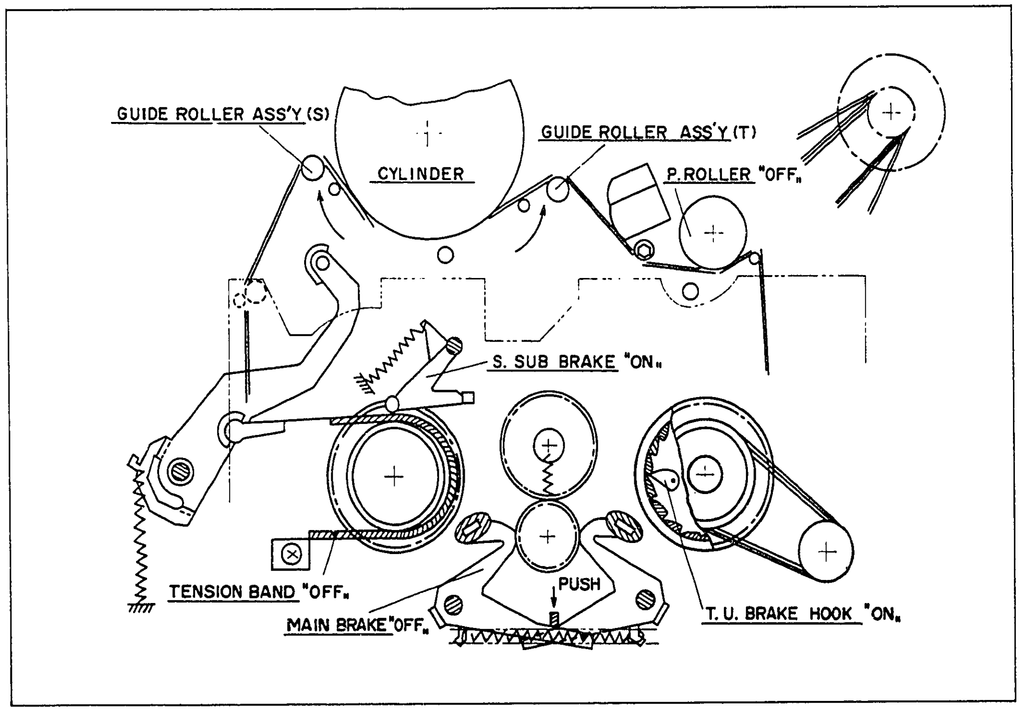


Fig. 5-2 Loading Mode

(see Fig. 5-7). When the loading motor turns further, both guide roller assemblies move along the guide grooves in the chassis. When the guide roller assemblies approximately reach the arm stoppers, the mechanism state switch detects the 4th contact "PLAY" and stops turning the loading motor.

During loading, by the operation of the loading drive arm engaged with gear (R) and gear (L) (shown in Fig. 5-7), braking is applied to the supply reel table by the supply sub brake to prevent tape slack when the tape is supplied. Braking is applied to the take-up reel table by the take-up brake hook in this reel table during loading.

Just before loading is completed, the supply sub-brake is released from the supply reel table and the take-up brake hook is released from the gear in the take-up reel table by the operation of the loading gear assembly. The pressure roller is compressed against the capstan shaft and the mechanism enters the playback mode. The tension band is moved by the spring force as the supply guide roller assembly advances, and as soon as the playback mode is entered, it operates to control the supply tape tension.

2-3. Unloading Mode (Fig. 5-3)

When the STOP button is pressed in the playback or record mode, the loading motor turns counterclockwise (as viewed from the shaft), and the guide roller assemblies, installed to the link arm which is engaged with gears (L) and (R) (shown in Fig. 5-7), move along the grooves in the chassis and return to the stop positions.

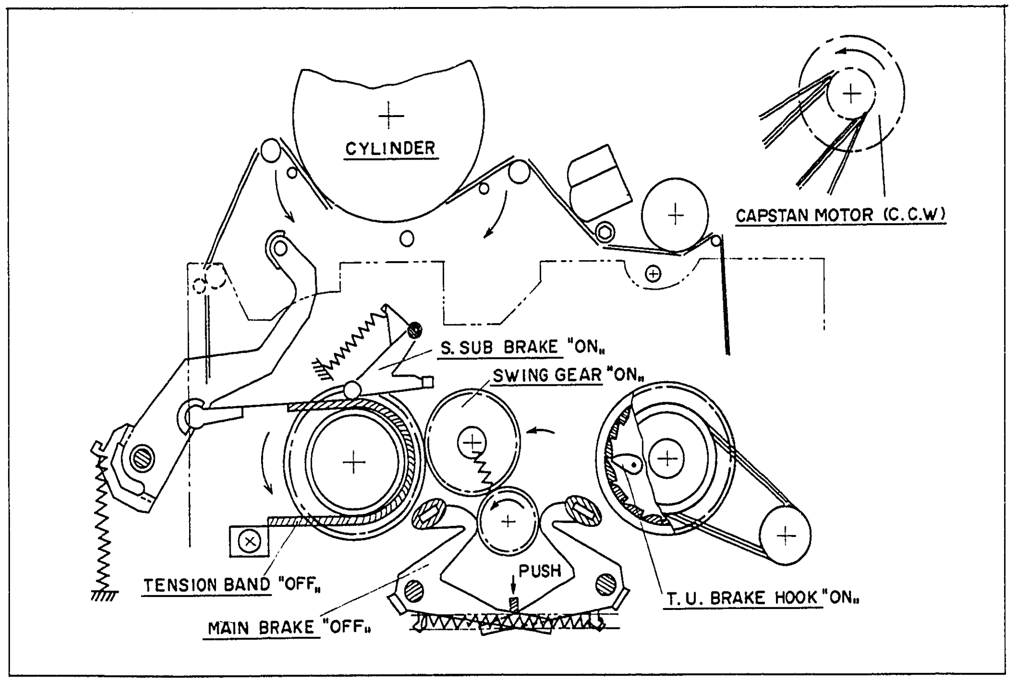


Fig. 5-3 Unloading Mode

To take up the tape supplied, the capstan motor turns counterclockwise. This series of the operations compresses the swing gear against the supply reel table and turns the supply reel table counterclockwise to house the tape in the cassette case.

During unloading, the supply sub-brake is compressed against the supply reel table and the take-up brake hook is engaged with the gear in the take-up reel table during loading.

2-4. Fast Forward Mode (Fig. 5-4)

When the F.FWD button is pressed in the stop mode, the loading motor turns clockwise and releases the main brakes from both reel tables. As the capstan motor turns clockwise, the swing gear is compressed against the take-up reel table and turns the reel table at high speed to take up the tape. Meantime, the supply sub-brake is compressed against the supply reel table to prevent the tape becoming slack during fast forward. The take-up brake hook and the gear in the take-up reel are disengaged each other.

2-5. Rewind Mode (Fig. 5-4)

The mechanism state is almost the same as during fast forward, but the capstan motor rotates counterclockwise at high-speed. Weak back torque is applied to the take-up reel table because the pulley rotates to prevent the tape becoming slack.

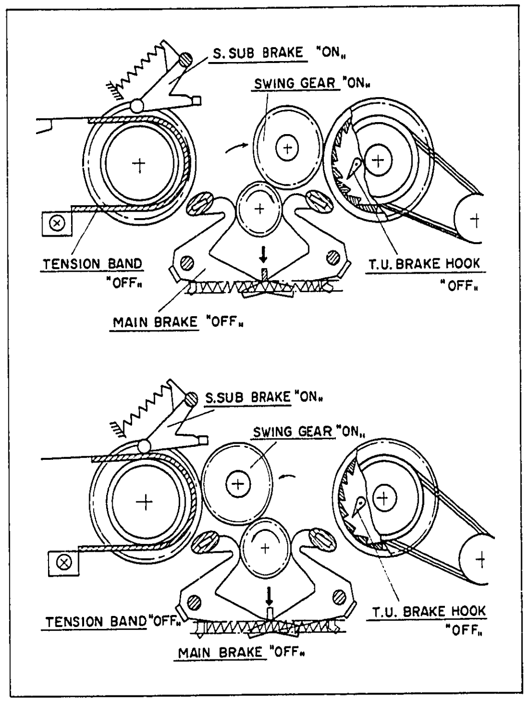

S. SUB BRAKE "ON"
SWING GEAR "ON"
TENSION BAND "OFF"
T.U. BRAKE HOOK "OFF"
MAIN BRAKE "OFF"
S.SUB BRAKE "ON"
SWING GEAR "ON"
TENSION BAND "OFF"
T.U. BRAKE HOOK "OFF"
MAIN BRAKE "OFF"

Fig. 5-4 F.Fwd/Rewind Modes

2-6. Reel Drive Path in Play and unloading Modes (Fig. 5-5).

Both the supply and take-up reel tables must be driven at the appropriate torque in the play and unloading modes. This is because the torque transmitted from the capstan motor is limited by the slip mechanism provided on the take-up pulley and is then transmitted to both reel tables. The torque transmitted to the belt pulley in Fig. 5-5 is transmitted to the take-up pulley via the belt.

The slip mechanism provided in the upper part of the take-up pulley limits the torque from the capstan motor to an appropriate value and it is transmitted to the pulley gear via the take-up gear, idler gear, and clutch gear. The swing gear compressed against the pulley gear swings its neck to the left and right and is compressed against both reel tables to transmit the torque. Meantime, the clutch gear is pushed up by the clutch lever and is engaged with the idler gear. This operation is performed by the drive arm engaged with the gear (R) as the loading motor rotates.

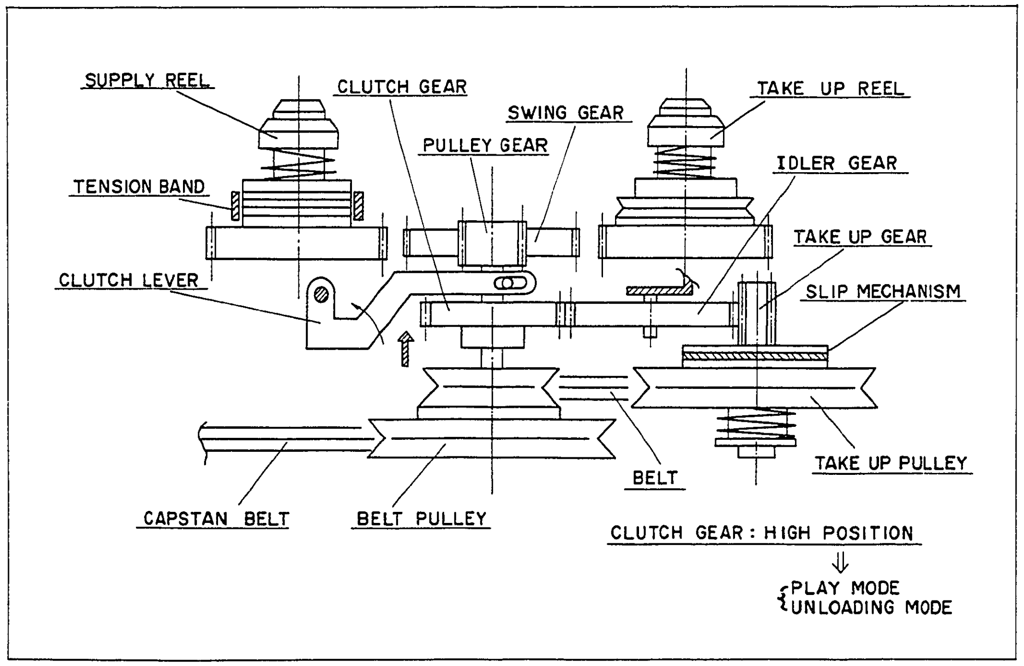

SUPPLY REEL
CLUTCH GEAR
SWING GEAR
PULLEY GEAR
TAKE UP REEL
IDLER GEAR
TENSION BAND
TAKE UP GEAR
CLUTCH LEVER
SLIP MECHANISM
BELT
TAKE UP PULLEY
CAPSTAN BELT
BELT PULLEY
CLUTCH GEAR : HIGH POSITION
⇓
PLAY MODE
UNLOADING MODE

Fig. 5-5 Reel Drive in Play/Unloading Modes

2-7. Reel Drive Path in F.Fwd and Rewind Modes (Fig. 5-6)

Since strong torque must be applied to both reel tables in the fast forward and rewind modes, the torque from the capstan motor should not be limited and transmitted directly to both reel tables. When the F.FWD or REWIND button is pressed in the stop mode, the loading motor turns clockwise and the mechanism state switch detects the 2nd position, then the turning of loading motor is stopped. During these operations, simultaneously when the main brakes are released from both reel tables, the clutch gear is pushed down and the engagement with the idler gear is released. When the clutch gear is depressed, it engages with the belt pulley directly, and the torque from the capstan motor is transmitted directly to the pulley gear without any slipping.

The weak torque which is transmitted via the slip mechanism is not transmitted to the pulley gear because the idler gear and clutch gear are disengaged each other.

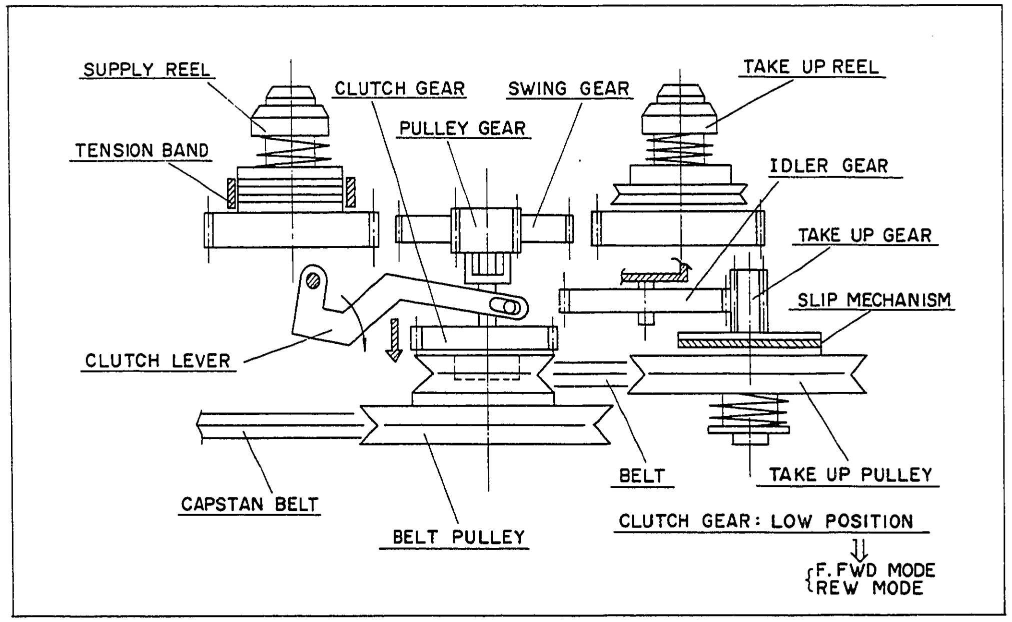

SUPPLY REEL
CLUTCH GEAR
SWING GEAR
TAKE UP REEL
TENSION BAND
PULLEY GEAR
IDLER GEAR
TAKE UP GEAR
SLIP MECHANISM
CLUTCH LEVER
CAPSTAN BELT
BELT PULLEY
BELT
TAKE UP PULLEY
CLUTCH GEAR: LOW POSITION
F.FWD MODE
REW MODE

Fig. 5-6 Driving Path (F.Fwd/Rewind Modes)

2-8. Main Brake Drive Mechanism (Fig. 5-7)

When the PLAY, F.FWD or REWIND button is pressed in the stop mode, the loading motor turns clockwise and drives the worm gear via three (3) pulleys. This worm gear is engaged with the gear (R). The guide groove is provided on the gear (R), and the drive arm engaged with this groove pulls the brake slider to the left in Fig. 5-7 as the loading motor turns. The projection on the slider is engaged with the recess in the lock plate, and when the slider moves to the left, the brake slider is also pulled to the left. Through this operation, the ramp X (See Fig. 5-7) of the brake slider depresses the main brake drive pin in contact with this ramp downward in Fig. 5-7. When the main brake drive pin is pressed in the direction of the arrow in Fig. 5-7, the main brakes are released from both reel tables and braking is released.

When the lock plate passes under the change piece and touches it, the rotation of the change piece slips and the engagement between the lock plate and slider is not released and the lock plate moves to the left and is set to the position shown in Fig. 5-7 (a).

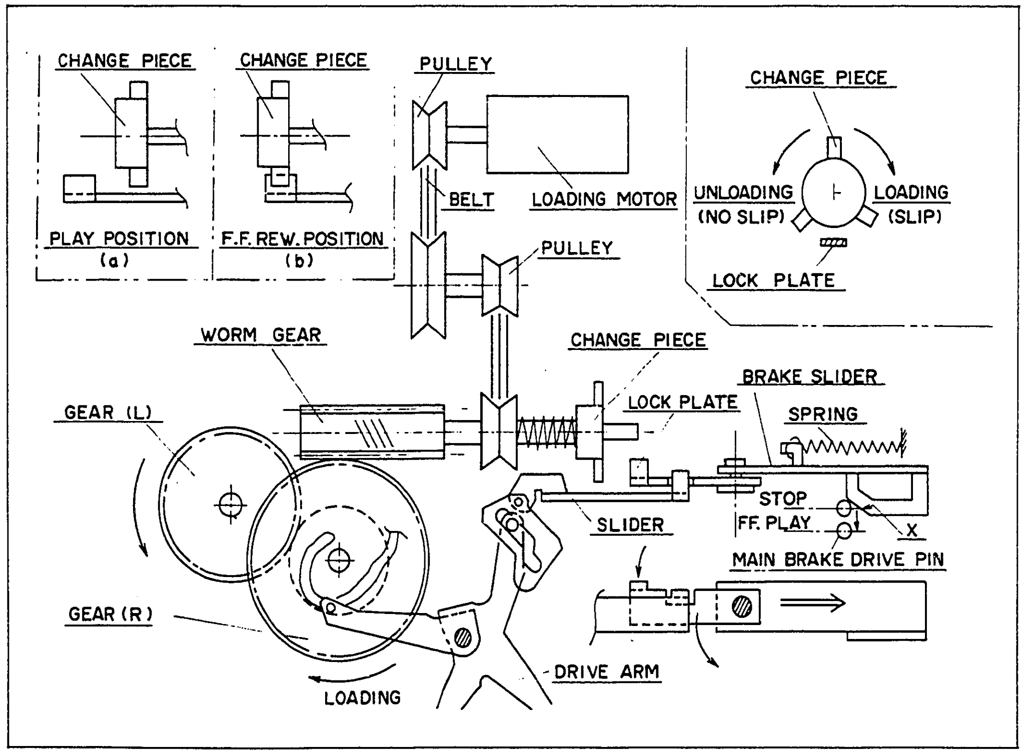

CHANGE PIECE
CHANGE PIECE
PULLEY
CHANGE PIECE
PLAY POSITION
(a)
F.F. REW. POSITION
(b)
BELT
LOADING MOTOR
PULLEY
UNLOADING
(NO SLIP)
LOADING
(SLIP)
LOCK PLATE
WORM GEAR
CHANGE PIECE
BRAKE SLIDER
GEAR (L)
LOCK PLATE
SPRING
STOP
FF. PLAY
X
SLIDER
MAIN BRAKE DRIVE PIN
GEAR (R)
DRIVE ARM
LOADING

Fig. 5-7 Main Brake Drive Mechanism

piece, the mechanism state switch detects the 2nd position and stops turning the loading motor. That is, the lock plate is set to the position in Fig. 5-7 (b).
When the main brakes are applied, for example when the STOP button is pressed in the playback mode, the lock plate moves to the right from the state shown in Fig. 5-7 (a). When the lock plate reaches under the change piece, it is pushed down by the projection on the change piece. With this operation, the engagement between the slider and lock plate is released and the brake slider is rapidly moved to the right by the spring force. Since the main brake drive pin which is in contact with the ramp of the brake slider is compressed against this ramp, accompanying with the rapid shift of the brake slider, the pin is rapidly pushed up as shown in the figure and the main brake operates.
When the main brakes is applied in the fast forward mode, since the lock plate is set under the change piece as shown in Fig. 5-7 (b), simultaneously when the stop button is pressed and the loading motor starts turning counterclockwise, the change piece also turns counterclockwise. With this operation, as the change piece pushes down the lock plate, the engagement between the slider and lock plate is released, and the main brake is applied.
When the projection on the change piece comes into contact with the lock plate during loading, the turning of the change piece slips and it does not depresses the lock plate. During unloading, the turning of the change piece does not slip and the change piece pushes down the lock plate.

2-9. Operation Chart (Fig. 5-8)

This chart shows the operation timing of the main components. "ON" means that the component is operating and "OFF" means that the component is not operating or is being released. As can be seen in the chart, the take-up brake hook in the take-up reel table operates in the reverse search mode as well as during loading and unloading.

	MODE SWITCH POSITION	OPERATION MODE	S.SUB BRAKE	T.U. BRAKE HOOK	PRESSURE ROLLER	TENSION BAND	REMARKS
1	STOP	STOP	ON	ON	OFF	OFF	
							MAIN BRAKE IS RELEASED
2	FF REW	F. FWD, REWIND	ON	OFF	OFF	OFF	
3	REC-PAUSE	REC PAUSE	ON	ON	OFF	OFF	
4	REC/PLAY	REC, PLAY, PLAY-PAUSE, FORWARD VISUAL SEARCH	OFF	OFF	ON	ON	
5	REVERSE	REVERSE VISUAL SEARCH	OFF	ON	ON	OFF	

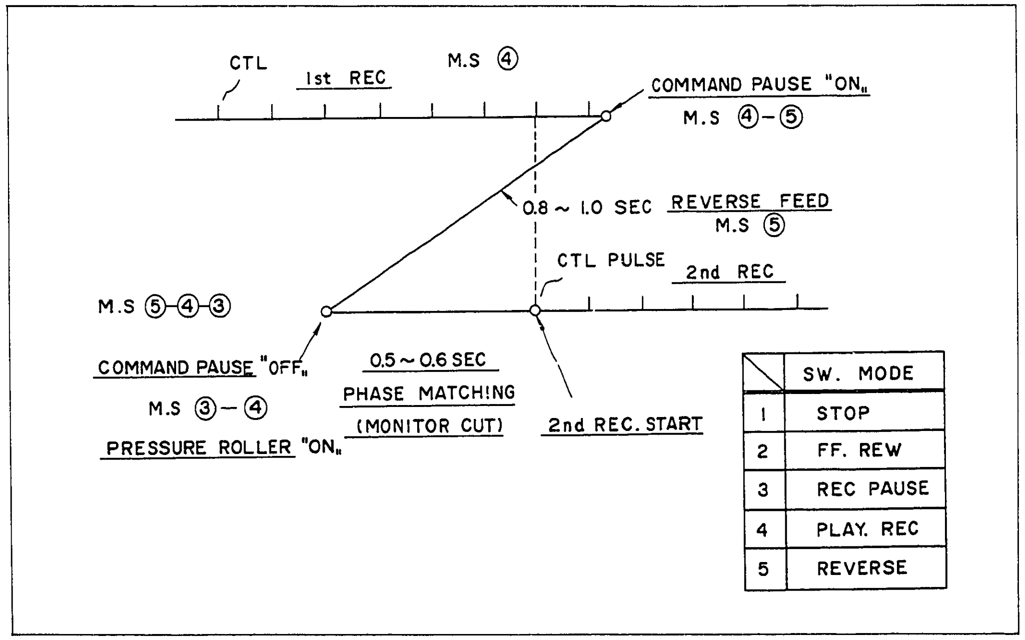
Fig. 5-8 Operation Chart

2-10. Record Pause Mode (Fig. 5-9)

In this mode the mechanism operates so the joint of pictures recorded previously and to be recorded later does not appear as distortion during playback.
When the PAUSE button is pressed in the previously record mode, the loading motor turns in the loading direction and the mechanism state switch advances to the 5th position. With this operation, braking is applied to the take-up reel table by the take-up brake hook in the take-up reel to prevent tape slack occurring when the tape is run in reverse (to the supply reel). When the capstan motor turns counterclockwise afterwards, the tape is returned to the supply reel and is stopped after approx. 0.8 seconds. After the tape is stopped, the loading motor turns in the unloading direction and the mechanism state switch is returned to the 3rd from 5th position. This operation releases the pressure roller from the capstan shaft.
Then, the capstan motor changes its turninng direction to clockwise to prepare for the next start and stands by in this state (record pause mode).

When the pause mode is released, the loading motor turns in the loading direction to advance the mechanism state switch to the 4th from 3rd position. This operation compresses the pressure roller against the capstan and the tape is fed to the direction of the take-up reel.

The servo circuit performs phase matching during these operations, and after the tape speed of the tape to be played back is aligned with that during recording, the video circuit is switched to the record mode. With this operation, since the timings of the CTL pulses recorded previously and to be recorded later are aligned, the picture at the joint is not distorted during playback. This is called the phase matching mode (record pause mode).



	SW. MODE
1	STOP
2	FF. REW
3	REC PAUSE
4	PLAY. REC
5	REVERSE

Fig. 5-9 Record Pause Mode

6.1 GENERAL

Table 1-1a,b shows the differences between the VT-1310A/1305A and VT-1100A/1105A. The composition of the VT-1310A/1305A is described as follows.

Luminance/Chroma Circuit:
The "HQ" system employs new ICs revised from those in the VT-1100A/1105A for requirements of productivity and also newly employs the Detail Enhancer circuit as a exclusive IC HA11888.

System Control Circuit:
System control circuit employs the new µP revised from VT-1100A/1105A for requirements of productivity.

Tuning Control Circuit:
107CH, Voltage Synthesizer tuning control circuit employs the new µP and REG/BAND SELECTOR IC, revised from VT-1100A/1105A for requirements of productivity.

Timer Control Circuit:
4-Event/2-Week Timer control circuit employs the new µP revised from VT-1100A/1105A for requirements of productivity.

Audio Circuit:
New audio processing IC is used. The circuit configuration of the VT-1310A/1305A is very similar to that in the VT-1100A/1105A.

Servo Circuit:
Same as in VT-1100A/1105A except that;
Time constant components for each MMs in the main servo processing ICHA11853, low-pass filters and limiters on the SERVO SUB board in the VT-1100A/1105A are integrated into two modules, BX6238 and BX6239.

Miscellaneous Circuit:
Other circuits are almost the same as VT-1100A/1105A .

Table 6-1a (Y)/(PY) Chassis Comparison Table

#	ITEM	Y	PY	NOTE
1	MECHANISM	Y MECHA	SAME AS Y	
2	LAYOUT		SEE ACTUAL UNIT	
3	P.C.B	A) LUMINANCE/CHROMINANCE B) AUDIO JACK SYSTEM CONTROL SERVO CAPSTAN DRIVER U-V TUNER U-V TUNING C) REGULATOR CYLINDER DRIVER D) TIMER AND KEY	A) LUMINANCE/CHROMINANCE AUDIO JACK U-V TUNER U-V TUNING B) SYSTEM CONTROL SERVO CAPSTAN DRIVER CYLINDER DRIVER C) REGULATOR D) TIMER AND KEY	
4	CIRCUIT COMPONENT ("HT-" and "BX-" means hybrid IC)	HT-4705 HT-4723 HT-4495 HT-4497	HT-4765C HT-4763 HA-11888 M51485L MSM6964	LUMINANCE
		HA11856	HT4706	CHROMINANCE
		BA5119S	M51654AP	AUDIO
		HA11853 TRANSISTORS	HA11853 HA11887	SERVO
		SERVO SUB (I) (II) CIRCUIT BOARD	BX-6238 BX-6239 (3 heads) BX-6240 (2 heads)	
		SYSTEM CONTROL MICROPROCESSOR	REFINED TO INTEGRATE SOME COMPONENTS	SYSTEM CONTROL
		LA7934	LA79356	TUNING CIRCUIT
		TUNING MICROPROCESSOR	REFINED TO INTEGRATE SOME COMPONENTS	
		TIMER/INPUT KEY/FUNCTION SW	SAME AS Y	
		TIMER MICROPROCESSOR	SAME AS Y	
		STK-5471	STK-5471	REGULATOR
		TUNER	SLIGHTLY CHANGED BY REFINING TUNING MICROPROCESSOR	
		RF CONVERTER	SAME AS Y	

Table 6-1b Difference between VT-1100A/1105A & VT-1310A/1305A (Circuit)

MODEL ITEM		VT-1100A/1105A	VT-1310A/1305A	NOTE
CHASSIS		Y	PY	
LUMA		HT-4755	HT-4765C	
		HT-4723	HT-4763	
		HT-4495	HA-11888	DETAIL ENHANCER
		HT-4497 (MSM6964 is mounted)	M51485L MSM6964	2fsc OSC CCD 1H DELAY LINE
CHROMA		HA11856ANT	HT-4706	
CYLINDER	SHAPE	MOUNT TYPE OF PREAMP	SAME AS Y	
	MOTOR	3-PHASE	SAME AS Y	
SERVO		HA11853	HA11853	
		SOME TRANSISTORS	HA11887	CFG AMP
		SUB P.C.B	BX-6238 BX-6239	
SYSTEM		HD614042SD76	HD614042SE43	
TUNING CIRCUIT		LA7934 M50161-452	LA7935 M50161-454	
TIMER		M50752-635	M50752-622	
TUNER				REFINING VS µCON, AUDIO MUTING
AUDIO		BA5119S	M5165AP	

6-2 LUMINANCE/CHROMA

6-2-1 Comparison of IC Functions

Differences between VT-1310A/1305A and VT-1100A/1105A in Luminance/Chroma Circuit are shown in Table 6-2.

Table 6-2 Comparison of IC Functions between VT-1310A/1305A and VT-1100A/1105A

	IC Code		Major Difference and Function
	VT-1310A/ 1305A	VT-1100A/ 1105A	
IC201	HT4765C	HT4755	◦ Detail Enhancer circuit is moved to exclusive IC (IC203). ◦ External Phase Compensation circuit (Q202/Q204/ Q222) is integrated into this IC. ◦ AGC Switch in IC205 (HT4763) is integrated into this IC.
IC202	HT4706A	HA11856 ANT	◦ Peripheral circuits are integrated into this IC. ◦ Monitor Cut Switch (Q205) ◦ Output Buffer Amplifier (Q208) of Delay Line (DL201). ◦ 3.58MHz BPF (Q226) ◦ 3.58MHz Crystal Oscillator ◦ Peripheral resistors and capacitors
IC203	HA11888	--	◦ Detail Enhancer in IC201 is moved to this exclusive IC. (Works during recording mode at all tape speeds SP/LP/SP) ◦ This circuit works as a buffer amplifier during playback mode (equivalent to IC208 in VT-1100A/ 1105A)
IC204	MSM6964	HA4497	◦ Monolithic IC MSM6964 integrated in Hybrid IC HA4497 is employed indendently as a new circuit. ◦ Doubler circuit in HA4497 is moved to IC206.
IC205	HT4763	HT4723	◦ AGC Switch circuit is moved to IC201. ◦ PB5V Switch (Q206) is integrated into this IC.
IC206	M51485L	--	◦ Doubler circuit is moved from IC204 HA4497 ◦ LEVEL SHIFT (MUTE SW) Q216 and Q217 are integrated into this IC. ◦ Buffer Amplifier is moved from IC204. ◦ 9V Regulator circuit is incorporated and supplys 9V for IC203 and IC204.

6-2-2 Detail Enhancer Circuit Operation

As shown in Fig. 6-1, the input signal passing through the detail enhancer is applied to the adder circuit via R211, R212 and C253 and is added to the input signal directly applied to the adder, thus the enhancer characteristic is produced.
The detail enhancer circuit works during recording at all tape speeds, SP, LP and EP.
The enhancer characteristic is almost the same as that of the VT-1100A/1105A.

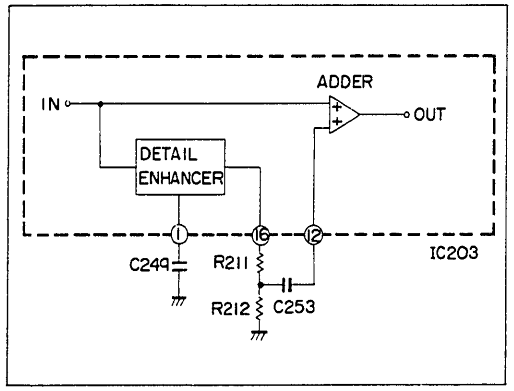
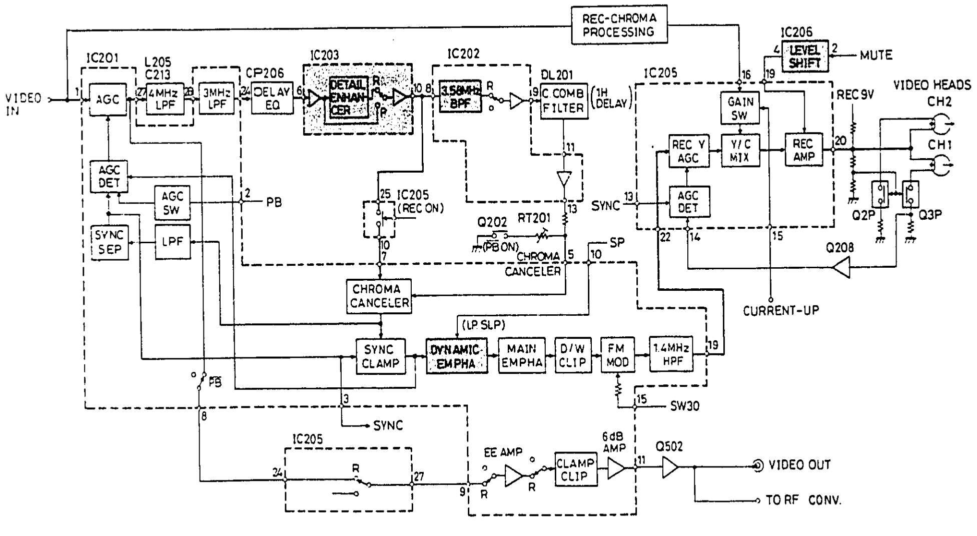


Fig. 6-1 Detail Enhancer Circuit

6-2-3 Circuit Blockdiagram

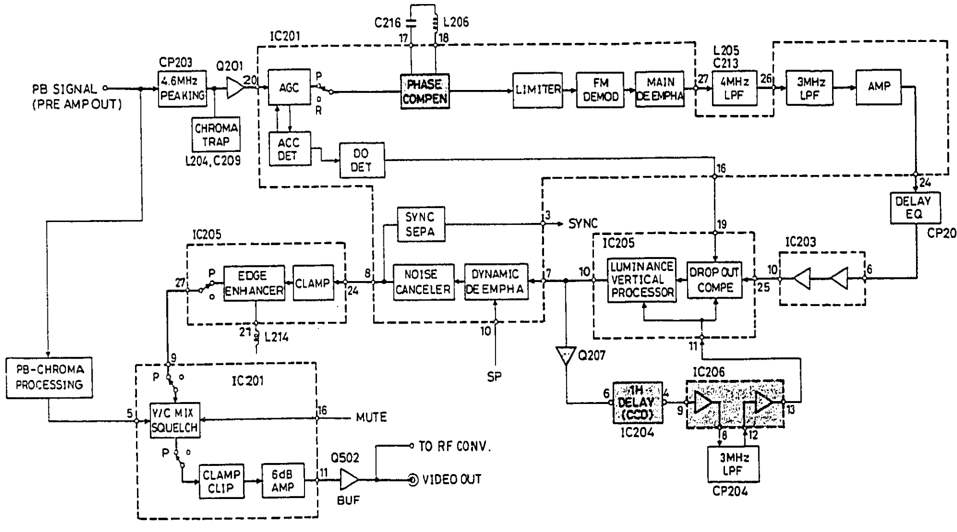
Fig. 6-2 to Fig. 6-5 are simplified Luminance/Chrominance Record/Playback Circuit Blockdiagrams.

Meshed portions are changed blocks from the VT-1100A/1105A.


VIDEO IN
IC201
AGC
AGC DET
AGC SW
SYNC SEP
LPF
L205 C213
4MHz LPF
3MHz LPF
CP206
DELAY EQ
IC203
DETAIL ENHANCER
IC202
3.58MHz BPF
DL201
C COMB FILTER
(1H DELAY)
REC-CHROMA PROCESSING
IC206
LEVEL SHIFT
MUTE
IC205
GAIN SW
REC Y AGC
Y/C MIX
REC AMP
AGC DET
REC 9V
VIDEO HEADS
CH2
CH1
Q2P
Q3P
Q208
SYNC
PB
IC205 (REC ON)
Q202 (PB ON)
RT201
CHROMA CANCELER
SP
CURRENT-UP
CHROMA CANCELER
(LP SLP)
SYNC CLAMP
DYNAMIC EMPHA
MAIN EMPHA
D/W CLIP
FM MOD
1.4MHz HPF
SW30
PB
SYNC
IC205
EE AMP
CLAMP CLIP
6dB AMP
Q502
VIDEO OUT
TO RF CONV.
R
P

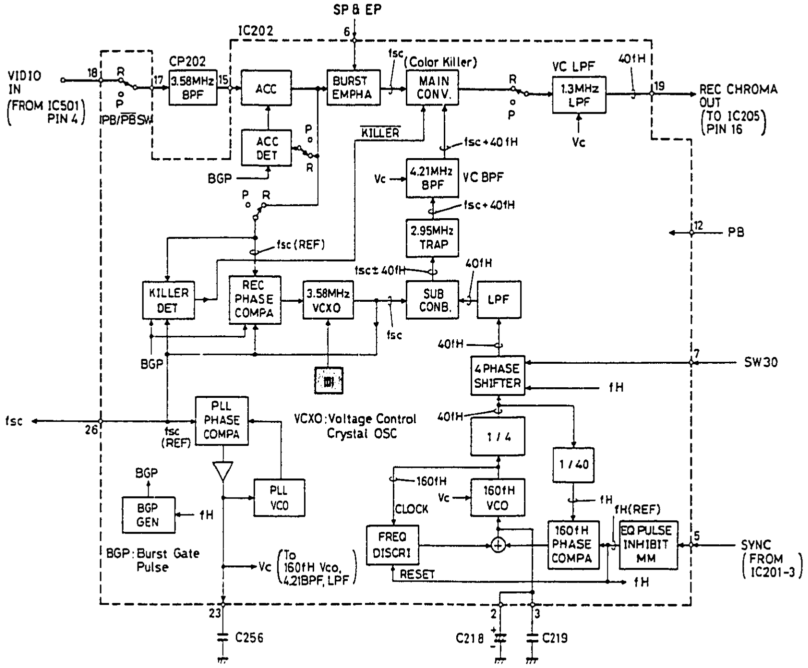
Meshed portions are changed from VT-1100A/1105A

Fig. 6-2 Simplified Luminance Record Circuit Diagram


PB SIGNAL (PRE AMP OUT)
CP203
4.6MHz PEAKING
CHROMA TRAP
L204, C209
Q201
IC201
AGC
ACC DET
DO DET
C216
L206
PHASE COMPEN
LIMITER
FM DEMOD
MAIN DE EMPHA
L205 C213
4MHz LPF
3MHz LPF
AMP
DELAY EQ
CP206
SYNC SEPA
SYNC
IC205
EDGE ENHANCER
CLAMP
L214
NOISE CANCELER
DYNAMIC DE EMPHA
SP
IC205
LUMINANCE VERTICAL PROCESSOR
DROP OUT COMPE
IC203
Q207
IC206
1H DELAY (CCD)
IC204
3MHz LPF
CP204
PB-CHROMA PROCESSING
IC201
Y/C MIX SQUELCH
MUTE
CLAMP CLIP
6dB AMP
Q502
BUF
TO RF CONV.
VIDEO OUT
P
R

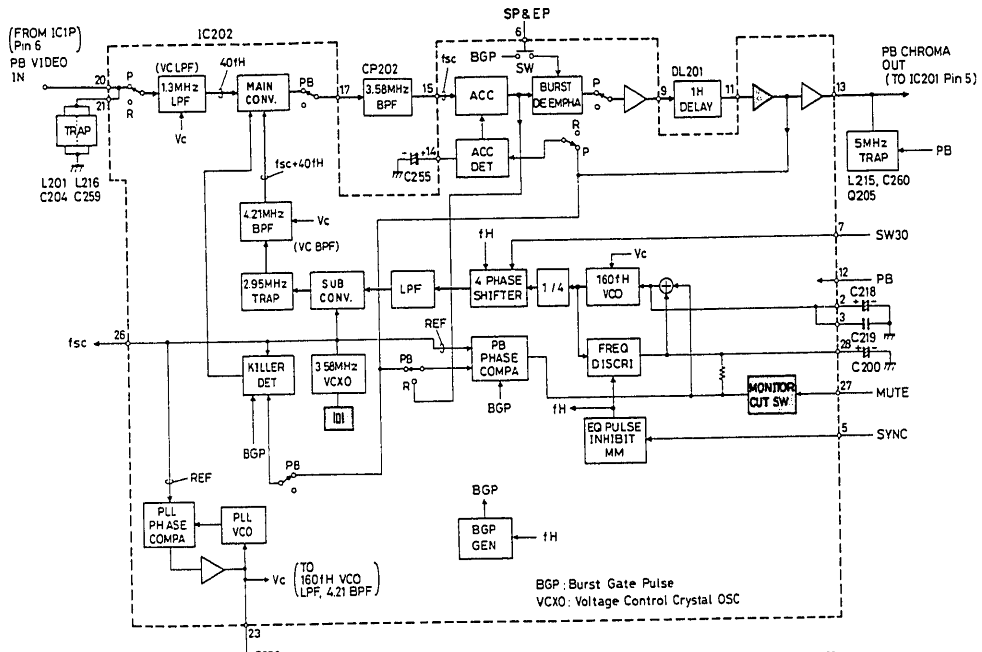
Meshed portions are changed from VT-1100A/1105A

Fig. 6-3 Simplified Luminance Playback Circuit Diagram


SP & EP
IC202
VIDIO IN (FROM IC501 PIN 4)
PB/PB SW
CP202
3.58MHz BPF
ACC
ACC DET
BGP
BURST EMPHA
fsc (Color Killer)
MAIN CONV.
KILLER
fsc+40fH
Vc
4.21MHz BPF
VC BPF
2.95MHz TRAP
fsc±40fH
40fH
SUB CONB.
LPF
VC LPF
1.3MHz LPF
REC CHROMA OUT (TO IC205 PIN 16)
PB
fsc (REF)
KILLER DET
REC PHASE COMPA
3.58MHz VCXO
fsc
SW30
4PHASE SHIFTER
fH
PLL PHASE COMPA
PLL VCO
BGP GEN
VCXO: Voltage Control Crystal OSC
1/4
1/40
160fH
CLOCK
160fH VCO
FREQ DISCRI
RESET
160fH PHASE COMPA
fH(REF)
EQ PULSE INHIBIT MM
SYNC (FROM IC201-3)
BGP: Burst Gate Pulse
Vc (To 160fH Vco, 4.21BPF, LPF)
C256
C218
C219
P
R

Meshed portion is changed from VT-1100A/1105A

Fig. 6-4 Simplified Chrominance Record Circuit Diagram


FROM IC1P Pin 6
PB VIDEO IN
IC202
(VC LPF)
40fH
1.3MHz LPF
MAIN CONV.
Vc
PB
P
R
20
21
TRAP
L201 L216
C204 C259
fsc+40fH
4.21MHz BPF
(VC BPF)
2.95MHz TRAP
SUB CONV.
LPF
4 PHASE SHIFTER
1/4
160fH VCO
fH
REF
PB PHASE COMPA
FREQ DISCRI
KILLER DET
3.58MHz VCXO
BGP
fsc
26
PLL PHASE COMPA
PLL VCO
Vc (TO 160fH VCO LPF, 4.21 BPF)
23
C256
CP202
17
3.58MHz BPF
15
SP&EP
6
fsc
BGP
SW
ACC
ACC DET
C255
14
BURST DE EMPHA
DL201
9
1H DELAY
11
13
PB CHROMA OUT (TO IC201 Pin 5)
5MHz TRAP
L215, C260
Q205
7
SW30
12
C218
2
3
C219
28
C200
27
MUTE
5
SYNC
MONITOR CUT SW
EQ PULSE INHIBIT MM
BGP GEN
BGP : Burst Gate Pulse
VCXO : Voltage Control Crystal OSC

Meshed portions are changed from VT-1100A/1105A

Fig. 6-5 Simplified Chrominance Playback Circuit Diagram

6-3 SYSTEM CONTROL

6-3-1 General

Fig. 6-6 is a simplified system control circuit diagram of VT-1310A/1305A. In this figure, there are only 1 differences from VT-1100A/1105A, the VTR mode indication is added to Digital multidisplay. But the following items regarding system control and tuning control μPs are revised from these in the VT-1100A/1105A.

Following items are the revised points in each μP.

S-μP:

Trick play signal, ASBL REC MUTE signal, pause/F.ADV signal and SP/LP/EP signal for the requirements of productivity.

Tu-μP:

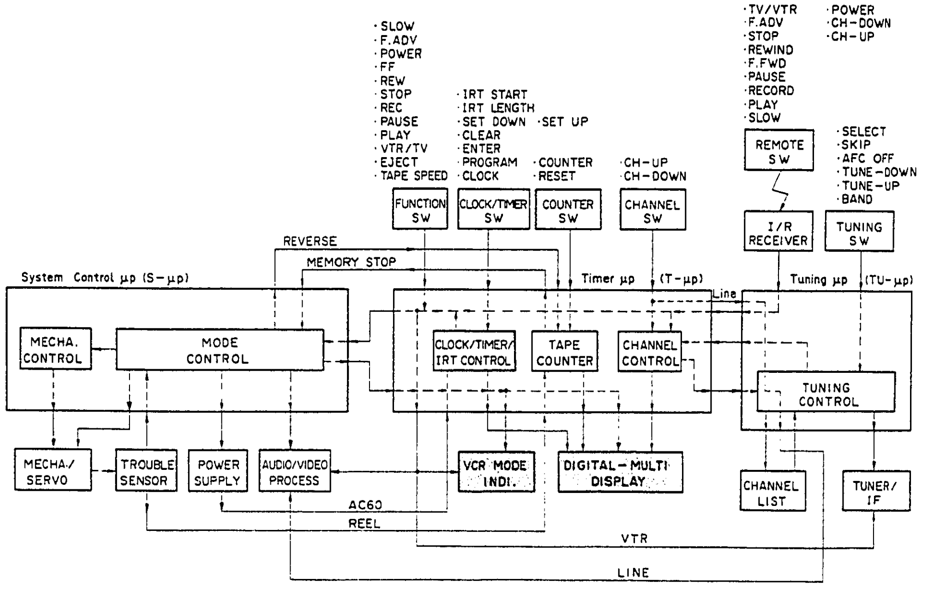
AFC signal, Mute signal, Reset signal, 5.0V output and current source for the requirements of productivity.

T-μP:

VTR mode display and Key matrix.

6-3-2 System Control Circuit

Type of S-μP in VT-1310A/1305A and VT-1100A/1105A are HD614042SE43 and HD614042SD76 respectively. They have almost the same functions basically, except for some items shown in Table 6-3.


·SLOW
·F.ADV
·POWER
·FF
·REW
·STOP
·REC
·PAUSE
·PLAY
·VTR/TV
·EJECT
·TAPE SPEED
·IRT START
·IRT LENGTH
·SET DOWN
·SET UP
·CLEAR
·ENTER
·PROGRAM
·CLOCK
·COUNTER
·RESET
·CH-UP
·CH-DOWN
·TV/VTR
·F.ADV
·STOP
·REWIND
·F.FWD
·PAUSE
·RECORD
·PLAY
·SLOW
·POWER
·CH-DOWN
·CH-UP
·SELECT
·SKIP
·AFC OFF
·TUNE-DOWN
·TUNE-UP
·BAND
FUNCTION SW
CLOCK/TIMER SW
COUNTER SW
CHANNEL SW
REMOTE SW
I/R RECEIVER
TUNING SW
REVERSE
MEMORY STOP
System Control μp (S-μp)
Timer μp (T-μp)
Tuning μp (TU-μp)
Line
MECHA. CONTROL
MODE CONTROL
CLOCK/TIMER/IRT CONTROL
TAPE COUNTER
CHANNEL CONTROL
TUNING CONTROL
MECHA./SERVO
TROUBLE SENSOR
POWER SUPPLY
AUDIO/VIDEO PROCESS
VCR MODE INDI.
DIGITAL-MULTI DISPLAY
CHANNEL LIST
TUNER/IF
AC60
REEL
VTR
LINE

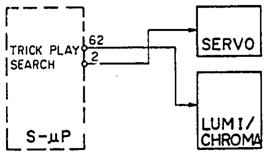
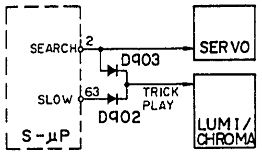
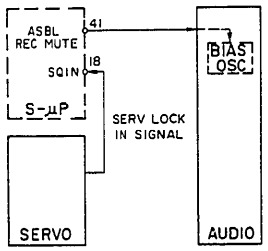
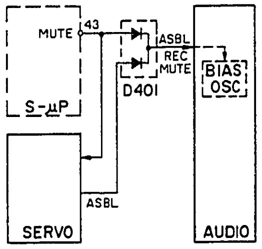
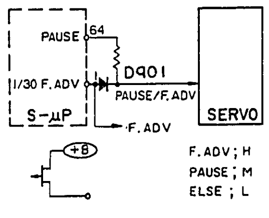
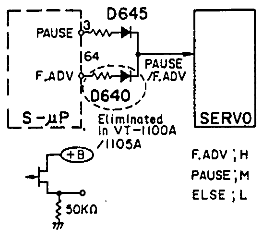
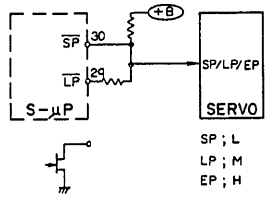
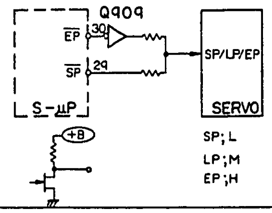
Meshed portions are newly added or changed from VT-1100A/1105A

Fig. 6-6 System Control Block Diagram

Table 6-3 shows the system control circuit differences between VT-1310A/1305A and VT-1100A/1105A.

1. TRICK PLAY signal. In VT-1100A/1105A, Trickplay signal was made by adding the SEARCH signal and SLOW signal with D902 and D903. In the VT-1310A/1305A, Trickplay port (port No.62 of S-µP) is newly added and outputs High, during SEARCH and SLOW modes.
2. ASBL REC MUTE signal. In VT-1100A/1105A, ASBL REC MUTE signal was made by adding the Mute signal (S-µP port No.43) and ASSEMBLE signal from SERVO circuit with D401. In the VT-1310A/1305A, port No.18 of S-µP receives the SQUELCH signal from SERVO circuit, and port No.41 outputs ASBL REC MUTE signal (ASBL REC MUTE = MUTE + ASSEMBLE).

Table 6-3 System Control Circuit Differences between VT-1310A/1305A & VT-1100A/1105A

NO.	ITEMS	VT-1310A/1305A	VT-1100A/1105A	NOTES
1.	TRICK PLAY SIGNAL	 TRICK PLAY SEARCH 62 2 S-µP SERVO LUMI/CHROMA TRICK PLAY= SERCH+SLOW	 SEARCH 2 D903 SLOW 63 D902 TRICK PLAY S-µP SERVO LUMI/CHROMA	
2.	OSC STOP SIGNAL	 ASBL REC MUTE 41 SQIN 18 S-µP SERV LOCK IN SIGNAL BIAS OSC SERVO AUDIO	 MUTE 43 ASBL REC MUTE D401 S-µP BIAS OSC ASBL SERVO AUDIO	
3	PAUSE/F. ADV SIGNAL	 PAUSE 64 D901 1/30 F.ADV 3 PAUSE/F.ADV S-µP F.ADV SERVO +B F.ADV ; H PAUSE ; M ELSE ; L	 D645 PAUSE 3 F.ADV 64 PAUSE /F.ADV D640 S-µP Eliminated in VT-1100A /1105A SERVO +B 50KΩ F.ADV ; H PAUSE ; M ELSE ; L	Applied to VT-1310A /1305A only
4	SP/LP/EP SIGNAL	 +B SP 30 LP 29 S-µP SP/LP/EP SERVO SP ; L LP ; M EP ; H	 Q909 EP 30 SP 29 S-µP SP/LP/EP SERVO +B SP; L LP; M EP; H	

3. PAUSE/F.ADV signal. In VT-1100A/1105A, the Tri-state signal PAUSE/F.ADV was made by adding the PAUSE signal and F.ADV signal with D640 and D645. In VT-1310A/1305A, the PAUSE/F.ADV signal is made by adding these signals without diodes. Because the output ports No.3 and 64 of the VT-1100A/1105A S-µP each have PULL-DOWN Resistors (40-160kohms) in internal circuit of the µP, but these PULL-DOWN Resistors were eliminated in VT-1310A/1305A S-µP.
4. SP/LP/EP Signal. In VT-1100A/1105A the Tri-state signal SP/LP/EP was made by adding $\overline{SP}$ signal and $\overline{EP}$ signal with inverter Q909 and resistors. Then in VT-1310A/1305A, the same signal was made by adding $\overline{SP}$ signal and $\overline{LP}$ signal with only 2 resistors. The logic and types of FETs of output ports were changed from $\overline{SP}$, $\overline{EP}$ to $\overline{SP}$, $\overline{LP}$, from N-CH output FET with PULL-UP Resistor to open Drain N-CH output FET.

6-3-3 Timer Control Circuit

T-µPs in VT-1310A/1305A and VT-1100A/1105A are M50752-622 and M50752-635 respectively. They have almost the same functions basically except some items shown in Table 6-4. Table 6-4 shows the Timer Circuit differences between VT-1310A/1305A and VT-1100A/1105A.

1. Mode display. Mode display in VT-1310A/1305A has 2-way, VTR ON, STOP and PAUSE indicator with LEDs and PLAY, REC, FF and REW indicators by Digital Multidisplay.
   On the other hand, the mode display in VT-1100A/1105A had 1-way, VTR ON, STOP, PAUSE, PLAY, REC, FF and REW indicators with LEDs.
2. Key Matrix Circuit
   Counter Reverse input port (port No.7) was added and a Matrix sw with Q753 was eliminated for the same purpose.
3. No. of Programs/Periods.
   Changed from 2 programs/2 weeks to 4 programs/2 weeks.

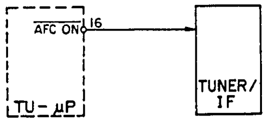
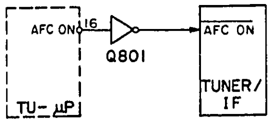
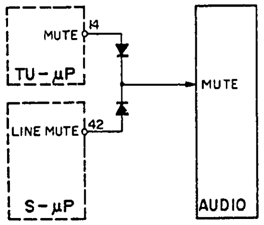
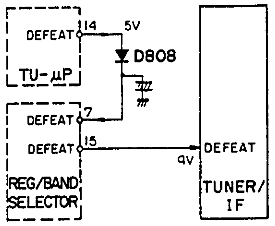
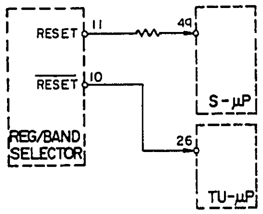
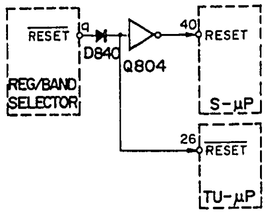
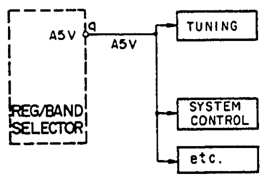
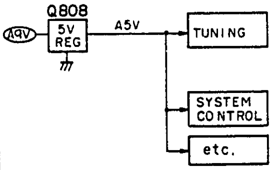
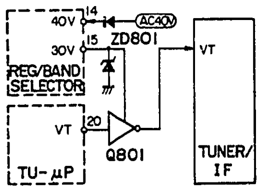
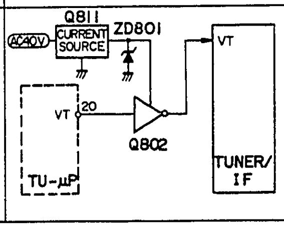
Table 6-4 Timer Circuit Differences between VT-1310A/1305A & VT-1100A/1105A

NO.	ITEMS	VT-1100A/1105A	VT-1310A/1305A	NOTES
1	MODE DISPLAY	VCR ON STOP PAUSE PLAY REC FF REW } BY LED INDI.	VCR ON STOP PAUSE } BY LED INDI. PLAY REC FF REW } BY DIGITAL MULTIDISPLAY	
2	KEY MATRIX	COUNTER REVERSE Q758	(INDEPENDENT PORT NO.7)	
3	EVENT/PERIOD	2 PROGRAMS / 2 WEEKS	4 PROGRAMS / 2 WEEKS	

6-3-4 Tuning Control Circuit

Tunig µP and REG/BAND SELECTOR IC were revised from those of VT-1100A/1105A, from M50161-452SP to M50161-454SP and from LA7934 to LA7935 respectively. There is only one revised point in Tu-µP which is shown in Table 6-5 item 1. 4 points are revised in REG/BAND SELECTOR IC as shown in Table 6-5 item 2 to 5. Table 6-5 shows the Tuning Circuit Differences between VT-1310A/1305A and VT-1100A/1105A.

Table 6-5 Tuning Circuit Differences between VT-1310A/1305A & VT-1100A/1105A

NO.	ITEMS	VT-1310A /1305A (M50161-454SP LA7935)	VT-1100A/1105A (M50161-452SP LA7934)	NOTES
1	AFC SIGNAL	 AFC ON 16 TU-µP TUNER/ IF	 AFC ON 16 Q801 TU-µP AFC ON TUNER/ IF	
2	MUTE SIGNAL	 MUTE 14 TU-µP LINE MUTE 42 S-µP MUTE AUDIO	 DEFEAT 14 5V D808 TU-µP DEFEAT 7 DEFEAT 15 9V REG/BAND SELECTOR DEFEAT TUNER/ IF	
3	RESET SIGNAL	 RESET 11 49 RESET 10 S-µP REG/BAND SELECTOR 26 TU-µP	 RESET 9 D840 Q804 40 RESET REG/BAND SELECTOR S-µP 26 RESET TU-µP	
4	5.0V OUT PUT	 A5V 9 A5V TUNING REG/BAND SELECTOR SYSTEM CONTROL etc.	 Q808 A9V 5V REG A5V TUNING SYSTEM CONTROL etc.	
5	CURRENT SOURCE	 40V 14 AC40V 30V 15 ZD801 REG/BAND SELECTOR VT VT 20 Q801 TU-µP TUNER/ IF	 Q811 AC40V CURRENT SOURCE ZD801 VT VT 20 Q802 TU-µP TUNER/ IF	

1. AFC Signal. An Inverter Q801 was eliminated by changing the polarity of output port No.16 in Tu-µP from AFC ON TO AFC $\overline{\text{ON}}$.
2. Mute Signal. Audio Mute signal was supplied to Tuner/IF Mute circuit through the level shift circuit in REG/BAND SELECTOR IC to defeat tuning noise: The Mute signal from Tu-µP was shifted from 5V to 9V signal. However, in VT-1310A/1305A, the Mute signal for defeating tuning noise from Tu-µP is supplied to the Automatic Gain Control circuit in Audio Processing circuit. The Line Mute Signal from S-µP is added to this signal by a diode adder circuit.
3. Reset Signal. In VT-1100A 1105A, $\overline{\text{RESET}}$ signal from REG/BAND SELECTOR IC to reset the µPs during a power source failure was added to Tu-µP directly and also added to S-µP through an Inverter Q804. However. in VT-1310A/1305A, REG/BAND SELECTOR IC has RESET and $\overline{\text{RESET}}$ signals for both µPs.
4. 5.0V Output. In VT-1100A/1105A, the 5V Regulator Q808 supplies A5V to TUNING, SYSTEM CONTROL and etc. circuits. However, in VT-1310A/1305A, REG/BAND SELECTOR IC includes an A5V source.
5. Current Source. In VT-1100A/1105A, the 30V source for VT signal was supplied from current source Q811 and Zener diode ZD801. However, in VT-1310A/1305A, REG/BAND SELECTOR IC also includes a current source circuit for the same purpose.

6-4 VT-1310A/1305A AUDIO CIRCUIT

The audio circuit configuration of the VT-1310A/1305A is very similar to the VT-1100A/1105A. New audio processing IC M5165P which consists of LINE/TUNER input switch, ALC, REC/PB/LINE amp, SP-EQ switches and bias switch is used.

Fig. 6-7 shows the record audio processing circuit and Fig. 6-8 shows the playback audio processing circuit.

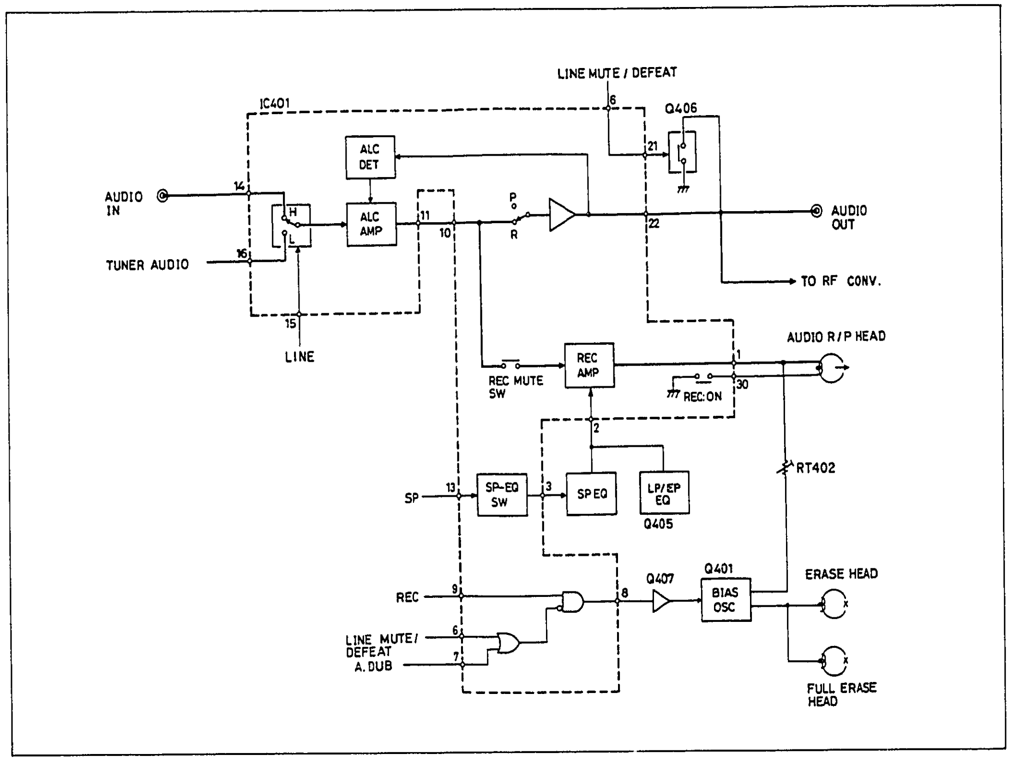

LINE MUTE / DEFEAT
IC401
Q406
ALC DET
AUDIO IN
TUNER AUDIO
H
L
ALC AMP
P
R
AUDIO OUT
TO RF CONV.
LINE
AUDIO R/P HEAD
REC MUTE SW
REC AMP
REC:ON
RT402
SP
SP-EQ SW
SP EQ
LP/EP EQ
Q405
REC
LINE MUTE/ DEFEAT
A.DUB
Q407
Q401
BIAS OSC
ERASE HEAD
FULL ERASE HEAD
14
16
15
11
10
6
21
22
1
30
2
13
3
9
6
7
8

Fig. 6-7 Record Audio Processing Circuit

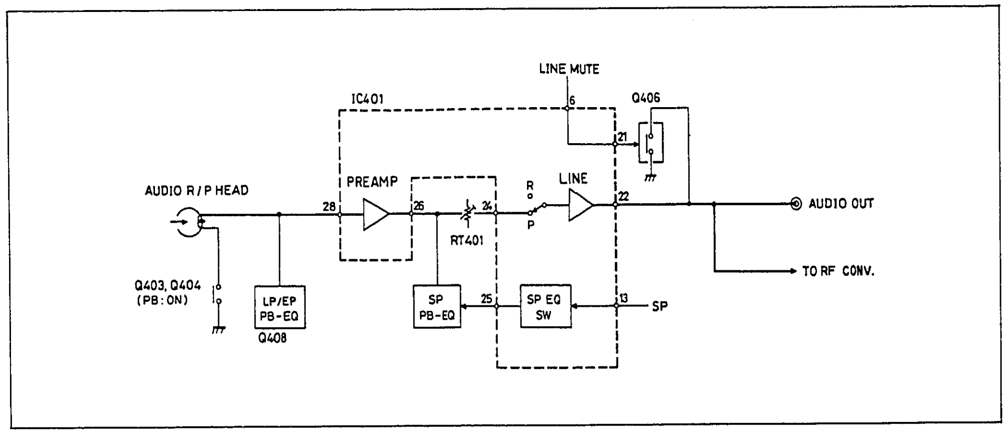

LINE MUTE
IC401
Q406
AUDIO R/P HEAD
PREAMP
R
LINE
P
RT401
AUDIO OUT
TO RF CONV.
Q403, Q404 (PB: ON)
LP/EP PB-EQ
Q408
SP PB-EQ
SP EQ SW
SP
28
26
24
25
6
21
22
13

Fig. 6-8 PB Audio Processing Circuit

HITACHI

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Tel. 312-593-1550

Southern Regional Office
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Tel. 404-763-0360

Western Regional Office
401 West Artesia Boulevard, Compton, California 90220 U.S.A.
Tel. 213-537-8383

HITACHI SALES CORPORATION OF HAWAII. INC.
3219 Koapaka Street. Honolulu, Hawaii 96819, U.S.A.
Tel. 808-836-3621

HITACHI (HSC) CANADA INC.
3300 Trans-Canada Highway, Pointe Claire, Quebec,
H9R 1B1, Canada
Tel. 514-697-9150

Hitachi Sales Centroamericana, S.A.
San Rafael de Escazu, (Apartado 10272), San Jose,
Costa Rica
Tel. 28-2011, 28-0037

Hitachi Sales Corporation de Panama, S.A.
Nuevo Reparto el Carmen, Calle Ramon Arias y Calle B
Edificio Brasil 100, (Apartado 7657) Panama 5
Panama City, Rep. of Panama
Tel. 61-3100, 61-4305

Hitachi Sales de Chile Cia., Ltda.
Av. Mexico, 0183, Casilla 9793, Correo Central
Santiago, Chile
Tel. 774165

HITACHI Ltd. TOKYO JAPAN
Head Office: THE HITACHI ATAGO BLDG.
No. 15-12, 2-Chome Nishi-Shinbashi
Minato-Ku, Tokyo 105, Japan
Tel. Tokyo (03) 502-2111

VT-1100A/1105A TK No. 2508E TOKAI
1310A/1305A

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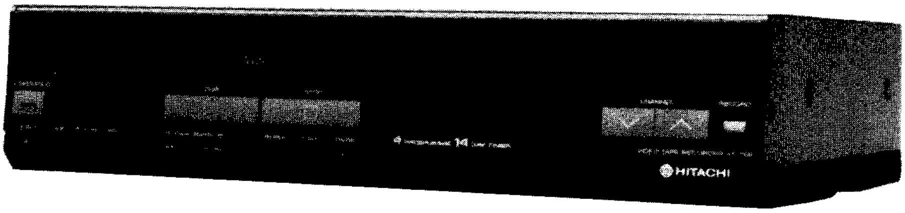
HITACHI
● SERVICE MANUAL

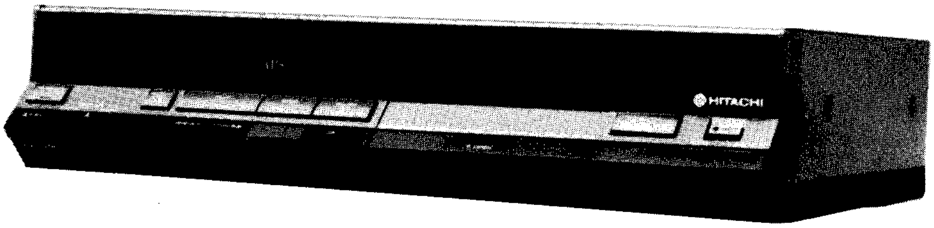
TK **No. 2397E**

VT-110E/120E(CT)

Technical Data



— VT-110E —



— VT-120E —

MC-Service

VHS
THIS VIDEO DECK IS A VHS TYPE VIDEO RECORDER.
FOR PROPER OPERATION, ONLY THE VHS TYPE CASSETTE MUST BE USED.

Differences between VT-110E and VT-120E

MODEL / ITEM	VT-110E	VT-120E
SHAPE OF FRONT PANEL	STRAIGHT FACE	SEMI-SLANT FACE
OPERATING SOUND	——	Pi-SOUND

SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

VIDEO CASSETTE RECORDER

February 1986 **TOKAI WORKS**

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SPECIFICATIONS

ITEM	VT-110E/120E
Format:	VHS PAL Standard
Recording:	Rotary Two-Head Helical Scan Azimuth Recording
Tape Speed:	23.39 mm/sec.
Tape Width:	12.7 mm
Operation Temperature:	5°C to 40°C
Video:	PAL colour (system B & G) & CCIR monochrome signals 625 lines
Recording Time:	240 min. (with Hitachi E-240 cassette)
Aerial Input:	VHF channels 2 — 12 CATV channels S1 — S20 UHF channels 21 — 69
RF Output:	UHF channels 37 (30 — 39 adjustable) (System G)
Video Input:	0.5 to 1.5V p-p 75 ohm Unbalanced
Video Output:	1V p-p 75 ohm Unbalanced
S/N Ratio (Video):	40 dB
S/N Ratio (Audio):	43 dB
Horizontal Resolution:	Colour 240 lines
Audio Input:	−2 dBm 50 Kohm
Audio Output:	−2 dBm 10 Kohm
Audio Frequency Range:	70 Hz to 12 kHz
Power:	AC 220V 50 Hz
Power Consumption:	34W (including timer)
Timer:	24 hour digital indication
Cabinet Size:	435 mm(W) x 95 mm(H) x 324 mm(D)
Weight:	7.0 kg
Accessory Included:	1 — Aerial cable 2 — Programme sheets 1 — Infrared Remote control unit

* Design and specifications are subject to change without notice.

SAFETY PRECAUTIONS

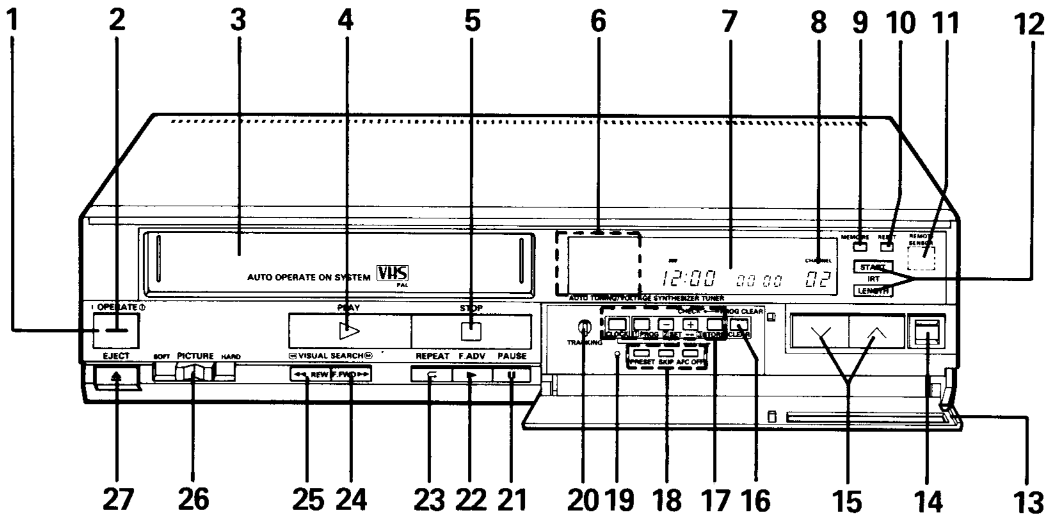
The following precautions should be observed when servicing.

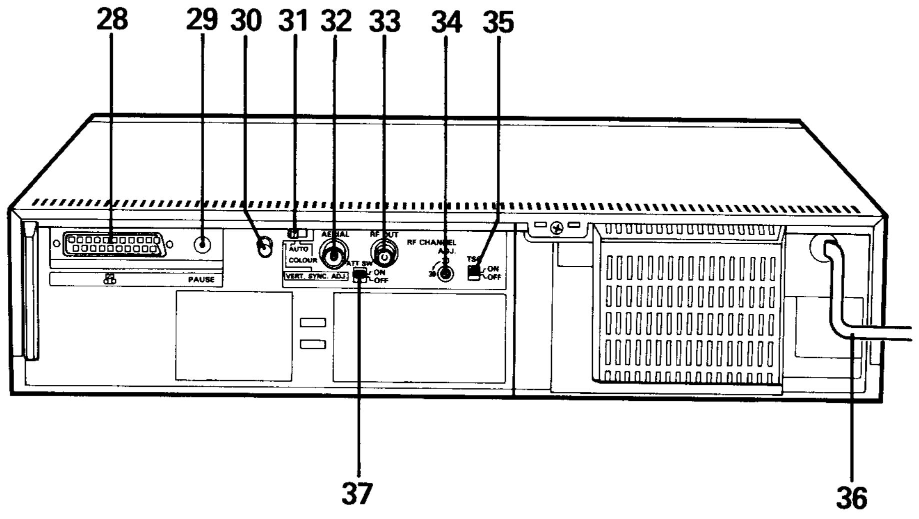
1. Since many parts in the unit have special safety-related characteristics, always use genuine Hitachi replacement parts. Especially critical parts in the power circuit block should not be replaced with other makers'. Critical parts are marked with ⚠ in the schematic diagram and circuit board diagram.
2. Before returning repaired unit to the customer, the service technician must thoroughly test the unit to ascertain that it is completely safe to operate without danger of electrical shock.

LIST OF DIFFERENCES

	ITEM		VT-110E/120E	VT-63E
FEATURES	HQ (HIGH QUALITY)		USED	UNUSED
	TRICK PLAY		○ VISUAL SEARCH ○ PAUSE ○ F. ADV (By Remote Control) ○ REPEAT	○ VISUAL SEARCH ○ PAUSE
	AUTO OPERATE ON FUNCTION		YES	NO
	NOISE LOCK SEARCH FUNCTION		YES	YES
	REMOTE CONTROL		WIRELESS	WIRED
	TIMER RECORDING PROGRAMS		4 PROGRAMMES/2 WEEKS	4 PROGRAMMES/2 WEEKS
	TIMER BACKUP POWER		ABOUT 5 MINUTES	ABOUT 5 MINUTES
	TIMER PROGRAMMED TIME DISPLAY		START AND STOP SIMULTANEOUSLY	START AND STOP SEQUENTIALLY
	IRT		CAN SET START TIME	CAN SET RECORDING TIME ONLY
	TAPE COUNTER INDICATOR		INDEPENDENT	CLOCK/COUNTER SWITCHING
	MEMORY STOP OPERATION MODE		REWIND AND FORWARD	REWIND
	CHANNEL TUNING FUNCTION		VOLTAGE SYNTHESIZER (AUTO TUNING)	VOLTAGE SYNTHESIZER
	INPUT SELECT SWITCH		NONE	YES
	PLAYBACK PICTURE CONTROL		HIGH FREQUENCY CONTROL	HIGH FREQUENCY CONTROL
	ONE BUTTON RECORDING		YES	NO
CHASSIS	BASIC CHASSIS TYPE		UY	UX
	CYLINDER MOTOR		THREE-PHASE OUTER ROTOR FG: 300 Hz	SINGLE-PHASE FLAT FG: 200 Hz
	VIDEO HEAD		2 HEADS CH-1/CH-2: 65 μm CONNECTOR TYPE	2 HEADS CH-1/CH-2: 65 μm SOLDERED TYPE
	HEATER		NONE (USED HEAT SINK)	YES
	DEW SENSOR		NO	NO
MAIN CONTROL ICs	VIDEO SYSTEM	Y-SIGNAL PROCESS CHROMA SIGNAL PROCESS REC/PB AMP AND CORRECTOR PICTURE CONTROL	HT4727 (IC203) HT4539 (IC301) HT4708 (IC205) HA11852 (IC1) MSM6965RS (IC204)	HT4238 (IC202) HT4239 (IC203) HT4207 (IC201) —— ——
	AUDIO SYSTEM	REC/PB AMP	BA5115L (IC402)	BA5115L (IC402)
	SERVO SYSTEM	SPEED/PHASE CONTROL CYLINDER MOTOR DRIVE CAPSTAN MOTOR DRIVE TRICK PLAY CONTROL	M54898P (IC601) HA13403 (IC1651) M54648L-B (IC602) ——	HA11843 (IC604) HA13430A (IC601) M54548L-A (IC603) ——
	SYSTEM CONTROL	SYSTEM CONTROL μP LOADING MOTOR DRIVE	HD614042SD37 (IC901) M54649L (IC902)	HD38820L26 (IC901) M54549L (IC902)
	TIMER	TIMER μP	HD614045SD53 (IC751)	M50757-681SP (IC101)
	CH-TUNING SYSTEM	TUNING μP BAND SWITCHING	M50161-354SP (IC801) LA7934 (IC802)	M50161-056SP (IC701) LA7910 (IC703)
	POWER SUPPLY	REGULATOR	STK5471 (IC851)	STK5451 (IC151)

CONTROLS AND FUNCTIONS — VT-110E —

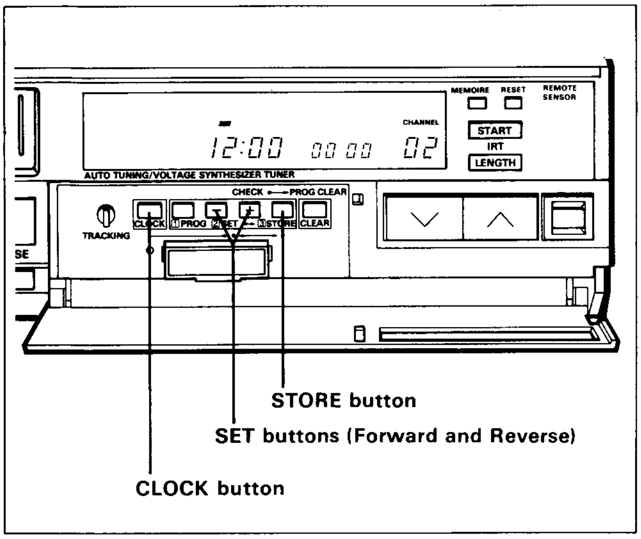




1. **OPERATE SWITCH**
   Turn system power on and off.
2. **OPERATE INDICATOR**
3. **CASSETTE COMPARTMENT**
   Insert a cassette in through the door, and loading will be completed automatically.
   Note: Power is turned on automatically when the cassette is loaded.
4. **PLAY BUTTON**
5. **STOP BUTTON**
   The STOP button must be pressed between "RECORD" and any other operation.
6. **MODE INDICATORS**
   - " ▭ " appears when a cassette is in the compartment.
   - "PLAY" appears during the playback mode.
   - "REC" appears during the record mode.
   - "◀◀" appears during the rewind mode and flashes during rewind visual search mode.
   - "▶▶" appears during the fast forward mode and flashes during forward visual search mode.
   - " ❚❚ " appears during the play/record pause mode.
   - " ⏲ " appears when turning the power off after programming the timer.
7. **DIGITAL DISPLAY**
   This shows the time with a 24-hour display and shows the tape position.
8. **CHANNEL INDICATOR DISPLAY**
   This shows the channel number corresponding to the channel selected.
9. **MEMORY BUTTON**
   Press this button so "M" is indicated in the display, then fast forward or rewind the tape. The tape stops when the counter reaches approximately "0000".
   Note: Press the button again to switch off the "M" indicator.
10. **COUNTER RESET BUTTON**
    To reset counter to "0000".
11. **INFRARED RAY RECEIVING SECTION**
    Receives infrared rays from remote control unit.
12. **INSTANT RECORDING TIMER BUTTONS (IRT)**
    This allows unattended recording.
    Timer will switch the VTR off automatically at a preselected time. This is convenient when you go out during recording.
13. **SECONDARY CONTROL DOOR**
14. **RECORD BUTTON**
    Press RECORD button to record.
15. **CHANNEL SELECT BUTTONS**
    Select the channels you wish to view or record by pressing these buttons.
    And you can also select the "AUX" position* by pressing this button to record or watch the programme input at the PERI jack.
    * One channel position either higher or lower outside the range of your preset channels.
16. **PROGRAMME CLEAR BUTTON**
    Press the button to clear the programming information.
17. **TIME SET BUTTONS**
18. **CHANNEL PRESET BUTTONS**
19. **TIMER RESET SWITCH**
    Press this switch if the digital display malfunctions or no display appears to reset the display. Set the correct present time for the clock then programme the timer.
20. **TRACKING CONTROL**
    To minimize noise in playback.
21. **PAUSE BUTTON**
    Press to pause during recording.
    Press to view a still picture during playback.
    Press again to release.
22. **FRAME ADVANCE BUTTON**
    When you hold FRAME ADVANCE button down during still playback mode, tape will be played back frame by frame. Operates only after PAUSE button has been pressed.
23. **REPEAT BUTTON**
    Press this button after pressing the PLAY button to repeat the scene you have just viewed during playback.
    The tape is rewound to the position where PLAY button was pressed, then the tape is played back from that position.
24. **FAST FORWARD/VISUAL SEARCH BUTTON**
    Press to activate fast forward.
    Press this button during playback and forward playback picture at high speed can be seen.
25. **REWIND/VISUAL SEARCH BUTTON**
    Press to start rewind.
    Press this button during playback and reverse playback picture at high speed can be seen.
26. **PICTURE CONTROL**
    Adjust the picture so it is easy to see.
27. **EJECT BUTTON**
    Press to remove cassette. The STOP button must be pressed before "EJECT".
28. **PERI JACK**
    For connection with a TV with a PERI or DIN jack using an exclusive cable.
29. **CAMERA PAUSE JACK**
    Connect Camera pause cable.
30. **VERTICAL SYNC. ADJUSTMENT CONTROL**
    If you see vertical shaking on the TV screen in the still playback mode, rotate this control to minimize shaking.
31. **AUTO/COLOUR SWITCH**
    AUTO: Circuits are automatically switched to colour or black/white mode. Set to this position when playing or recording PAL signal.
    COLOUR: When recording PAL signal in the area very far from broadcasting station, the recorded picture may lose colour. In this case set to this position in recording and playback.
32. **AERIAL INPUT SOCKET**
    Connect external aerial.
33. **RF OUTPUT**
    Connect to TV aerial input.
34. **RF CHANNEL CONTROL**
    Turn TSG ON/OFF switch to "ON" and rotate this control to set the video channel correctly.
35. **TSG ON/OFF SWITCH**
    Set to ON and check that the video channel of your TV set is correct. After setting, set this switch to OFF.
36. **MAINS LEAD**
37. **ATTENUATER SWITCH**
    Generally set to the NORMAL position.
    Set to "ATT-ON" when interference occurs in an area with a strong signal.

CLOCK TIME SETTING

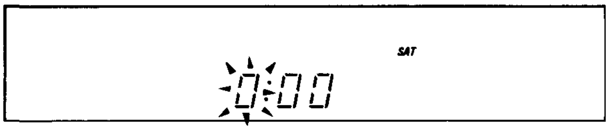
The built-in digital clock is based on a 24 hour cycle and gives you a constant readout of the time and day.


MEMOIRE
RESET
REMOTE SENSOR
CHANNEL
12:00 00 00 02
START
IRT
LENGTH
AUTO TUNING/VOLTAGE SYNTHESIZER TUNER
CHECK
PROG CLEAR
TRACKING
CLOCK
PROG
SET
STORE
CLEAR
STORE button
SET buttons (Forward and Reverse)
CLOCK button

- When the MAINS lead is plugged in for the first time, "— —: — —" will appear on the display.

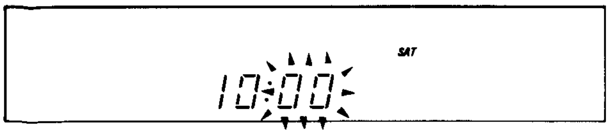
1. Press the CLOCK button.
   "SUN" flashes on and off and "0:00" lights.

2. Press the SET button (Forward or Reverse) to select the present day of the week.
   Hold the button down to advance rapidly.
   When the present day of the week appears, press the STORE button. "0" hour starts flashing.



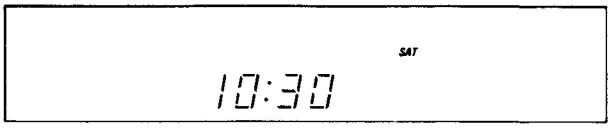
   For example, the above diagram shows that Saturday (SAT) has been set.

3. Press the SET button (Forward or Reverse) to set the present hour.
   Hold the button down to advance rapidly. Press the STORE button when the present hour appears.
   "00" minutes starts flashing.



   For example, the diagram shows that "10" hour has been set.

4. Press the SET button (Forward or Reverse) to set the minute.
   Hold the button down to advance rapidly. Press the STORE button when the present minute appears.



   For example, the diagram shows that "30" minutes has been set.

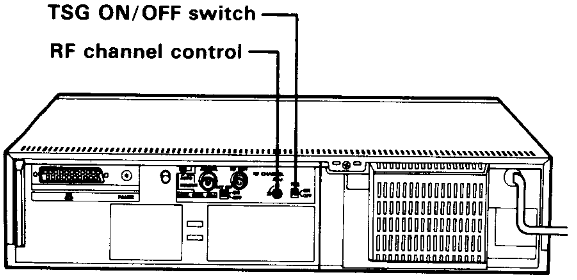
Now the clock has been set to the correct time of day.

Notes:

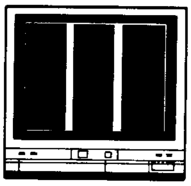
- This VTR has a built-in power failure compensation circuit. If power interruption of less than 5 minutes occurs, the clock time and programming will not be lost.
- The digital display is bright when the OPERATE switch is turned ON and automatically becomes dim when the switch is off.

VIDEO CHANNEL SETTING

The RF converter changes the video and audio signals from a previously recorded video tape during playback to the same type of signal used for TV broadcasts. The RF converter output in this unit is pre-set prior to shipment to UHF channel 37.



1. Turn the TV on and select an unused channel (CH37) (in some cases this may be marked A/V).
2. Turn the OPERATE switch on.
3. Set the TSG ON/OFF switch to "ON". Then tune the TV until the test pattern shown below is received.



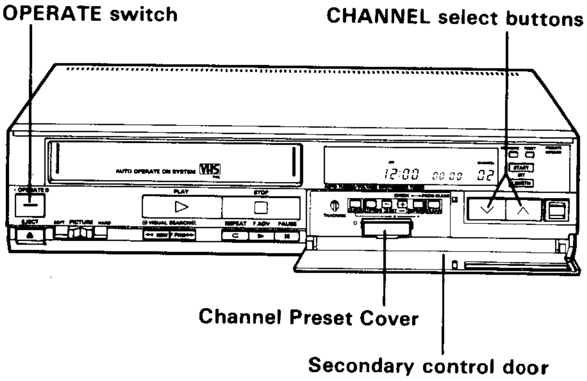
4. If it is not possible to correctly tune to the test pattern or channel 37 is used for broadcasting in your area, adjust the RF converter output with the RF channel control using a small screwdriver and re-adjust your TV until the test pattern is observed. For higher channel numbers, turn counterclockwise. For a lower channel, turn clockwise.
5. Having completed the adjustment, set the TSG ON/OFF switch to "OFF".

When connecting the VTR to a TV set provided with auto-tuning and the video channel cannot be set, operate as follows:

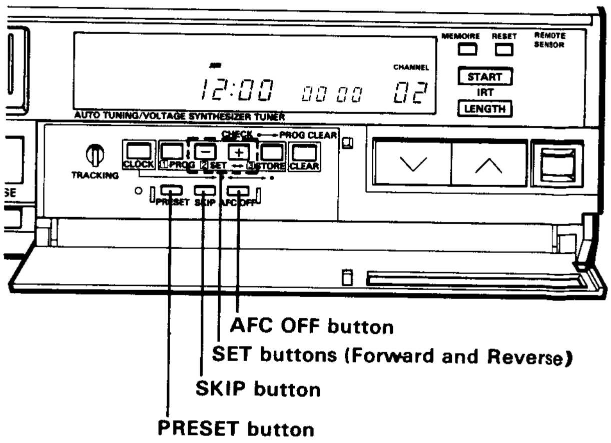
1. Remove the aerial cable from the AERIAL terminal on the VTR.
2. Leave the TSG ON/OFF switch "OFF".
3. Playback a blank tape.
4. Press the PAUSE button to obtain the pause mode.
5. Press the Auto-tuning button.
6. Auto-tuning starts and it stops at video channel 37. **Note:** The auto-tuning indicator of the TV set changes to an exact tuning indicator.
7. Set the channel memory of the TV to ON and store the channel which was set in item 6.
8. Set the TSG ON/OFF switch to "ON" and check that the picture appears on the TV screen. Now, the video channel of TV has been set properly.
9. Return the TSG ON/OFF switch to "OFF".
10. Reconnect the aerial cable to the VTR.

PRE-TUNING OF BUILT-IN TV TUNER

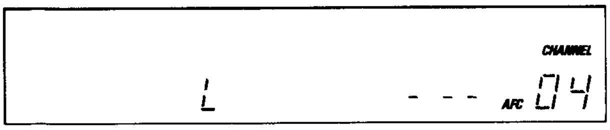
This VTR incorporates a complete television tuner with the required tuning controls. Once you have pre-tuned to preferred stations, you can select any of them by merely pressing the CHANNEL select button.



1. Turn the TV on and select the pre-tuned video channel.
2. Turn the OPERATE switch of the VTR on.
3. Open the Secondary control door to access the Pre-tuning controls.
4. Remove the Channel Preset Cover.

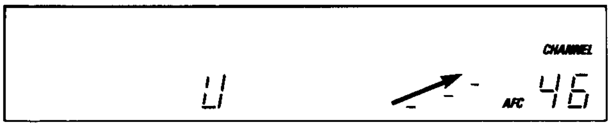


5. Press the PRESET button once. The display indication changes from the clock time display to the band indicator display. **Note:** Pressing the button twice will lock the display. If you have pressed it twice, press it once more.
6. Press the CHANNEL select button on VTR to select the channel to be memorized. **Notes:**
   1. The Channel Number Display can be now consecutively selected from "00" through "73" and then "95" through "99" and "AUX" by pressing the CHANNEL select button either upward or downward. In this case, Channel Number may be any number.
   2. When "AFC" is not indicated in the display, press AFC OFF button to display "AFC".

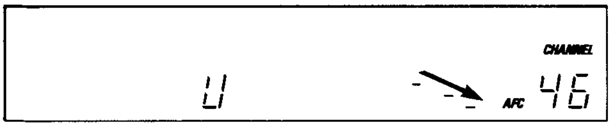


For example, the above diagram shows that channel 4 has been selected.

7. Press the SET button (Forward or Reverse) to start tuning.
   At a station that is broadcasting, the picture appears on the TV screen. If the station received is different from the channel to be preset, press SET button (Forward or Reverse) again.
   At the next station, the searching will stop and the new station can be preset. Repeat this until the desired station is reached. By repeating this, the Band indicator on the display will change in sequence L, H, U, L....
   Notes:
   - Press SET button (Forward); channels are searched in the order, VHF (1 – 12) → CATV (S1 – S20) → UHF (21 – 69), and "–" appears in sequence in the direction of the arrow during searching.



   - Press SET button (Reverse); channels are searched in the reverse order to the above, and "–" appears in sequence in the direction of the arrow.



8. Follow the same steps as explained in steps 6 and 7 above for other channels.
   You can preset up to 79 channels in memory.
9. After having completed tuning all channel memories you want, press the PRESET button once again.

These channels preset in memory as shown in the above can be selected by the CHANNEL select buttons on the VTR.

The provided sheet is used to list the programmes to which you pre-tune your VTR. List the programmes and paste the sheet on the side panel, etc. so as not to hinder you when you operate the VTR.

AFC (Automatic Frequency Control)

Since this unit has an AFC circuit, when a channel is preset following the above procedure, the AFC turns on automatically and you can receive the signal in optimum condition.

If a TV channel signal is marginal due to graininess or ghosting, the picture may sometimes be improved by manually tuning for best picture and then defeating the AFC action. To turn AFC off, follow the procedure below.

1. Select the desired channel by pressing CHANNEL select button.
2. Press the PRESET button once.
3. Press the AFC OFF button. "AFC" disappears from the display.
   Note: Pressing the button once again will turn the AFC on.
4. Press the PRESET button once again.

Channel selection

The channel up and down controls on the VTR permit advancing the tuner directly to the next higher or lower programmed channel.

Eliminating unwanted preset channels

You can rearrange the desired channels by eliminating unwanted preset channels for channel up/down tuning.

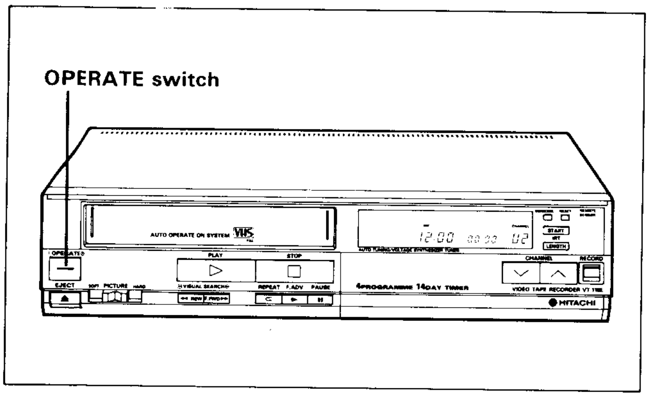
1. Press the PRESET button once.
2. Press the CHANNEL select buttons until an unwanted channel is found.
3. Press the SKIP button once.
   Sound will go off indicating the channel has been erased from memory.
4. Repeat steps 2 and 3 until all unwanted channels have been erased.
5. After eliminating them, press the PRESET button once again.

Note: To restore the erased channel, repeat the above steps 1 through 3.

TIMER RECORDING

The programmable electronic clock/timer permits the unattended recording of 4 preselected programmes within a period of 14 consecutive days, including the same programme(s) repeated on every day and the same programme(s) every week. It turns the unit on and off and selects the channel automatically.

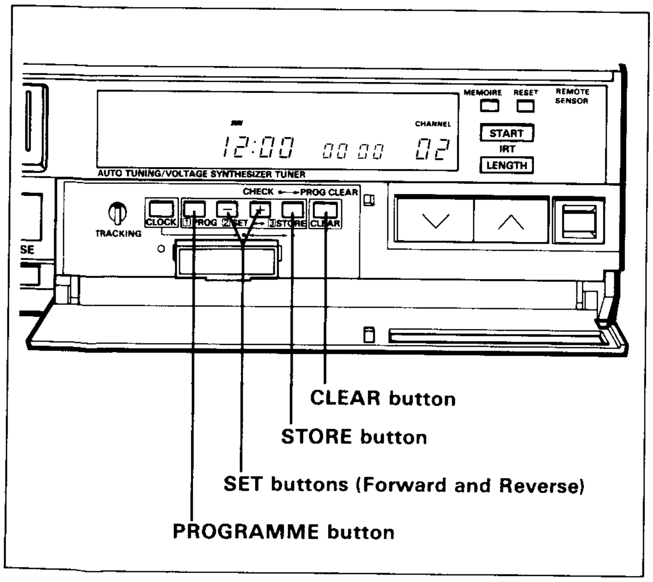
Preparations for timer recording


OPERATE switch
AUTO OPERATE ON SYSTEM VHS
12:00 00 00 02
HITACHI

- Your TV does not have to be on to make a recording because the VTR records TV programmes without the aid of your TV. Its only use is for monitoring.

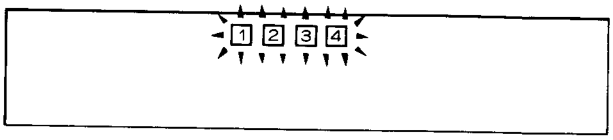
1. Make sure that the clock shows the present time and day correctly.
2. Insert a cassette.
   Be sure to check that the record safety tab is not missing. If the record safety tab is missing, recording will not begin.
3. Programme the timer.

Programming the timer for unattended recording
For unattended recording the timer needs to know what **day** to make the recording, the **time to start**, the **time to stop**, and the **channel to be recorded**.


MEMOIRE
RESET
REMOTE SENSOR
CHANNEL
12:00 00 00 02
START
IRT
LENGTH
AUTO TUNING/VOLTAGE SYNTHESIZER TUNER
CHECK ←→PROG CLEAR
CLOCK
PROG
SET
STORE
CLEAR
TRACKING
CLEAR button
STORE button
SET buttons (Forward and Reverse)
PROGRAMME button

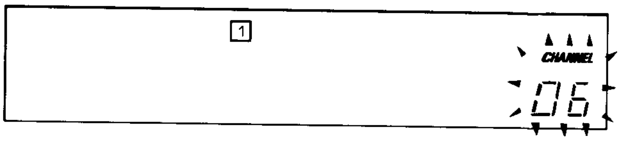
Note: If you input erroneous information by mistake when programming the timer, press the CLEAR button and input the correct information again.

1. Press the PROGRAMME button.
   Programme indicators (1 through 4) flash to indicate which memory positions have not been programmed. If a memory has been programmed, its indicator will not flash.



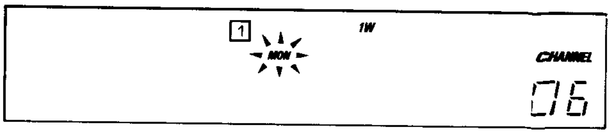
Note: You should determine which memory positions have not been programmed before entering new programming information. New information automatically erases previous programming.

2. Press the SET button (Forward) until the desired programme indicator lights. Programme indicators (1 through 4) light, in sequence, across top of digital display. Press the STORE button when the desired programme number is displayed. Channel number starts flashing.

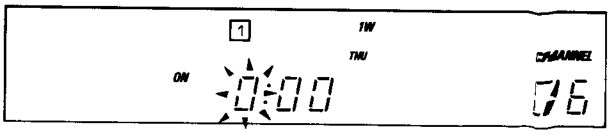

1
CHANNEL
06

For example, above diagram shows programme "1" has been set.

3. Choose the channel to be recorded by pressing the SET or CHANNEL select button. Then press the STORE button.
   "1W" appears and the present day flashes.


1
MON
1W
CHANNEL
06

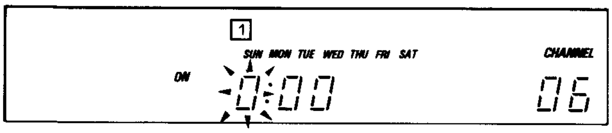
4. Press the SET button (Forward or Reverse) to select the day of recording. Make sure desired Week indicator (1W or 2W) lights. Continuing forward will advance timer to Week Two.
   Press the STORE button after selecting the day of recording. "0" hour starts flashing.


1
1W
THU
ON
0:00
CHANNEL
06

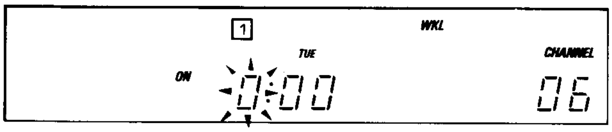
For example, above diagram shows recording on Thursday within 1 week from today.

Notes :

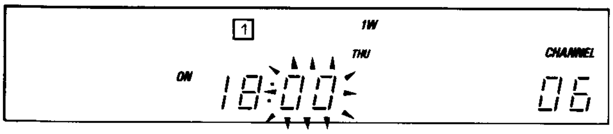
1. To record same time every day of the week: Press the SET button (Forward or Reverse) until all day indicators light. Hold down the button to advance rapidly. Then press the STORE button.



2. To record on a specified day at the same time each week: Press the SET button (Forward or Reverse) until the "WKL" indicator lights. Hold down the button to advance rapidly. Then press the STORE button.

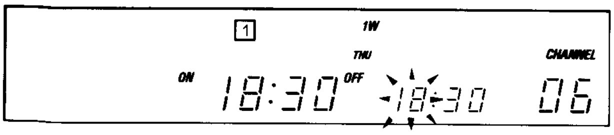


5. Select the hour for recording to start by pressing the SET button (Forward or Reverse). Hold down the button to advance rapidly. Press the STORE button after selecting the hour for recording to start. "00" minutes starts flashing.



For example, the above diagram shows "18" hours has been set.

6. Select the minutes for recording to start by pressing the SET button (Forward or Reverse). Hold down button to advance rapidly. Press the STORE button after selecting the minute for recording to start. "OFF" will appear and "18" hour starts flashing.



For example, the above diagram shows "30" minutes has been set.

7. Select the hour and minute to stop recording in the same procedures described in steps 5 and 6. Be sure to press the STORE button after selecting the minute.

Now, one programming has been completed. After few seconds the display returns the clock time display together with letters "[1]" automatically.

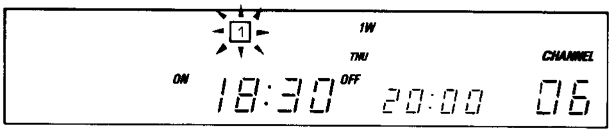
8. Turn off the OPERATE switch. The "⊙" indicator will come on.

Notes:

1. If the erase prevention tab is removed, the cassette is ejected automatically and "⊙" indication will flash. Stick a piece of cellophane tape over the erase prevention hole on the cassette to enable recording.
2. The "⊙" indication will flash, if a cassette is not inserted.

To clear a programme

1. Press the SET button (Forward) until desired programme indicator flashes. Then start and stop time appear on the display.

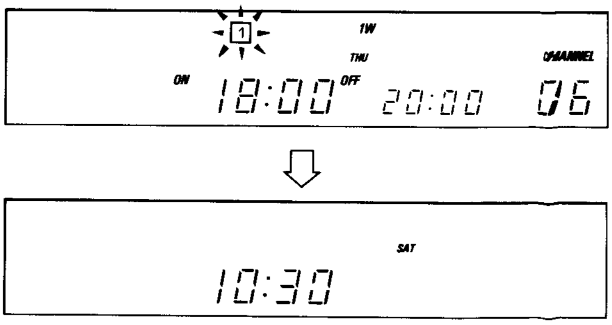


2. Press the CLEAR button. The display returns the clock time display to show that the programming has been cleared. Be sure to press the CLEAR button while the display shows the start and stop time. The programming does not clear if the CLEAR button is pressed when the display returns the clock time display.

To check programming

Press the SET button (Forward).

The programme indicator "[1]" flashes. If the programme No. 1 has been already programmed, both start and stop times are displayed in a few seconds. The display then automatically returns to the present time of day.

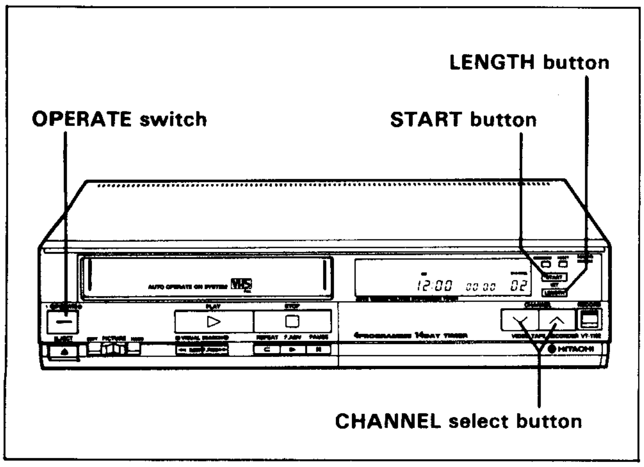


Programming errors

If programmes overlap, the VTR will select the programme with the earliest start time. When that programme is over, the VTR will switch to the next programme. If the start times are the same, the VTR will select the programmes in numerical order.

INSTANT RECORDING TIMER (IRT)

Instant Recording Timer allows you to make simplified timer recording without using the programme timer. There are two simplified methods as explained below.



■ FOR IMMEDIATE RECORDING

1. Insert the cassette (one with the erase prevention tab intact) into the cassette loading door.
2. Press CHANNEL select button to select the channel to be recorded.
3. Press LENGTH button to set the timer to "0:00". Then press LENGTH once again to indicate the recording time on the display. The time changes in hours and minutes in the order of 0:30, 1:00, 1:30, 2:00, 3:00 and 4:00 every time the button is pressed. Recording starts when 0:30 is displayed. During recording, the remaining time is displayed.
4. At the end of recording the display reads 0:00; the VTR will automatically stop recording.

Note: The IRT feature does not operate during play and after a program timer recording has started. During rewind mode, the IRT recording will automatically start after the tape is rewound fully to the end.

■ FOR SIMPLIFIED TIMER RECORDING

1. First perform Steps 1 and 2 of "FOR IMMEDIATE RECORDING".
2. Press START button to select the start time. Each press will change the clock display (the start time) by increments of 10 minutes from the nearest 10 minutes of the hour.
3. Press LENGTH button for the recording time. The counter display is reset to hours and minutes in the order of 0:00, 0:30, 1:00, 1:30, 2:00, 3:00 and 4:00 every time the button is pressed.
4. Press OPERATE switch off, and the "◷" indication will appear on the Display. The recording will start at the time you have selected and will automatically stop when the recording time display reads "0:00".

Notes:

1. The recording time can be extended any time during IRT by pressing LENGTH button . The recording time display will be reset to 0:30, 1:00, 1:30, 2:00, 3:00 or 4:00 as selected.
2. To stop the VTR during IRT, press LENGTH button until the recording time display reads 0:00, or press OPERATE switch and the STOP button within ten seconds.
3. To change the IRT program, the previous information must be first cleared.
4. If IRT and the program timer recording overlap, the former will override the latter.

To recall the IRT program

Press START or LENGTH button for recalling the start time and the recording time. In about 8 seconds the displays return to the present time of day.

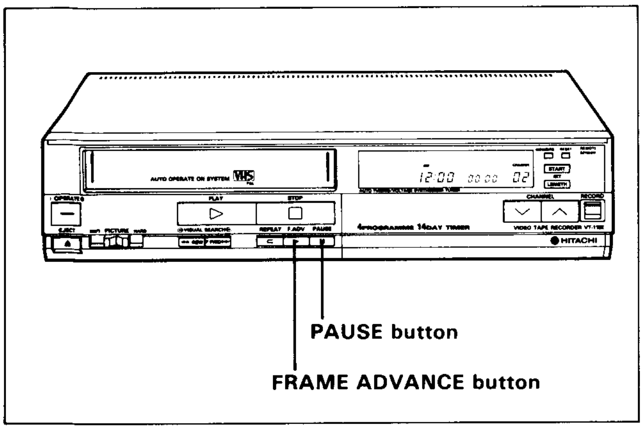
Note: To recall the start time or the recording time, press LENGTH button only once. Pressing more will change the recording time and cause a need for resetting.

To cancel Instant Recording

Press LENGTH button as many as may be required to indicate "0:00" on the display. After approximately 8 seconds the display will return to the present time of day, and IRT has been now cleared.

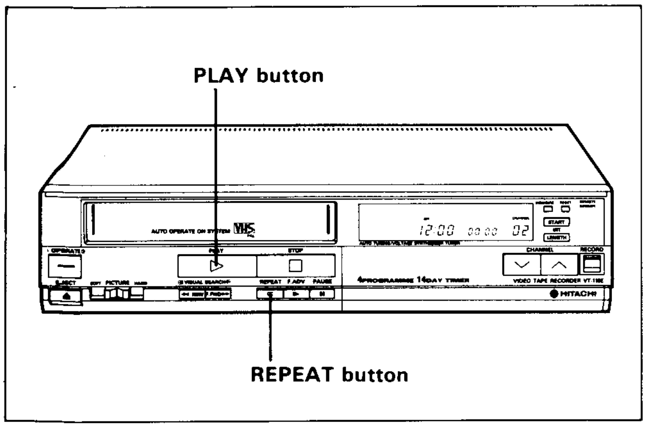
Note: OPERATE switch may be on or off.

Frame advance



When you hold FRAME ADVANCE button down during still playback mode, tape will be played back frame by frame. Operates only after PAUSE button has been pressed.

Repeat function



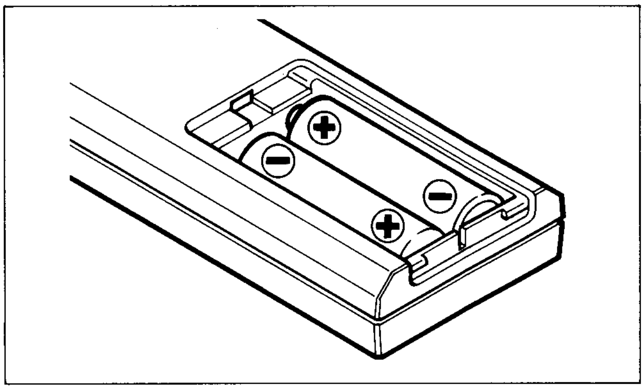
Use this function to repeat the scene you háve just viewed during playback.

1. During playback, press PLAY button at the scene where you want the repeat of the playback to start. The playback continues.
2. Press REPEAT button. The tape is automatically rewound to the position where PLAY button was pressed, and playback is repeated.

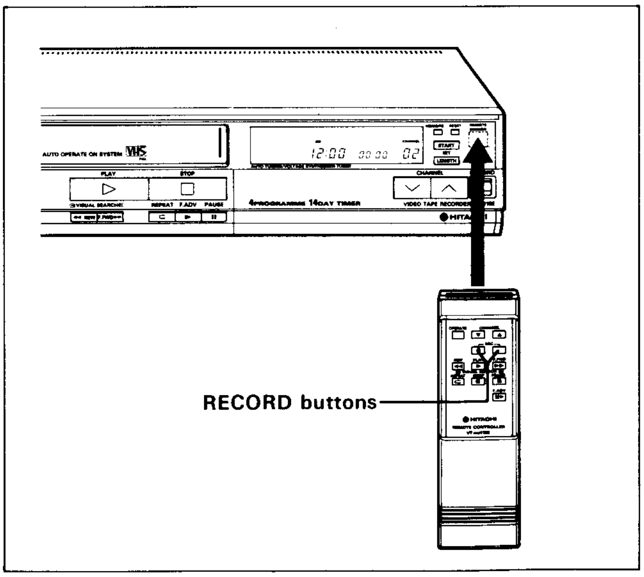
REMOTE OPERATION

You can operate the VTR from a distance using the Infrared Remote Control unit which performs the same functions as the corresponding buttons on the VTR — except for its RECORD buttons.

Power source of infrared remote control unit
The infrared remote control unit is powered by two batteries (size IEC standard R6). The life of the batteries is about a year although it depends on the numbers of times the unit is used. Replace the batteries when operation is not possible or when the distance becomes too small.

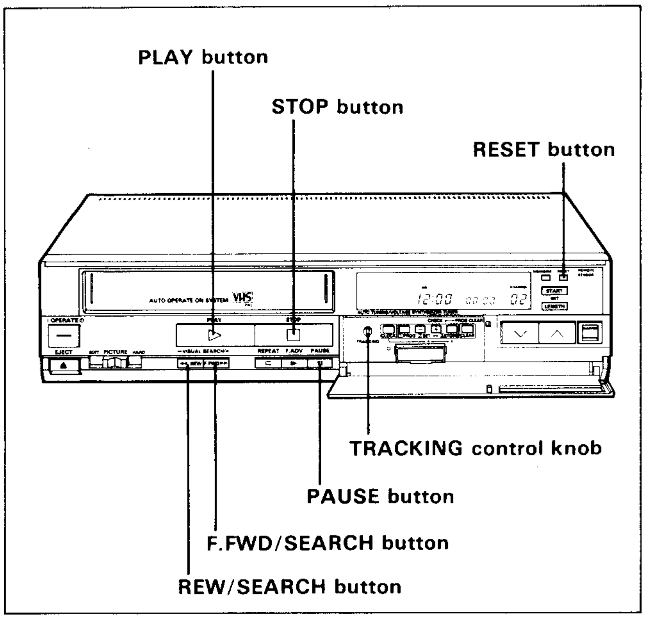


Operation of remote control
To use the infrared remote control unit aim it at the receiver on the front panel of the VTR.



Press RECORD buttons simultaneously on the remote control unit to record.
Note: The infrared rays will bounce off the walls and eventually reach the receiver on the VTR, but for best results transmit rays directly to the receiver.

PLAYBACK



1. Turn the TV set on and select the video channel.
2. Insert the cassette.
3. Press the PLAY button.
4. Press the STOP button to stop playback.

Tracking control adjustment

When playing prerecorded tapes or those recorded on units other than your own, black and white streaks may appear on your TV screen. If this occurs, adjust the TRACKING control until the streaks disappear. When playback of this particular tape is over, readjust the TRACKING control to its original position. The original position is normally in the center position.

Tape counter

This indicates the amount of video tape transported as a number.

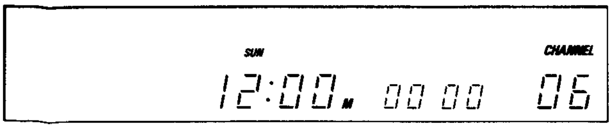
Press the RESET button to set the counter reading to "0000" when starting recording or playing back.

Note the number on the Tape counter at the beginning and end of each programme you record. This will allow you to use the counter to find the desired programme later.

Counter memory function

This is useful if there is a section of tape you want to view immediately after recording or you want to return to the same point several times.

1. Begin recording or playing back a tape.
2. At the point where you want playback to begin, reset the tape counter to "0000" by pressing the RESET button.
3. Press MEMORY button, and the "M" appears on the Display.



4. Continue to play or record.
5. Press the STOP button when recording or playback finishes.
6. Press the REWIND button.

The tape will automatically stop at the pre-selected "0000" position.

Actually, so that you won't miss the very first part of the programme to be viewed, the tape will stop slightly prior to "0000" at approximately the "9997" position.

Note: The counter memory function will also operate during fast-forwarding mode.

Automatic rewind

The VTR automatically rewinds the tape when the end of the tape is reached.

Rewind shut off

If OPERATE switch is pressed during rewind operation, power will be turned off automatically after the tape has been completely rewound.

Still playback

Press the PAUSE button to stop the picture on the screen during playback.

During still playback, press the PAUSE button to return to normal playback or the STOP button to stop the tape.

Notes:

- If you see vertical shaking on the TV screen in the still playback mode, rotate the VERT. SYNC. ADJ. control on the rear of the VTR to minimize shaking.
- When the still playback mode continues for about 5 minutes, the VTR switches to the stop mode automatically to prevent damage to the tape.
- The playback picture will have some noise in the still playback mode.

Visual search

This allows you to view the picture from a recorded tape at high speed in both the forward and reverse directions.

Press the PLAY button to play a tape, then press either the VISUAL SEARCH button REW or F.FWD. Pictures can be viewed at high speed in either the forward or reverse direction.

Note: The playback picture will have some noise in the visual search mode.

DISASSEMBLY

1. NAMES AND LOCATIONS OF CIRCUIT BOARDS

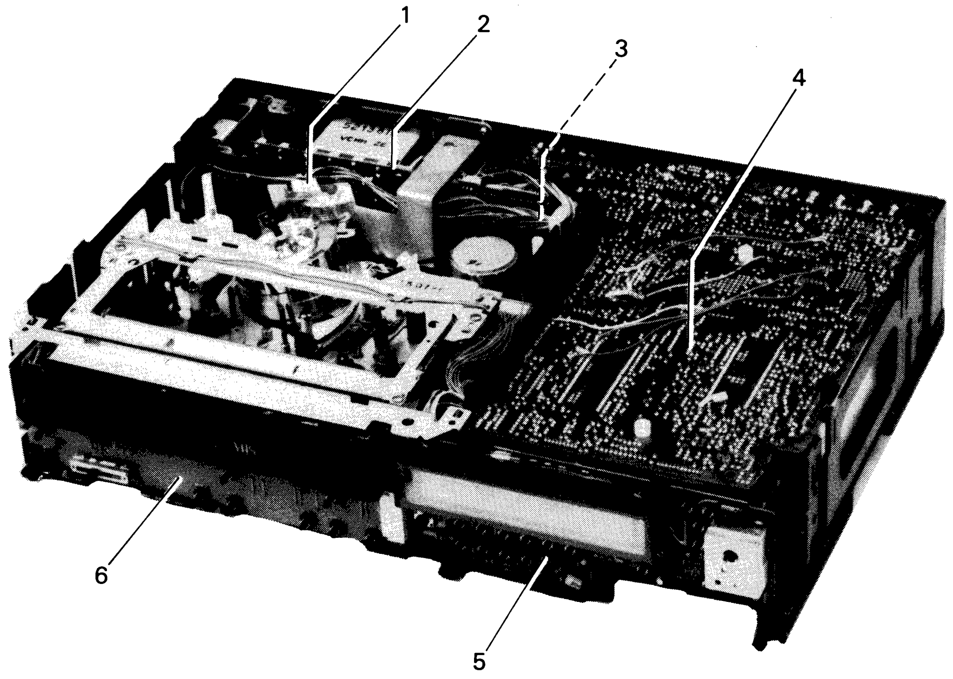


Fig. 1 Top View

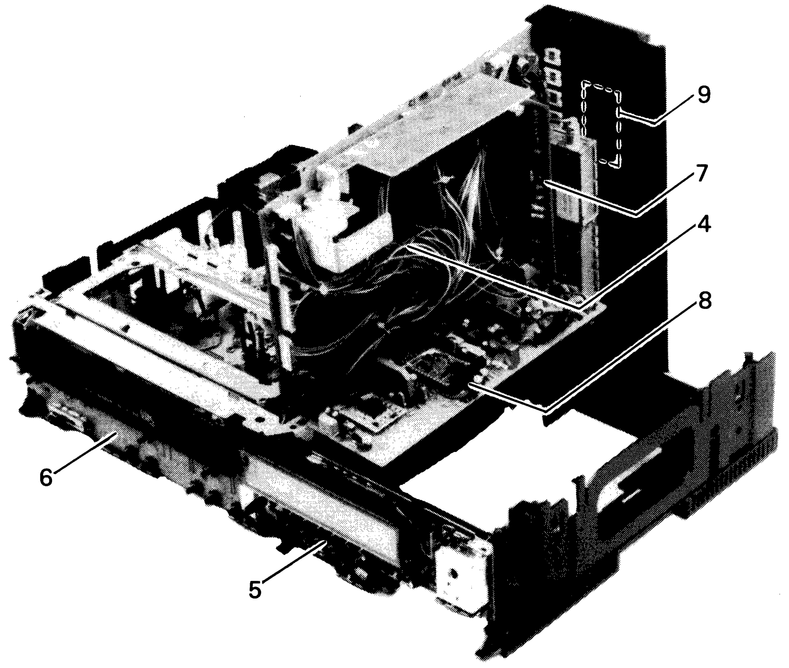


Fig. 2 Top View (with main circuit board open)

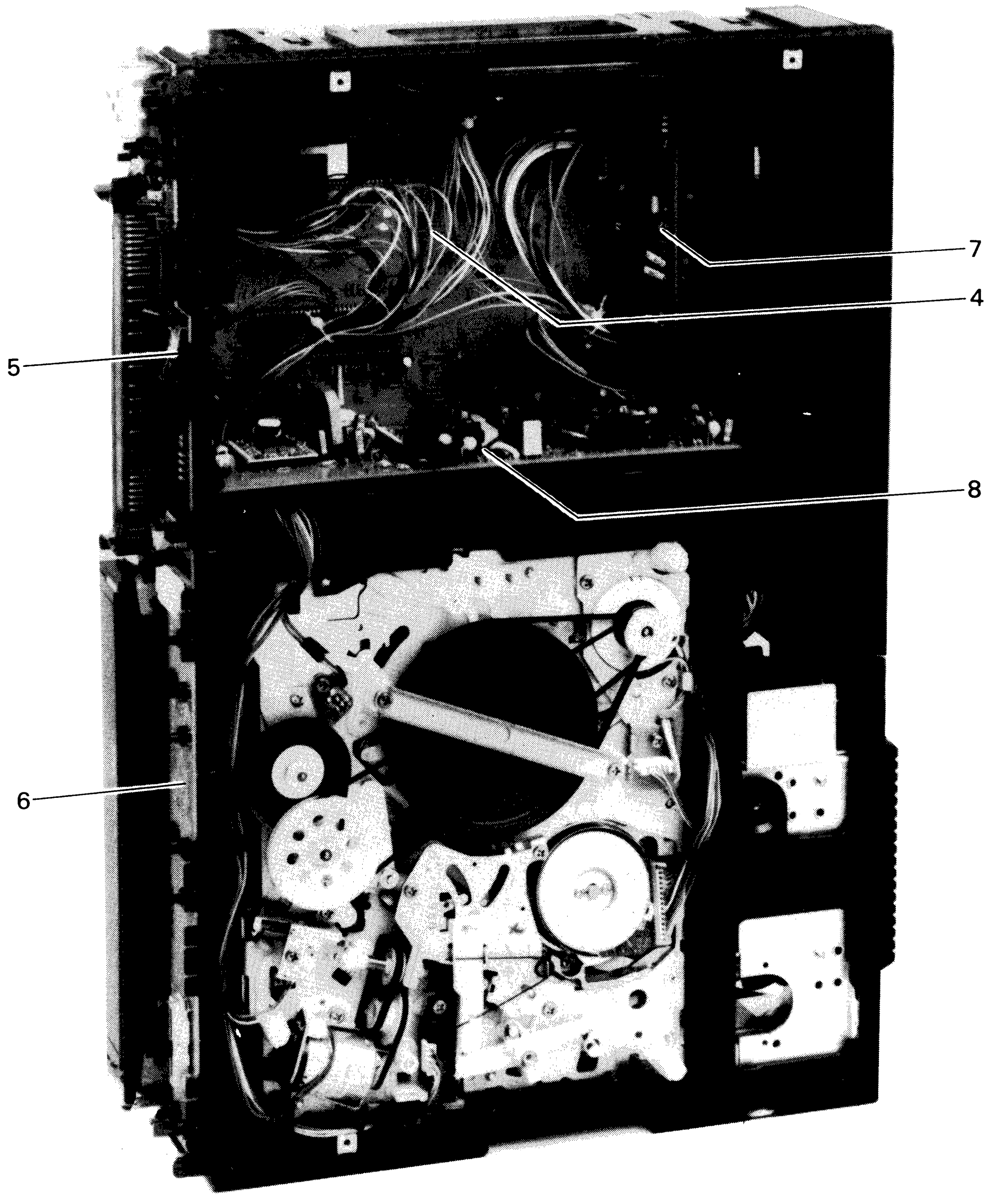


Fig. 3 Bottom View

1. Preamp circuit board
2. Regulator circuit board
3. Cylinder motor driver circuit board
4. Main circuit board
5. Timer circuit board
6. Operation switch circuit board
7. VS tuning circuit board
8. Y/chroma circuit board
9. Buzzer circuit board — VT-120E only —

(See page 2-9 for details on removing these circuit boards.)

2. NAMES AND LOCATIONS OF MAIN MECHANICAL COMPONENTS

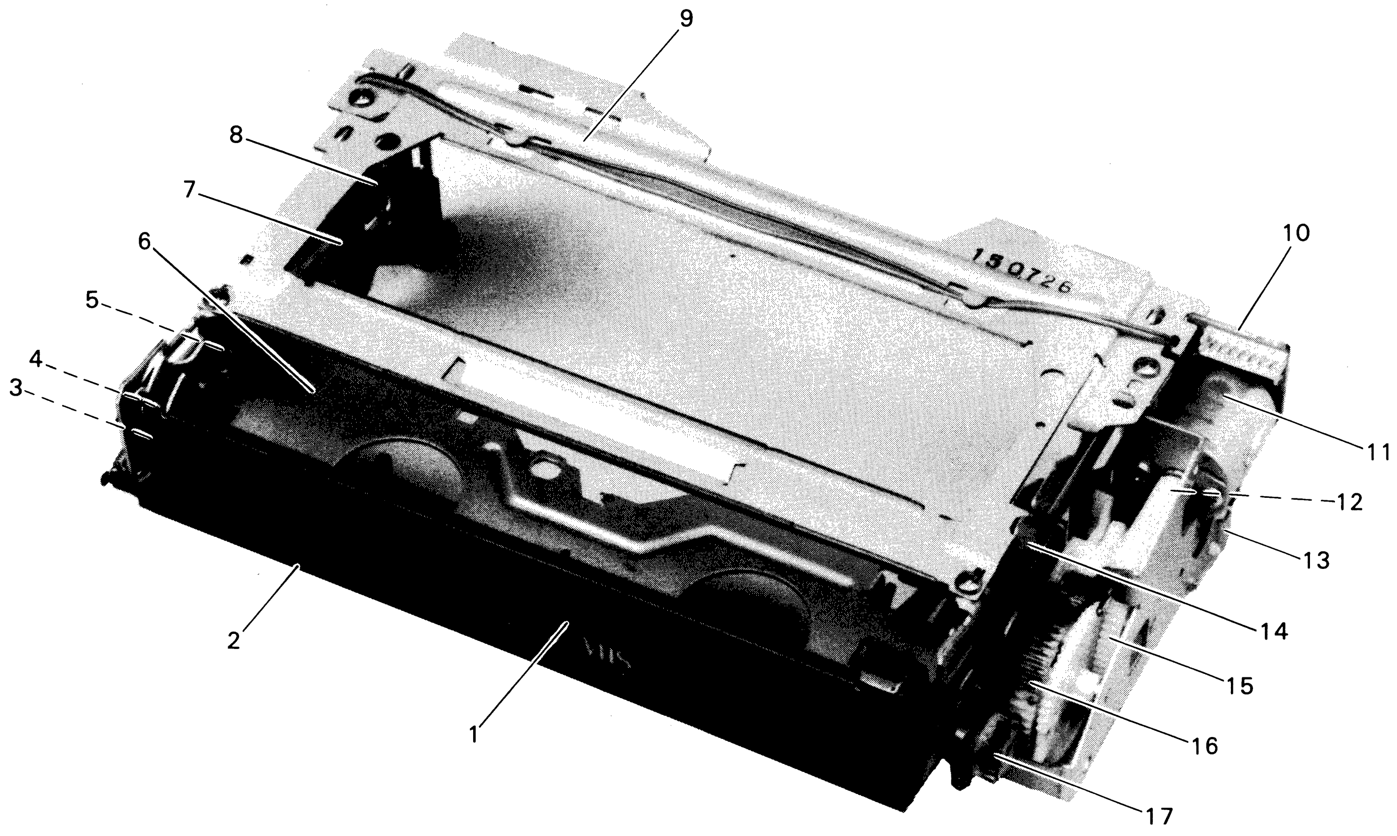


Fig. 4 Cassette Loading Mechanism

1. Cassette door
2. Front holder
3. Synchro gear (L)
4. Door arm
5. Drive gear (L)
6. Cassette holder
7. Side chassis (L)
8. Supply end sensor
9. Chassis holder
10. Cassette loading motor circuit board
11. Cassette loading motor
12. Cassette-in switch
13. Cassette-up switch
14. Side chassis (R)
15. Drive gear (R)
16. Clutch gear
17. Synchro gear (R)

(See page 2-11 for details on removing the above components.)

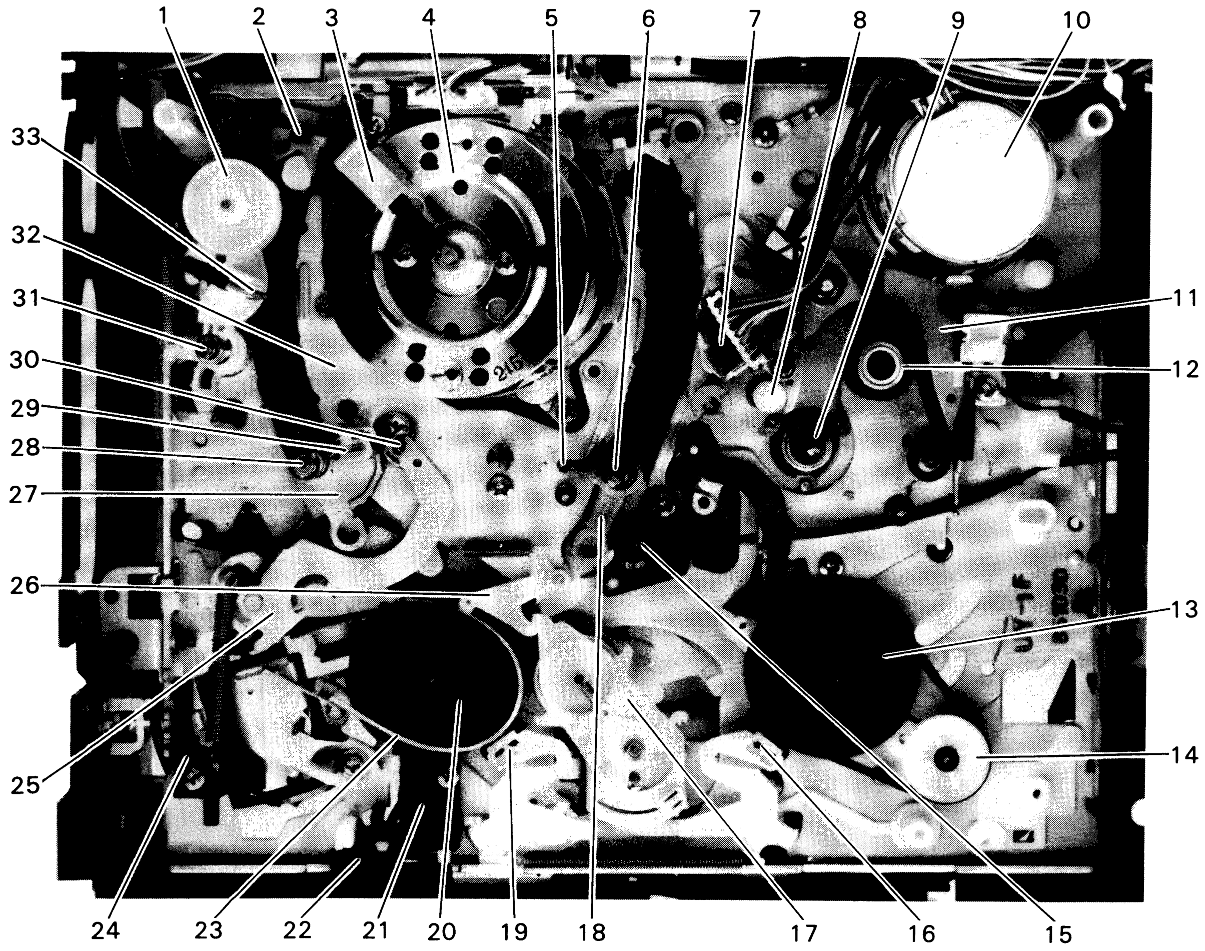


Fig. 5 Top View of Mechanism

1. Impedance roller
2. Catcher/cylinder base
3. Ground brush
4. Upper cylinder (video heads)
5. Inclined guide (take-up)
6. Take-up guide roller
7. A/C (audio/control) head
8. Take-up guide pole
9. Capstan shaft
10. Capstan motor
11. Arm bracket
12. Pressure roller
13. Take-up reel disk
14. Load pulley
15. End lamp
16. Main brake (take-up)
17. Reel drive gear
18. Take-up guide roller base
19. Main brake (supply)
20. Supply reel disk
21. Safety tab switch
22. Record prevention arm
23. Tension band
24. Spring hanger
25. Tension arm
26. Supply sub brake
27. Supply guide roller base
28. Supply guide roller
29. Inclined guide (supply)
30. Tension pole
31. Supply guide pole
32. Subchassis
33. FE (full-erase) head

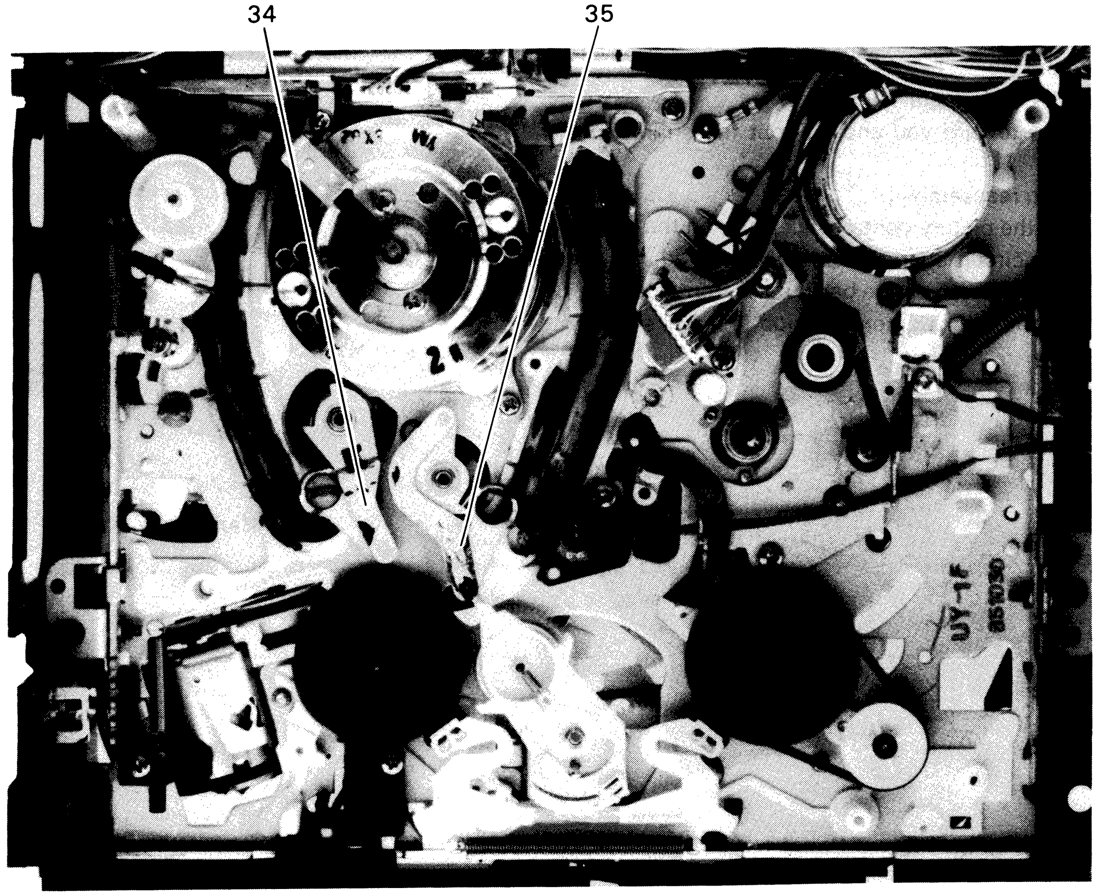


Fig. 6 Top View of Mechanism (with subchassis removed)

34. Supply loading link
35. Take-up loading link

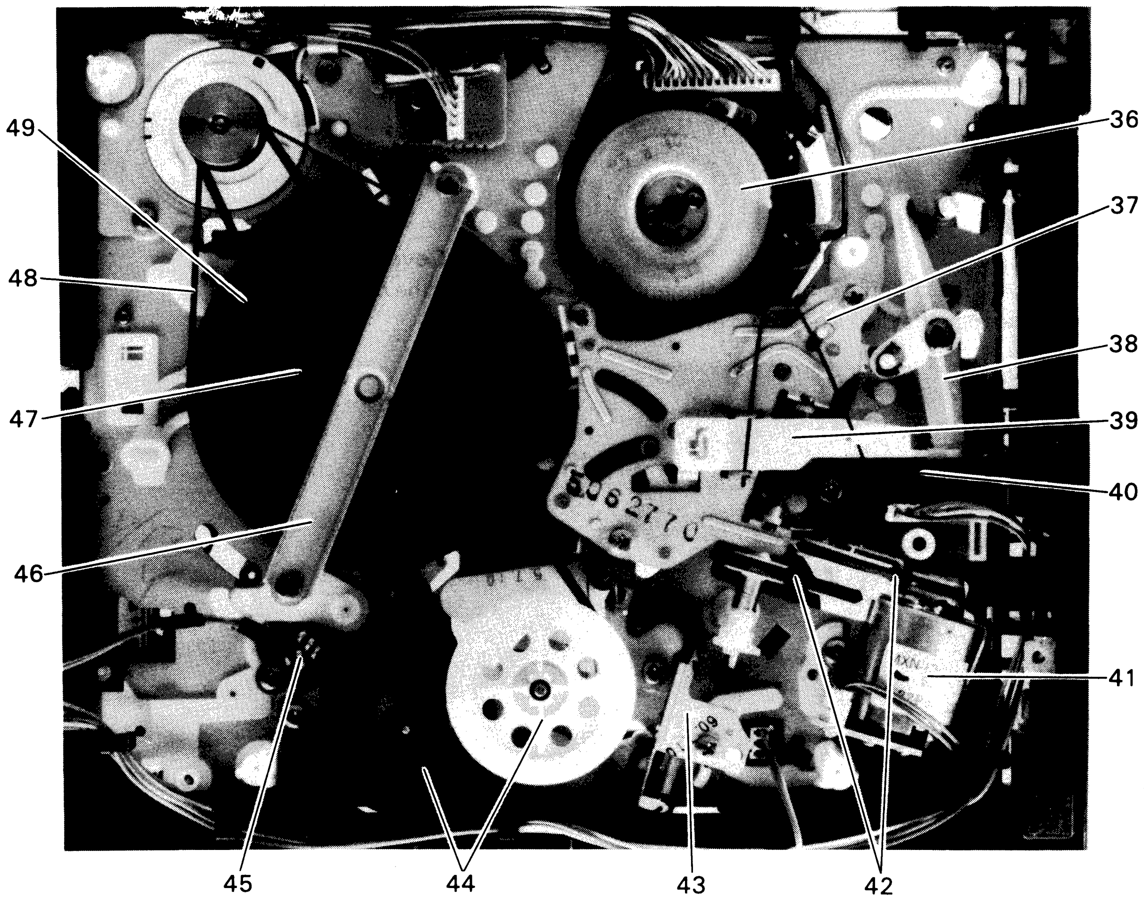


Fig. 7 Bottom View of Mechanism

36. Cylinder motor
37. Loading gear assembly
38. Tension release arm
39. Switch slider
40. Mechanism state switch
41. Loading motor
42. Loading belt
43. Brake slider
44. Clutch plate assembly
45. Reel sensor
46. Flywheel retainer bar
47. Reel belt
48. Capstan belt
49. Capstan flywheel

(See page 2-14 for details on removing the above components.)

3. CASE REMOVAL

1. **Preset door**
2. **Top cover**
3. **Bottom cover**
4. **Front panel**
5. **Shield cover**
6. **Remote controller**

1. Preset Door

1) Open the preset door. Press down on the attachment holder and pull outward in the direction of the arrow.

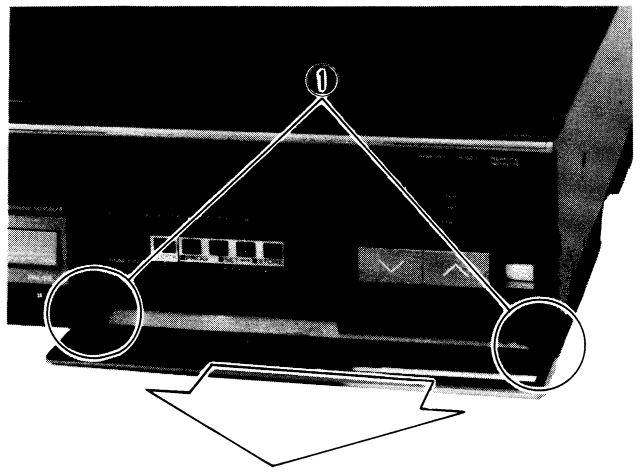


Fig. 1 Preset Door

2. Top Cover

1) Remove the 5 screws.
2) Lift the rear of the top cover upward. Slide the entire cover to the rear.

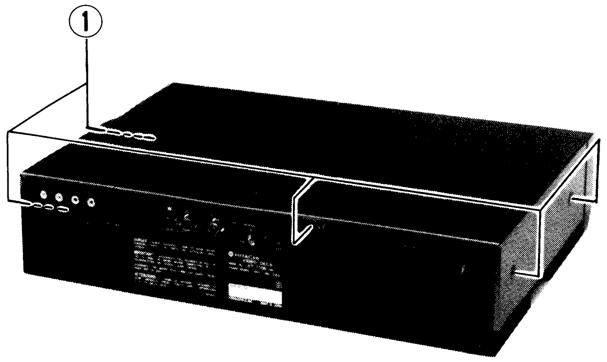


Fig. 2 Top Cover

3. Bottom Cover

1) Remove the 6 screws.

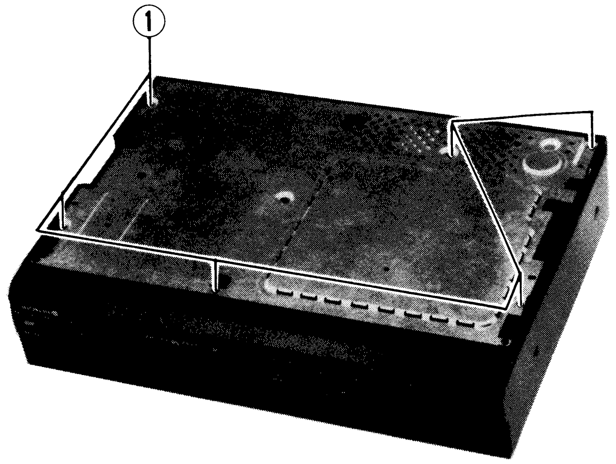


Fig. 3 Bottom Cover

4. Front Panel

1) Remove top and bottom covers (see items 2 and 3).
2) Remove the screw.
3) Release the 5 stoppers.
4) Tilt the top toward you and pull out the entire front panel.

[Cautions during reassembly]

* Make sure the picture control slide lever on the operation switch circuit board is correctly inserted into the picture control knob on the back of the front panel.

* Removing the tracking control knob first will simplify reassembly.

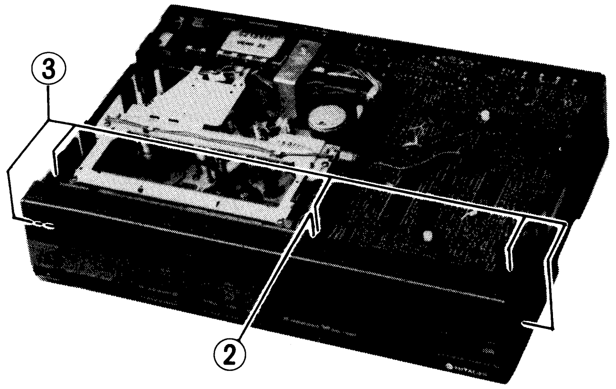


Fig. 4 Front Panel

5. Shield Cover

1) Remove the top cover (see item 2).
2) Remove the screw holding the shield cover.

[Cautions during reassembly]

* Make sure the rear of the shield cover correctly fits over the preamp circuit board's shield case.

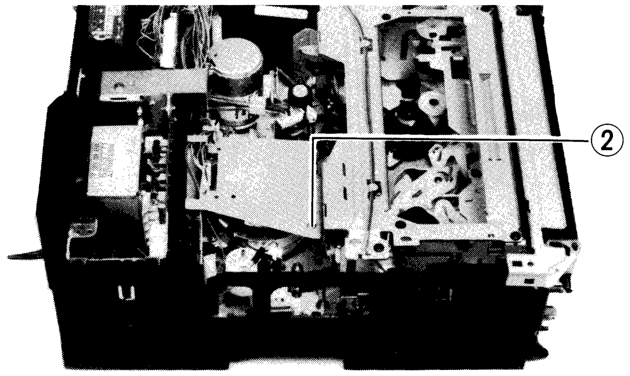


Fig. 5 Shield Cover

6. Remote Controller

1) Release 6 stoppers.

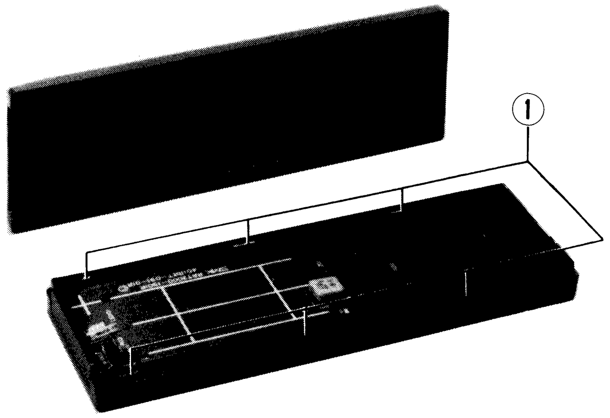


Fig. 6 Remote Controller

4. CIRCUIT BOARD REMOVAL

1. **Main Circuit Board Block** (Main, Y/chroma, VS tuning)
2. **Operation Switch Circuit Board**
3. **Timer Circuit Board**
4. **Regulator Circuit Board**
5. **Preamp Circuit Board**

1. Main Circuit Board Block

1) Remove the top and bottom covers (see items 2 and 3 in the section on case removal.)
2) Release the 2 stoppers.
3) Remove the 2 screws.
4) Push the circuit board holder in the direction of the arrow. Then lift up the entire circuit board.
5) The circuit board can now be opened in the direction of the arrow.

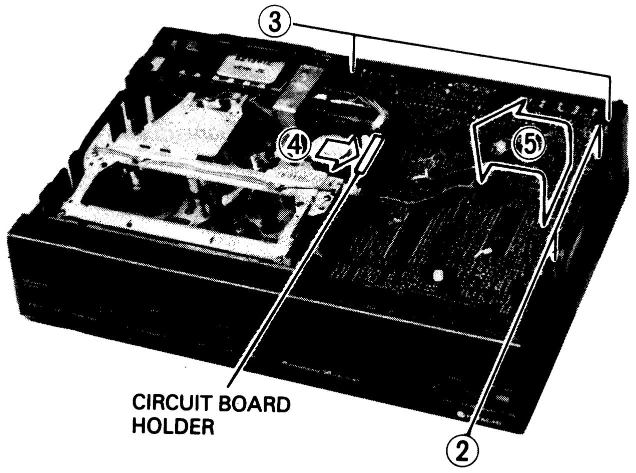


Fig. 1 Main Circuit Board Block

2. Operation Switch Circuit Board (Figs. 2 and 4)

1) Remove the top and bottom covers and the front panel (see items 2, 3 and 4 in the section on case removal.)
2) Disconnect the connector.
3) Release the 6 (5) upper and lower stoppers.

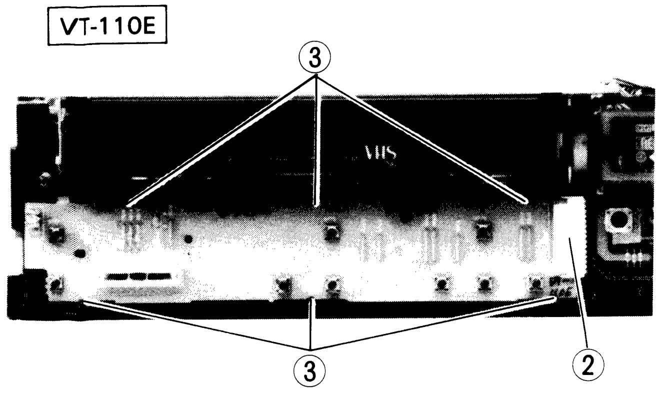


Fig. 2 Operation Switch Circuit Board

3. Timer Circuit Board (Figs. 3 and 4)

1) Remove the top and bottom covers and the front panel (see items 2, 3 and 4 in the section on case removal.)
2) Disconnect the connector.
3) Release the 5 (7) upper and lower stoppers.
4) Remove the 5 screws.

[Cautions while working]

- * Since the backup capacitor retains its charge for approx. 5 minutes after the AC power lead has been unplugged, press the reset switch to discharge the capacitor.

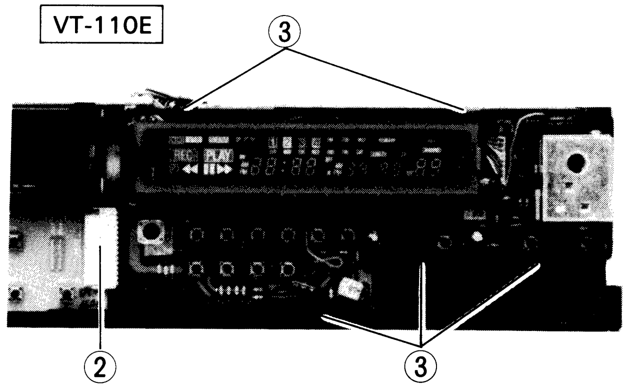


Fig. 3 Timer Circuit Board

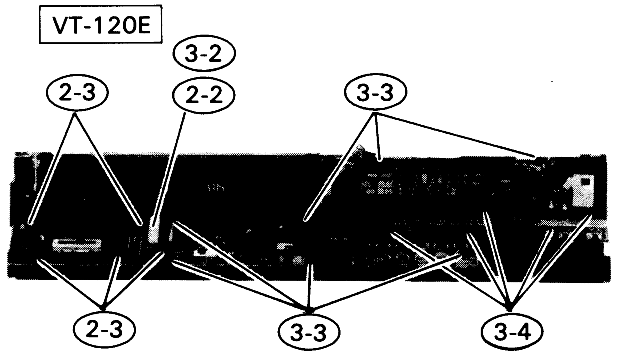


Fig. 4 Operation Switch/Timer Circuit Board

4. Regulator Circuit Board (Figs. 5 and 6)

1) Remove the top cover (see item 2 in the section on case removal).
2) Remove the 2 screws from the bottom cover.
3) Remove the screw holding the heat sink. Remove the heat sink.
4) Remove the 2 screws on the transformer holder.
5) Lift up in the direction of the arrow.

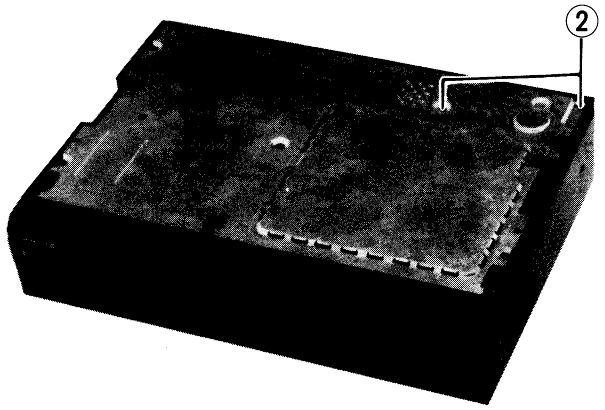


Fig. 5 Bottom Cover

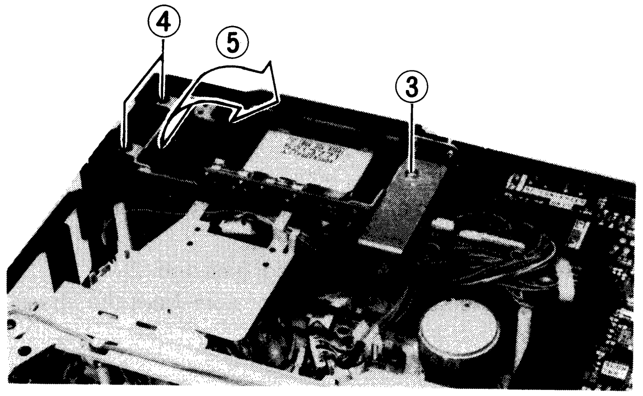


Fig. 6 Regulator Circuit Board

5. Preamp Circuit Board

1) Remove the top cover and the shield cover (see items 2 to 5 in the section on case removal).
2) Pull out and up.

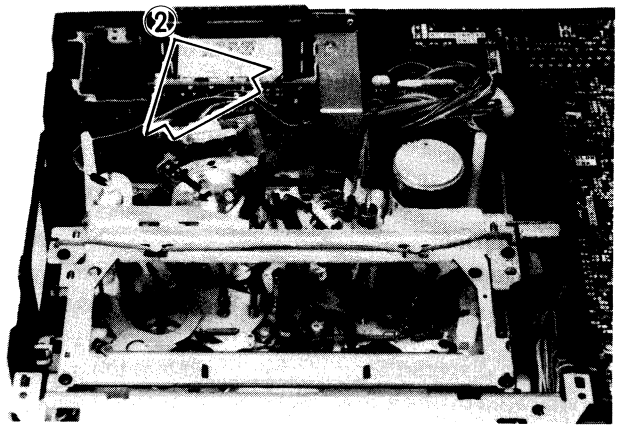


Fig. 7 Preamp Circuit Board

5. CASSETTE LOADING MECHANISM REMOVAL

1. **Cassette Door**
2. **Supply End Sensor**
3. **Chassis Holder**

* Components listed below will be described as if the top and bottom covers, front panel and shield cover have already been removed. (See items 2, 3, 4, and 5 in the section on case removal.)

4. **Cassette Loading Mechanism**
5. **Gear Cover**
6. **Door Arm**
7. **Drive Gear (L)**
8. **Motor Block**
9. **Cassette Loading Motor**
10. **Drive Gear (R)**
11. **Cassette Holder**

1. Cassette Door

1) Remove the top and bottom covers and the front panel (see items 2, 3 and 4 in the section on case removal).
2) Push and spread apart the front holder in the direction indicated by the arrow. Remove the cassette door.

[Cautions during reassembly]

* Make sure the pin on the door arm fit into the groove in the cassette door.

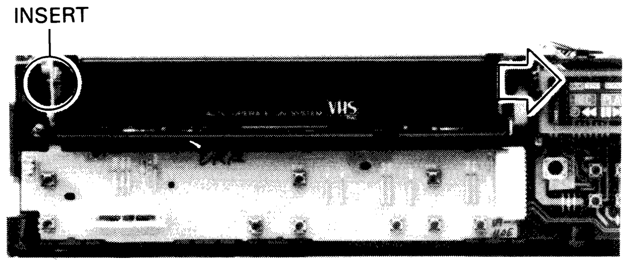


Fig. 1 Cassette Door

2. Supply End Sensor

1) Remove the top cover (see item 2 in the section on case removal).
2) Release the stopper.

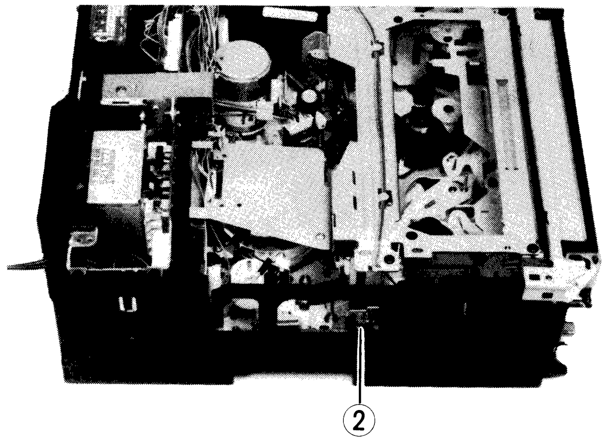


Fig. 2 Supply End Sensor

3. Chassis Holder

1) Remove the top and bottom covers (see items 2 and 3 in the section on case removal).
2) Remove the supply end sensor (see item 2).
3) Release the supply end sensor cord from the chassis holder.
4) Remove the 4 screws.

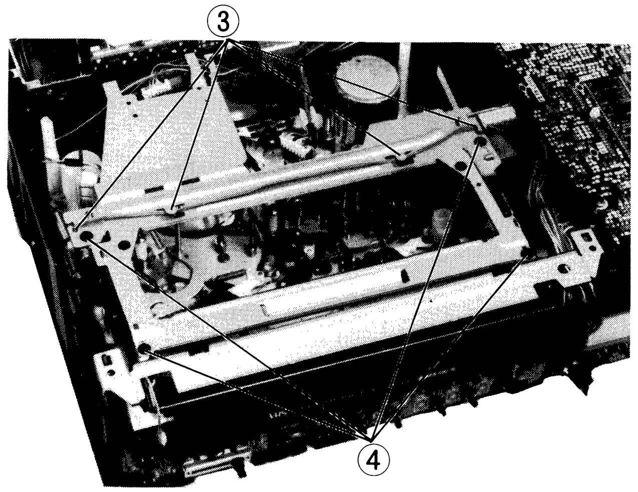


Fig. 3 Chassis Holder

4. Cassette Loading Mechanism

1) Push the reinforcing plate in the direction of the arrow, and lift upward.
2) Disconnect the connector.
3) Remove the 2 screws.
4) Lift the rear end of the mechanism upwards and release the engagement fitting on the bottom front.

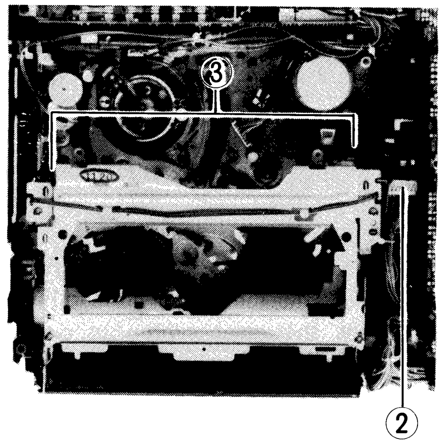


Fig. 4 Cassette Loading Mechanism

5. Gear Cover

1) Remove the cassette loading mechanism (see item 4).
2) Lift section (A) up slightly. Then pull the entire gear cover unit forward.

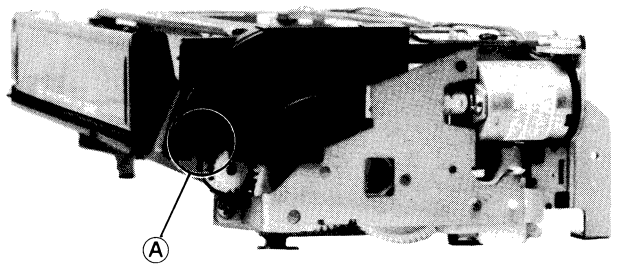


Fig. 5 Gear Cover

6. Door Arm

1) Remove the cassette loaidng mechanism (see item 4.)
2) Remove the spring.
3) Release the 2 stoppers.

[Cautions during reassembly]

* Insert the pin on the front edge of the door arm into the groove in the cassette door.

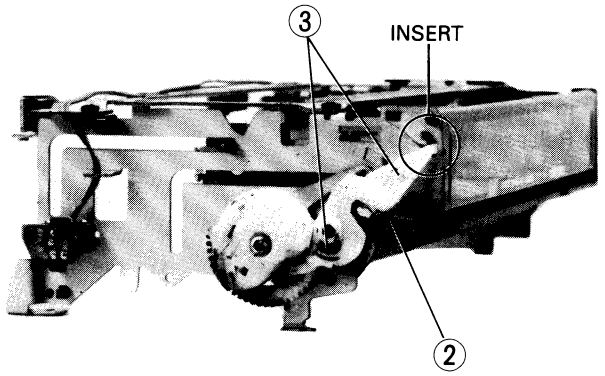


Fig. 6 Door Arm

7. Drive Gear (L)

1) Remove the cassette loading mechanism and the door arm (see items 4 and 6).
2) Release the stopper and pull out the drive gear (L).

[Cautions during reassembly]

* Align the triangular mark on the drive gear (L) with the triangular mark on the synchro gear (L).

* Insert the pin on the cassette holder into the groove in the drive arm.

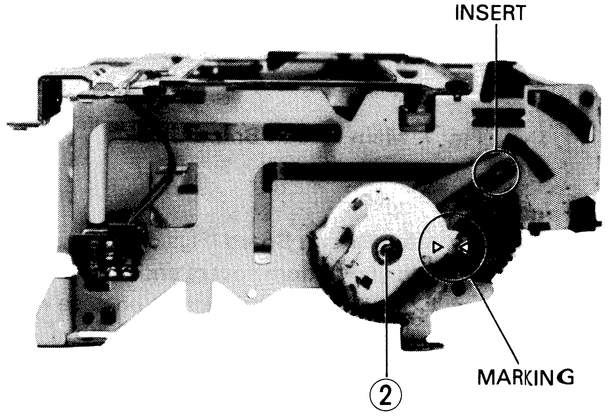


Fig. 7 Drive Gear (L)

8. Motor Block

1) Remove the cassette loading mechanism, the gear cover, the supply end sensor and the chassis holder (see items 4, 5, 2 and 3).
2) Remove the 2 screws holding the motor block.

[Cautions during reassembly]

- * Place the cassette holder in the unloaded position (prior to cassette insertion). Align the triangular markings on the synchro gear and the clutch gear.
- * Insert the slide pin on the cassette holder into the groove in the clutch gear's drive arm.

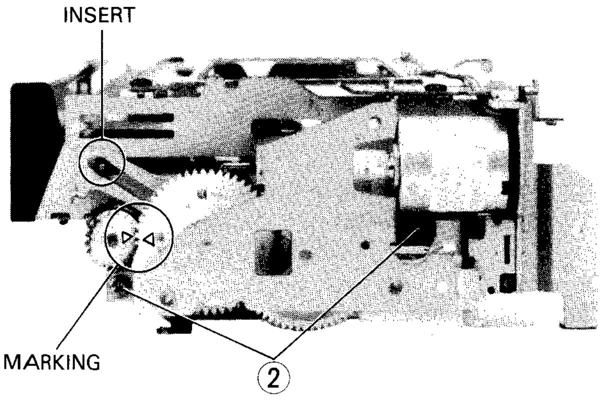


Fig. 8 Cassette Loading Motor Block

9. Cassette Loading Motor

1) Remove the cassette loading mechanism, the gear cover, the supply end sensor, the chassis holder and the motor block (see items 4, 5, 2, 3 and 8).
2) Remove the 2 screws holding the cassette loading motor.

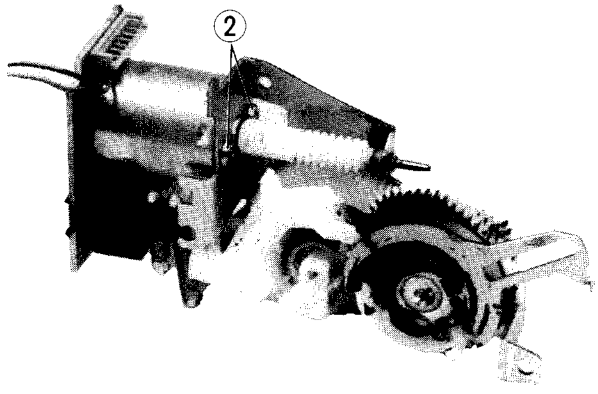


Fig. 9 Cassette Loading Motor

10. Drive Gear (R) (Figs. 10, 11 and 12)

1) Remove the cassette loading mechanism, the gear cover, the supply end sensor, the chassis holder and the motor block (see items 4, 5, 2, 3 and 8).
2) Remove the 2 springs. Pull the switch lever out.
3) Turn the drive arm counterclockwise and pull the clutch gear out.
4) Release the stopper. Pull out another gear.
5) Remove the screw holding the gear holder.

[Cautions during reassembly]

- * Position the triangular marking on the drive gear (R) so that it faces the worm gear. (See Fig. 11). The (○) and triangle can also be seen from the outside so that correct position can be checked after reassembling the motor block. (See Fig. 12)
- * Align marking (▷) on drive gear (R) with projection (⊙) on the clutch gear. (See Fig. 11)
- * Attach the spring on the clutch gear to both gears (See Fig. 11)

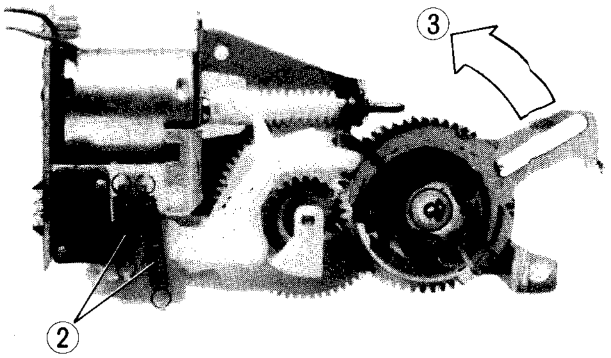


Fig. 10 Drive Gear (I)

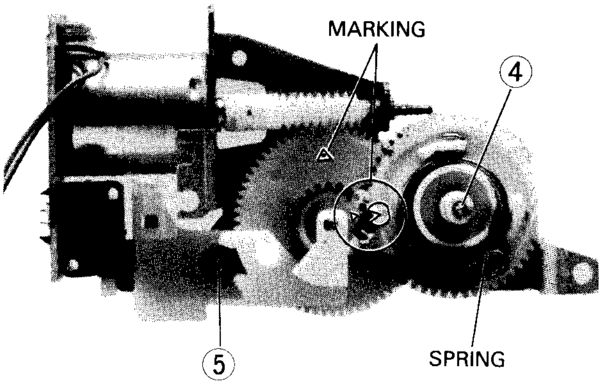


Fig. 11 Drive Gear (II)

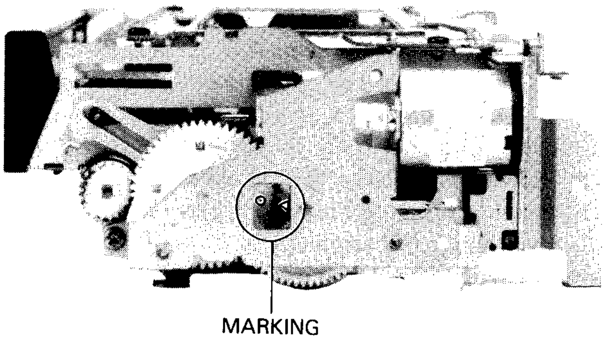


Fig. 12 Marking on Gear

11. Cassette Holder

1) Remove the cassette loading mechanism, the gear cover, the supply end sensor, the chassis holder and the motor block (see items 4, 5, 2, 3 and 8).
2) Remove the screw on top of the front holder. Remove the side chassis (R).

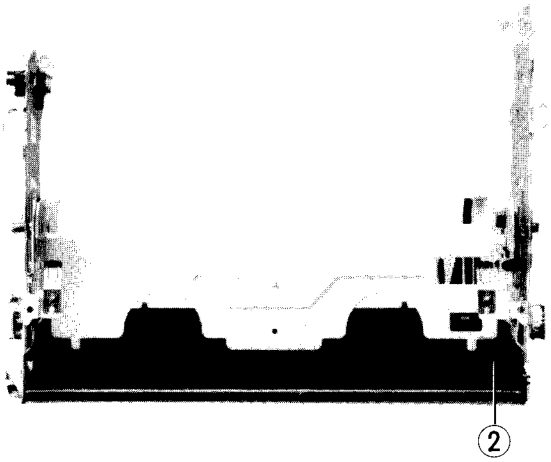


Fig. 13 Cassette Holder

6. MAIN MECHANICAL COMPONENTS REMOVAL

Heads

1. **Upper Cylinder (Video Heads)**
2. **Impedance Roller and FE (Full Erase) Head**
3. **A/C (Audio Control) Head**

Motors

4. **Cylinder Assembly**
   Rotor Magnet
   FG Coil
5. **Capstan Motor**
6. **Loading Motor**

Sensors, Switches

7. **End Lamp**
8. **Reel Sensor**
9. **Mechanism State Switch**
10. **Safety Tab Switch**

Others

11. **Main Brake**
12. **Subbrake**
13. **Supply Guide Pole**
14. **Take-up Guide Pole**
15. **Reel Drive Gear**
16. **Take-up Reel Disk**
17. **Load Pulley**
18. **Tension Arm/Tension Band**
19. **Guide Roller**
20. **Supply Reel Disk**
21. **Pressure Roller**
22. **Arm Bracket**
23. **Guide Base and Loading Link**
24. **Clutch Plate Assembly**
25. **Capstan Flywheel**
26. **Brake Slider**
27. **Loading Gear Assembly**

1. Upper Cylinder (Video Heads) (Figs. 1 and 2)

1) Remove the top cover and shield cover (see items 2 and 5 in the section on case removal)
2) Remove the screw holding the brush. Remove the earth brush.
3) Remove the 2 screws holding the upper cylinder. Pull the upper cylinder out.

[Cautions while working]

- * Since the upper cylinder has connectors, do not apply pressure in the direction of rotation. Pull the cylinder vertically upward in the direction of cylinder attachment.
- * Do not touch the video head tips with fingers or tools.

[Cautions during reassembly]

- * Insert so that the arrow on the rotary transformer matches the blue side of the video head connector.
- * Alternately tighten the 2 screws holding the upper cylinder.

[Adjustments after reassembly]

○ Adjustments after replacing the cylinder

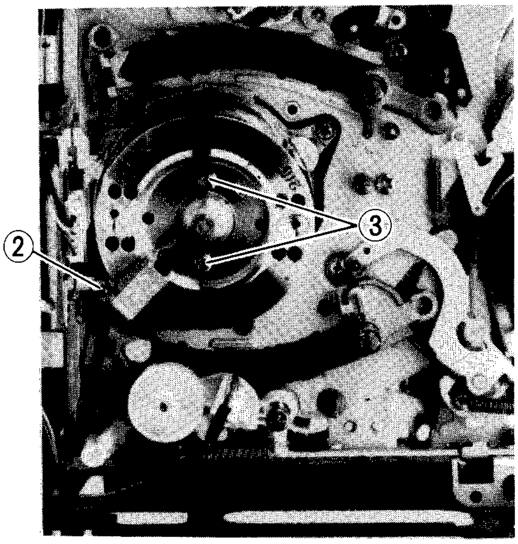


Fig. 1 **Video Head**

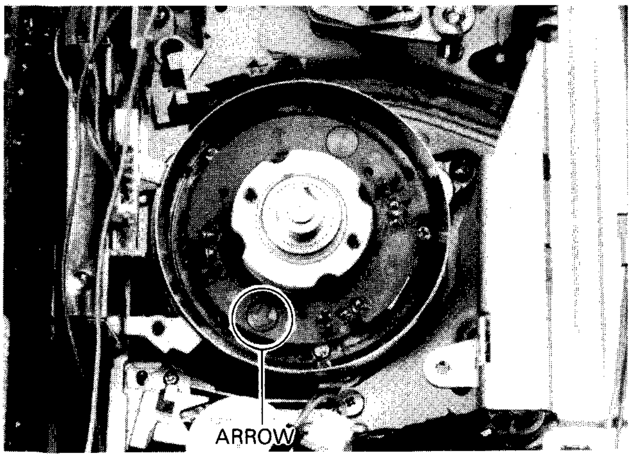


Fig. 2 **Rotary Transformer**

2. Impedance Roller and FE (Full Erase) Head

1) Remove top cover and shield cover (see items 2 and 5 in the section on case removal).
2) Disconnect the connector.
3) Remove the spring attached between the FE head base and the chassis.
4) Remove the lock nut on the guide pole and then pull the guide pole, spring and washer out.
5) Pull up the FE head together unit the base and out.
6) Then with the FE head removed, remove the screw on the back of the base.

[Adjustments after reassembly]

○ Guide pole height adjustment

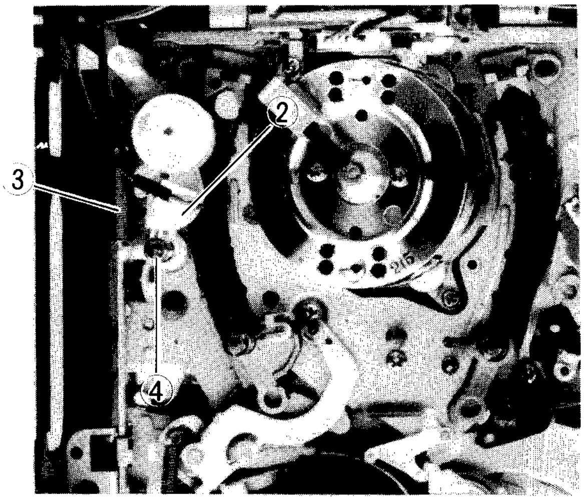


Fig. 3 **FE Head**

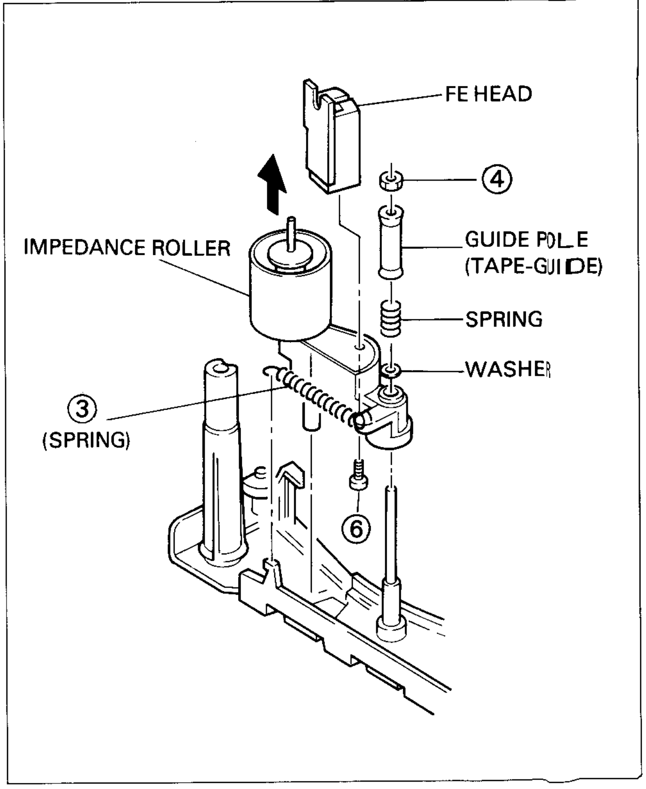


Fig. 4 **FE Head**

3. **A/C (Audio/Control) Head** (Figs. 5 and 6)

1) Remove the top cover (see item 2 in the section on case removal).
2) Release the lead from the wire guide. Pull out the connector.
3) Remove the lock nut and washer from the head base. Pull up the base and out.

* Apply the bottom of the spring under the head base to the stopper on the chassis, the top of the spring to the stopper on the base. (Fig. 6)

[Cautions during reassembly]

* Make sure the tip of the A/C head lock screw protrudes 3 to 4 mm from the top surface of head base 1.

* Make sure that head base 1 and head base 2 are parallel.

[Adjustments after reassembly]

○ A/C head adjustment
○ X value adjustment
○ Audio playback level adjustment
○ Audio bias level adjustment

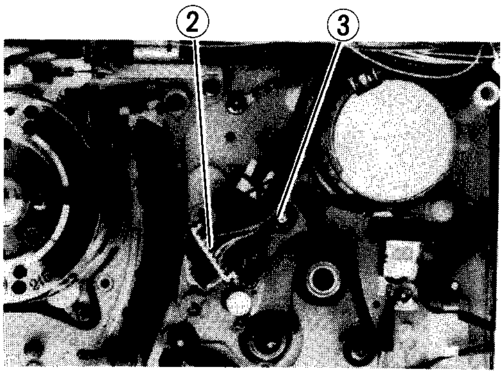


Fig. 5 AC Head

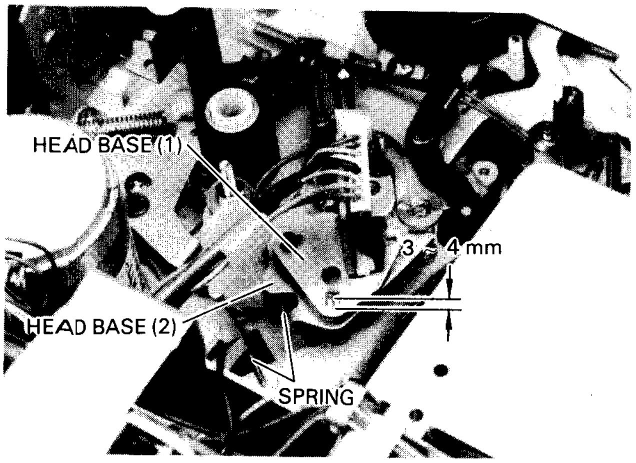


Fig. 6 Spring and Lock Screw

4. **Cylinder Assembly**

1) Remove the top cover and shield cover (see items 2 and 5 in the section on case removal).
2) Pull out the preamp circuit board.
3) Remove the bottom cover (see item 3 in the section on case removal.)
4) Disconnect the connector from the FG circuit board.
5) Remove the 3 screws holding the cylinder.
6) Remove the cylinder assembly from the top.

[Cautions during reassembly]

* Since the screws position on the back of the assembly, place the unit with the left side down to remove the screws.

* Do not touch the video head tips with fingers or tools.

[Adjustments after reassembly]

○ Adjustments after replacing the cylinder

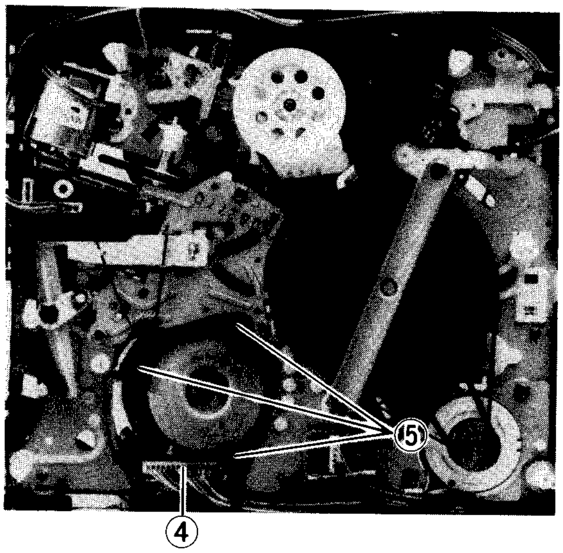


Fig. 7 Cylinder Assembly

[Removing only the rotor magnet and FG coil]

(Figs. 8 and 9)

a) Remove the bottom cover (see item 3 in the section on case removal).

b) Remove the 2 screws on the rotor. Pull the rotor magnet out.

c) Remove the 3 screws holding the FG coil.

[Cautions during reassembly]

- * Fit the slot on the cylinder rotating spindle into the protrusion on the rotor side, then lock the rotor magnet with the screws.

[Adjustments after reassembly]

○ Switching point adjustment

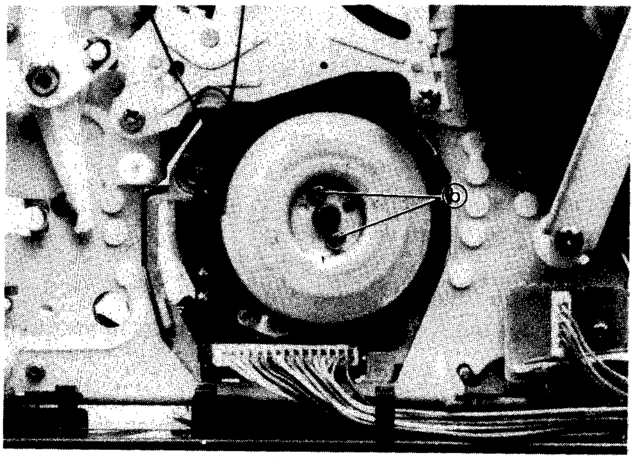


Fig. 8 Rotor Magnet

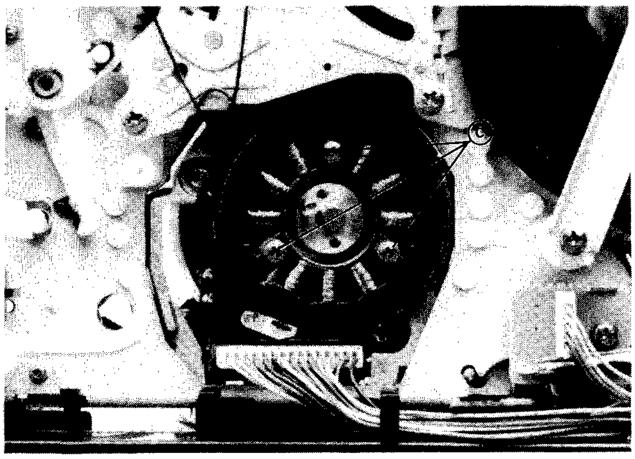


Fig. 9 FG Coil

5. Capstan Motor

1) Remove bottom cover (see item 3 in the section on case removal).
2) Remove the reel belt.
3) Remove the flywheel belt.
4) Disconnect the connector from the capstan motor circuit board.
5) Remove the 2 screws holding the capstan motor holder. Pull out the capstan motor holder.

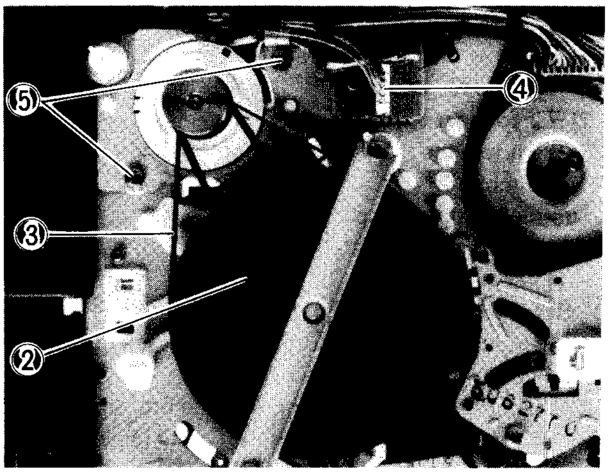


Fig. 10 Capstan Motor

6. Loading Motor

1) Remove the bottom cover (see item 3 in the section on case removal.)
2) Remove the loading belt.
3) Disconnect the connector from the loading motor circuit board.
4) Remove the screw holding the loading motor.

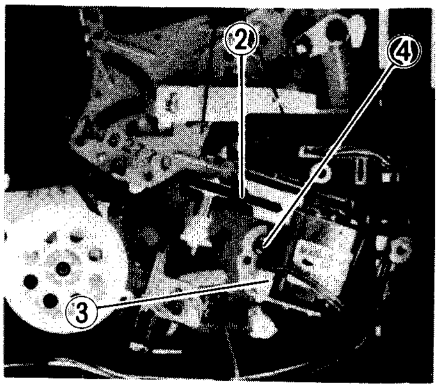


Fig. 11 Loading Motor

7. **End Lamp** (Fig. 13)
   1) Remove the top cover (see item 2 in the section on case removal).
   2) Remove the screw holding the end lamp.

8. **Reel Sensor** (Fig. 12)
   1) Remove the bottom cover (see item 3 in the section on case removal).
   2) Remove the screw holding the reel sensor.

9. **Mechanism State Switch** (Fig. 12)
   1) Remove the bottom cover (see item 3 in the section on case removal).
   2) Disconnect the connectors
   3) Remove the screw holding the mechanism state switch.

[Adjustments after reassembly]

○ Mechanism state switch adjustment

10. **Safety Tab Switch** (Figs. 12 and 13)
   1) Remove the top and bottom covers (see items 2 and 3 in the section on case removal).
   2) Disconnect the connector from the bottom side.
   3) Remove the screw holding the safety tab switch.

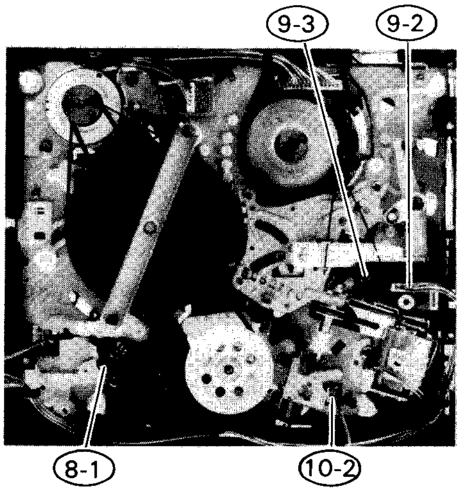


Fig. 12 Bottom View of Mechanism

* Components in items 11 to 17 are described as if the top cover has already been removed. See item 2 in the section on case removal.

11. **Main Brakes** (Fig. 13)
   1) Remove the spring between the supply and take-up brakes.
   2) Release each section engaged with the chassis.

12. **Supply Subbrake** (Fig. 13)
   1) Remove the spring between the subchassis and the brake.
   2) Release the section engaging the brake spindle.

13. **Supply Guide Pole** (Fig. 13)
   1) Remove the screw holding the guide pole.

[Cautions during reassembly]

* Make sure the washer and spring are inserted in the guide pole attachment shaft.

[Adjustments after reassembly]

○ Guide pole height adjustment

14. **Take-up Guide Pole** (Fig. 13)
   1) Remove the cap. Remove the screw holding the guide pole.

[Cautions during reassembly]

* Make sure the spring is inserted in the guide pole attachment shaft.

[Adjustments after reassembly]

○ Guide pole height adjustment

15. **Reel Drive Gear** (Fig. 13)
   1) Push the spring holder in the direction of arrow to pull the spring holder up and out.

MC-Service

16. Take-up Reel Disk (Fig. 13)

1) Remove the rubber belt across the load pulley and reel disk.
2) Remove the washer from the top of the disk.

[Cautions during reassembly]

* Make sure the washer is inserted in the reel disk attachment shaft.

[Adjustments after reassembly]

○ Reel disk height adjustment

17. Load Pulley (Fig. 13)

1) Remove the rubber belt across the pulley and the reel disk.
2) Remove the washer from the top of the pulley.

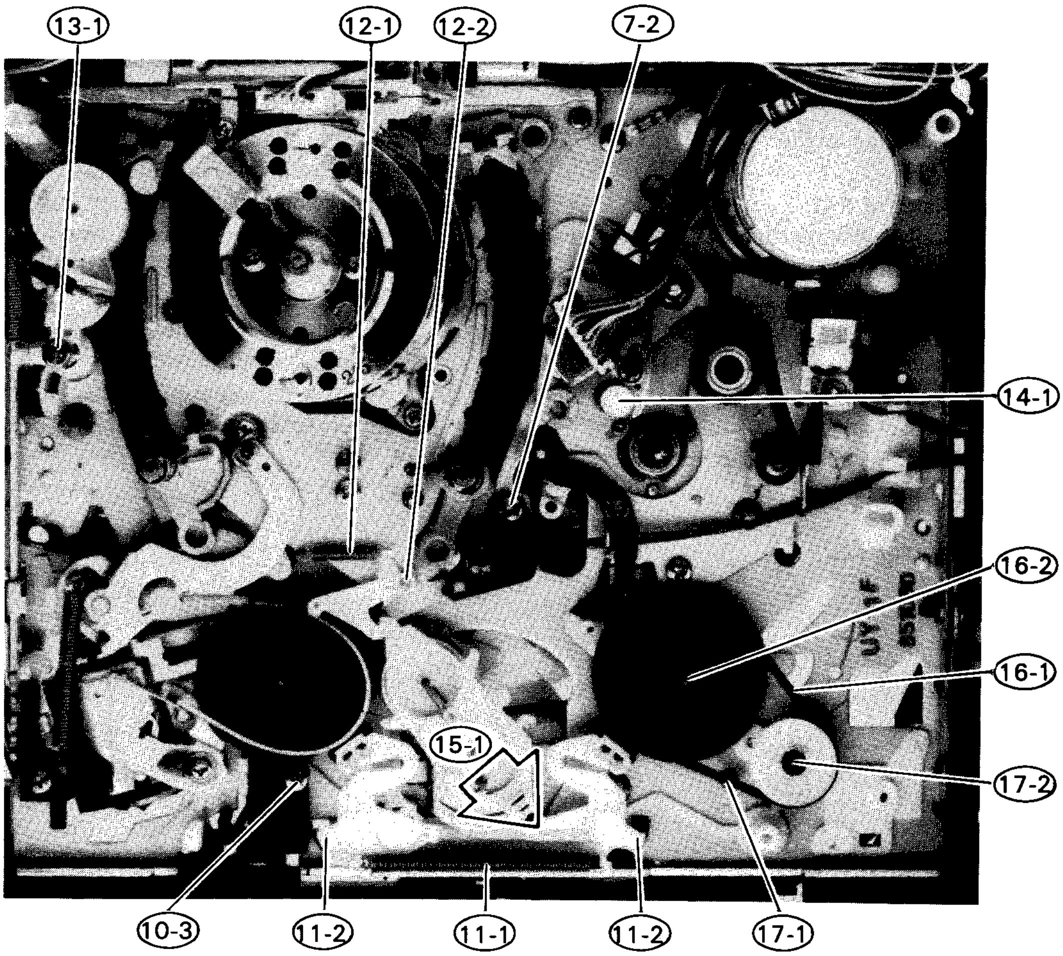

13-1
12-1
12-2
7-2
14-1
16-2
16-1
17-2
15-1
10-3
11-2
11-1
11-2
17-1

Fig. 13 Top View of Mechanism

* Components in items 18 to 23 are described as if the top and bottom covers, the front panel, the shield cover, and cassette loading mechanism have already been removed. See item 4 in the section on cassette loading mechanism removal and items 2, 3, 4 and 5 in the section on case removal.

18. Tension Arm/Tension Band (Fig. 14)

1) Remove spring (18-1) across the tension arm and spring holder.
2) Remove the screw holding the tension band.
3) Release the engagement section with the tension arm. Pull out the tension arm and tension band.

[Adjustments after ressembly]

○ Tension/tension pole position Adjustments

19. Guide Roller (Fig. 14)

* Remove the supply and take-up sides in the same way.

1) Loosen the hex lock nut on the guide roller.
2) Turn the guide roller counterclockwise to remove.

[Adjustments after reassembly]

○ Guide roller height adjustment

20. Supply Reel Disk (Fig. 14)

1) Remove the supply subbrake and tension arm/tension band (see items 12 and 18).
2) Remove the washer from the top of the disk.

[Cautions during reassembly]

* Make sure the washer and collar are inserted in the reel disk attachment shaft.

[Adjustments after reassembly]

○ Tension/tension pole position Adjustments

○ Reel disk height adjustment

21. Pressure Roller (Fig. 14)

1) Remove washer.

22. Arm Bracket Assembly (Fig. 14)

1) Remove the take-up reel disk and pressure roller (see items 16 and 21).
2) Release the 2 leads from the chassis.
3) Remove the 2 screws. Pull out the arm bracket assembly.

[Cautions during reassembly]

* Insert operation arm spindle into slot in take-up brake operation arm.
* Insert drive arm spindle into slot in link piece.

23. Guide Base/Loading Link (Fig. 14)

1) Remove supply subbrake and tension band/tension arm. (See items 12 and 18)
2) Remove the 3 screws holding the subchassis. Remove the subchassis and guide base.

[Cautions during reassembly]

* When reinstaling the loading link, make sure that the projection on the loading gear is aligned with the groove in the loading link.
* When reinstalling the guide base, make sure that the pin on the back of the guide base is inserted into the slot in the loading link.

[Adjustments after reassembly]

○ Tension/tension pole position Adjustments

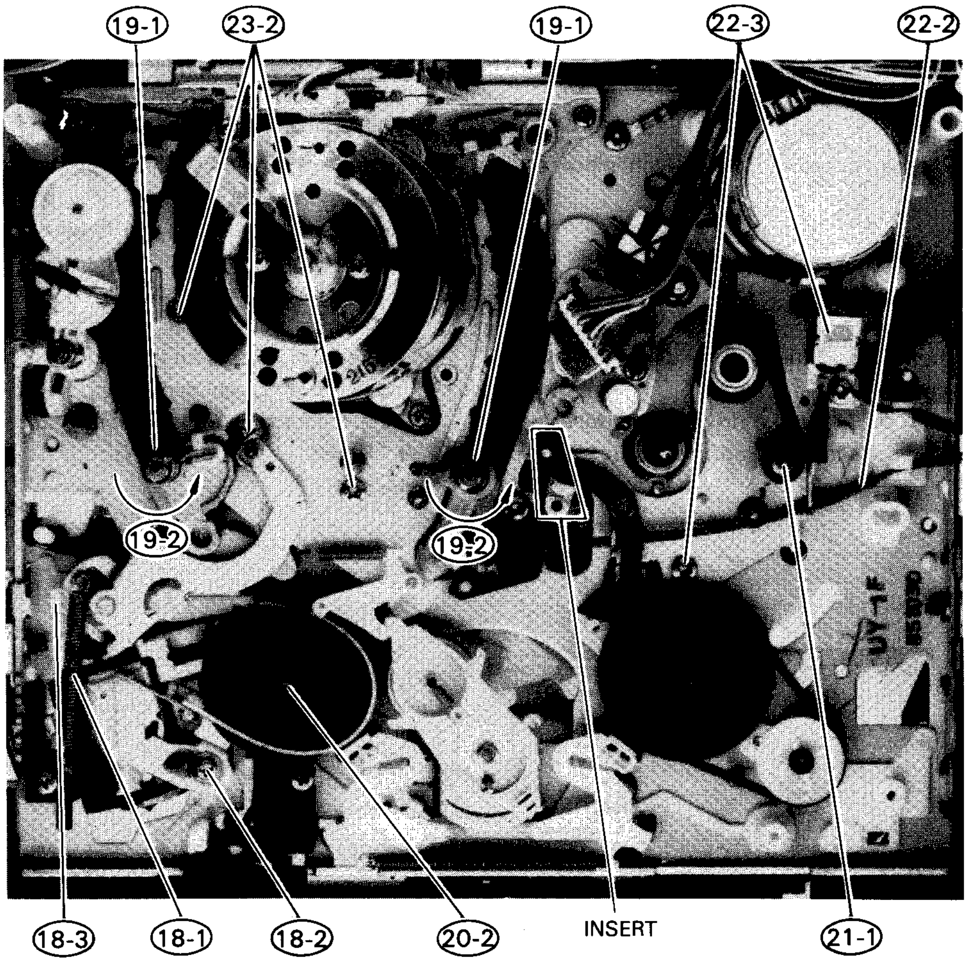

19-1
23-2
19-1
22-3
22-2
19-2
19-2
18-3
18-1
18-2
20-2
INSERT
21-1

Fig. 14 Top View of Mechanism

* Components in items 24 to 26 are described as if the top and bottom covers have already been removed. (See items 2 and 3 in the section on case removal)

24. Clutch Plate Assembly (Fig. 15)

1) Remove the reel drive gear (see item 15).
2) Remove reel belt.
3) Remove the 2 screws holding the clutch plate assembly.

25. Brake Slider (Fig. 15)

1) Remove the reel drive gear and clutch plate assembly (See items 15 and 24).
2) Remove the screw holding the brake slider.

[Cautions during reassembly]

- * Make sure the pin on the brake drive arm is inserted into the groove on the slider operating section.

26. Capstan Flywheel (Fig. 15)

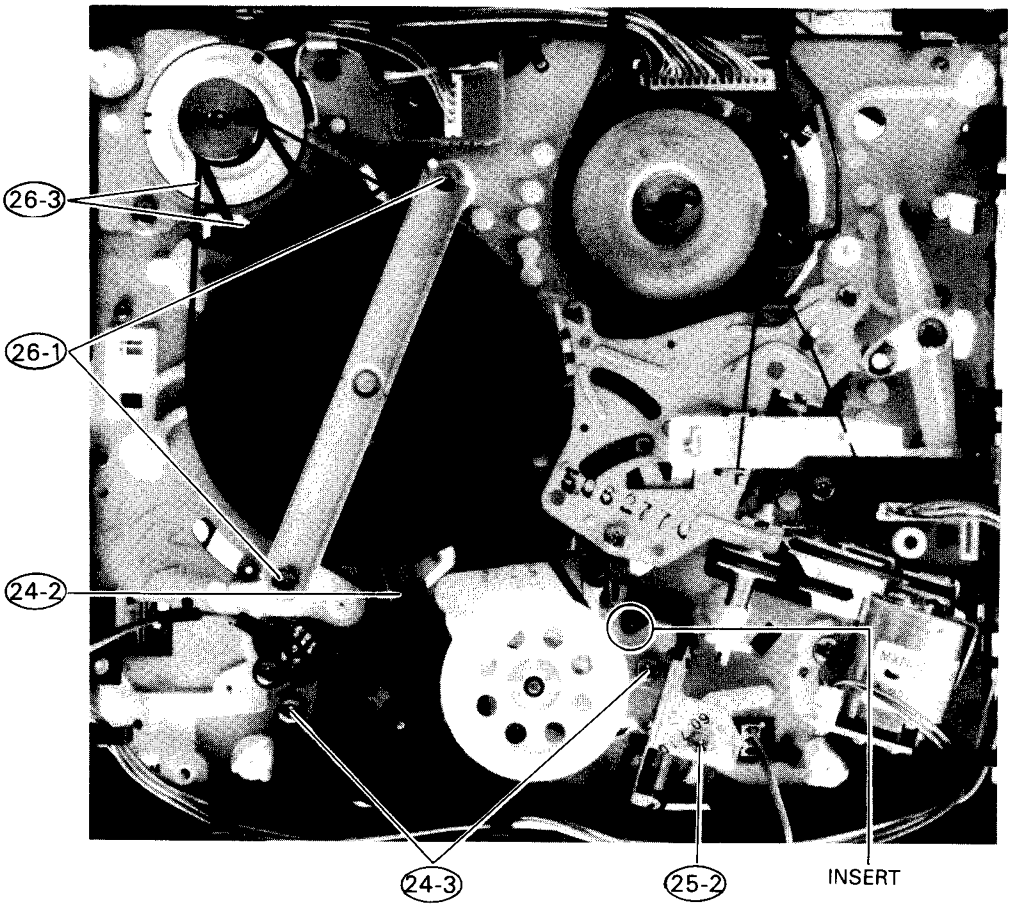
1) Remove the 2 screws holding the flywheel retainer bar. Remove the flywheel retainer bar.
2) Remove the nylon washer from the top of the capstan shaft.
3) Remove the reel belt and flywheel belt. Remove the flywheel.

[Cautions during reassembly]

- * Make sure the washer is inserted between the bottom side of the chassis and the flywheel.

[Adjustments after reassembly]

- ○ Reference oscillation frequency adjustment



MC-Service

Fig. 15 Bottom View of Mechanism

27. Loading Gear Assembly (Figs. 16 and 17)

1) Remove the top and bottom covers (see items 2 and 3 in the section on case removal).

Top Side

2) Remove the 2 screws from the top of the subchassis.
3) Remove the reel drive gear. (See item 15)

Bottom Side

4) Remove the mechanism state switch, clutch plate assembly, brake slider and capstan flywheel. (See items 9, 24, 25 and 26.)
5) Remove the spring and switch slider from the loading gear assembly.
6) Remove tension release arm.
7) Remove loading belt.
8) Remove the 3 screws holding the loading gear assembly.

[Cautions during reassembly]

- * Insert the pin on the take-up subbrake drive arm into the slot on the take-up subbrake operation arm.
- * Insert the pin on the pressure roller drive arm into the slot on the pressure roller operation arm.

[Adjustments after reassembly]

○ Mechanism state switch adjustment

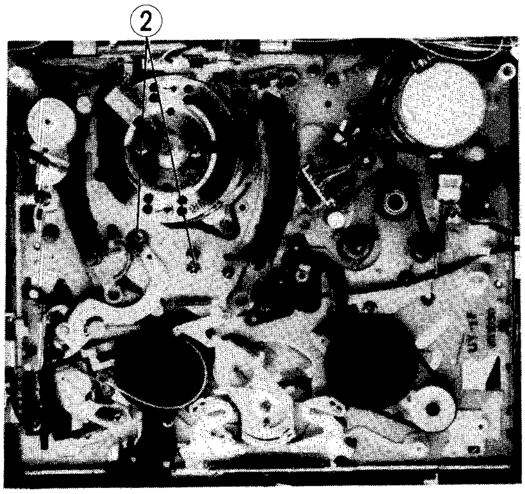


Fig. 16 Top View of Mechanism

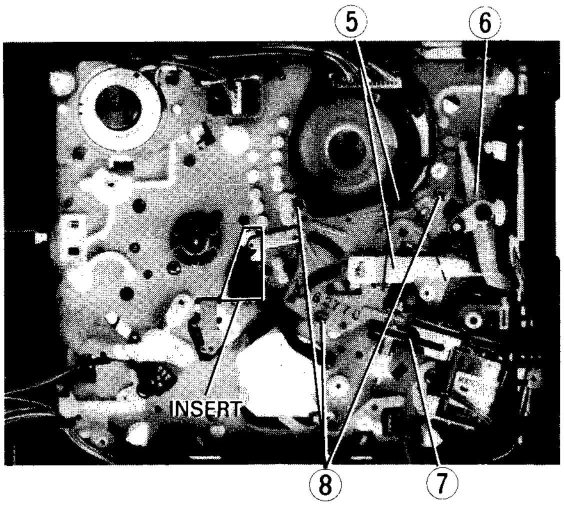


Fig. 17 Loading Gear Assembly
(with items in 9, 24, 25 and 26 removed)

MC-Service

CHAPTER 3

ELECTRIC CIRCUIT ADJUSTMENT

Test equipment and tapes necessary for adjustment.

1) Oscilloscope
2) Colour bar generator
3) VTVM
4) Frequency counter
5) Monitor TV
6) Alignment tape
7) Blank tape

Cautions on adjustments

1) If there are no special instructions, the following conditions apply:
   - ○ Oscilloscope probe: 10 : 1
   - ○ Oscilloscope synchronization: Auto-Sync
   - ○ Tracking control: center click.
2) When making more than one adjustment, make those adjustments in the order listed.

Resetting microprocessors

All microprocessors installed in the unit will be reset once the AC power lead is removed from the wall socket. However, the timer microprocessor's back-up circuit keeps it from resetting until about five minutes after power off.

The timer microprocessor can be reset by switch S759 on the timer circuit board. (Switch S759 can be operated by inserting a screwdriver into the round slot adjacent to the PRESET switch even when the front panel is attached.)

Adjust the main circuit board (servo and audio circuits) with the main circuit board open as shown in Fig. 1.

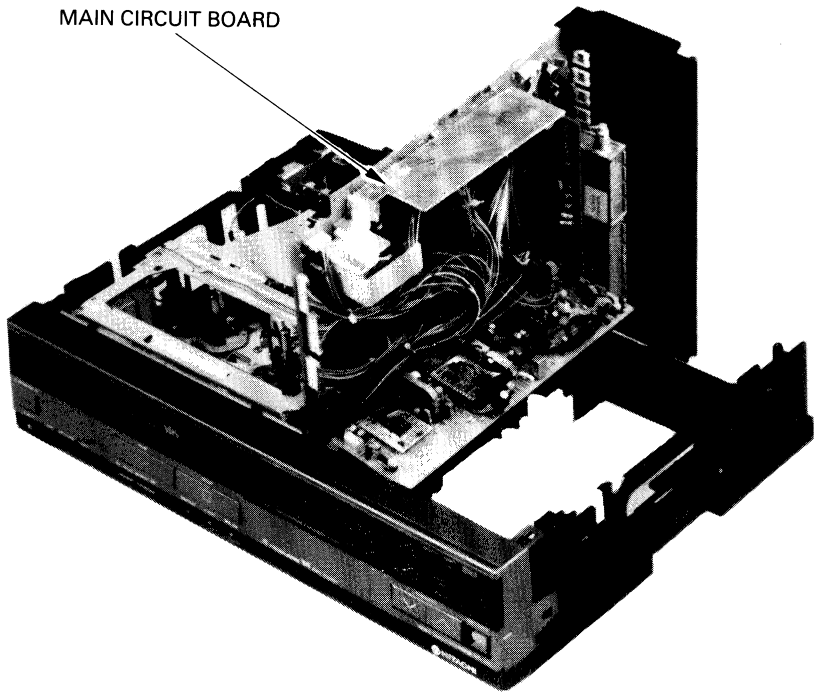


Fig. 1 Ready to Adjust Main Circuit Board

Adjust the Y/chroma circuit board with the left side down and the circuit board open as shown in Fig. 2.

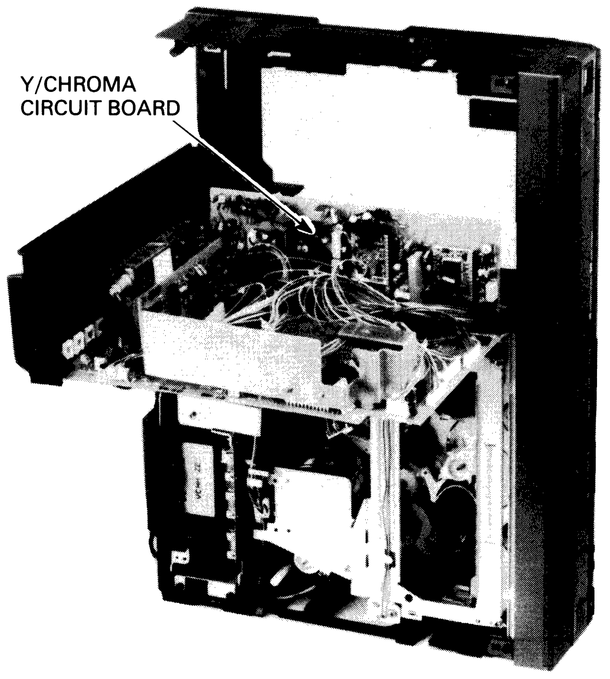


Fig. 2 Ready to Adjust Y/Chroma Circuit Board

* See item 1 in chapter 2 on circuit board removal, for details on main circuit board removal.

COMPONENTS LOCATIONS ON CIRCUIT BOARDS

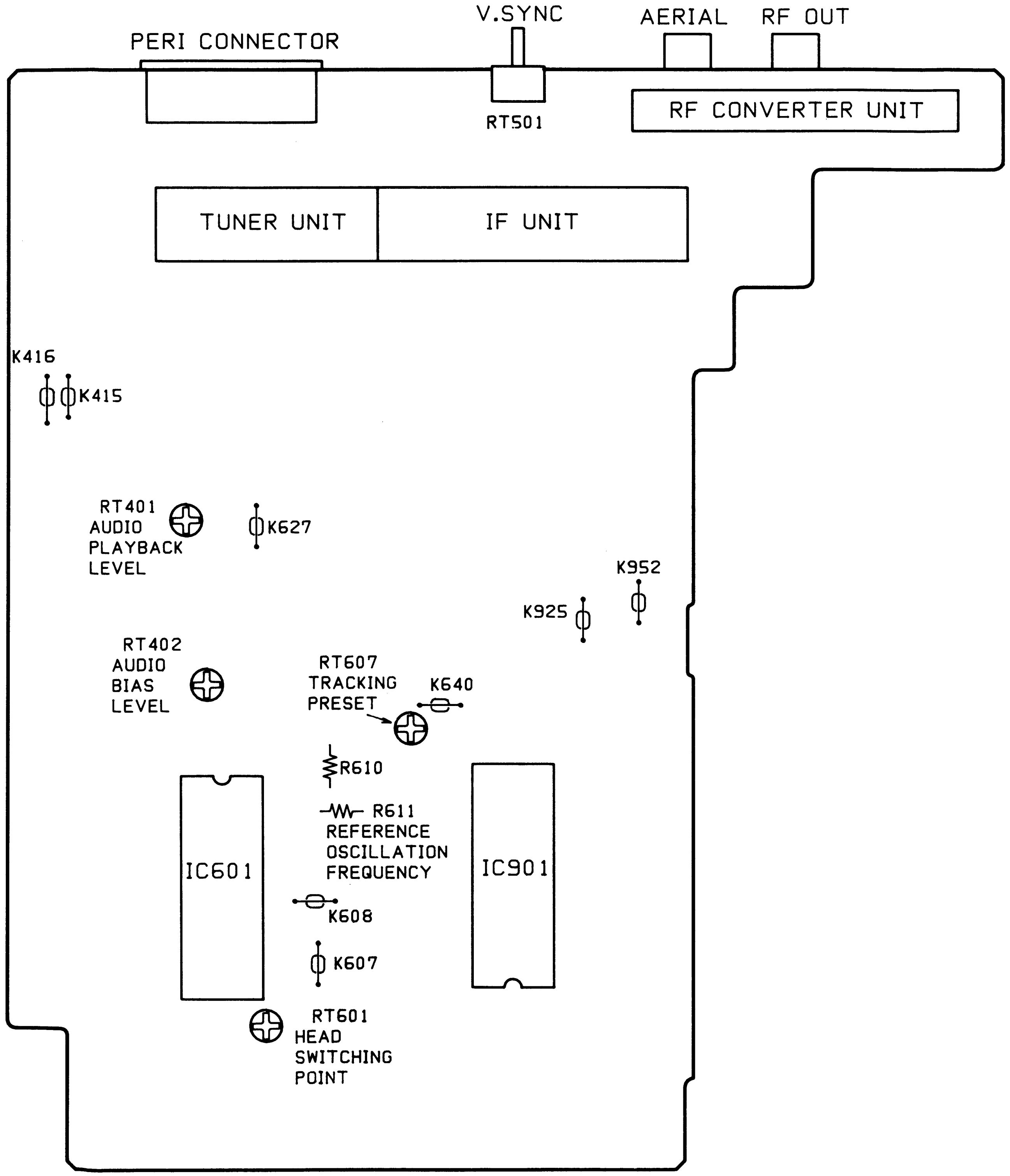

PERI CONNECTOR
V.SYNC
AERIAL
RF OUT
RT501
RF CONVERTER UNIT
TUNER UNIT
IF UNIT
K416
K415
RT401
AUDIO
PLAYBACK
LEVEL
K627
K952
K925
RT402
AUDIO
BIAS
LEVEL
RT607
TRACKING
PRESET
K640
R610
R611
REFERENCE
OSCILLATION
FREQUENCY
IC601
IC901
K608
K607
RT601
HEAD
SWITCHING
POINT

Fig. 3 Components on Main Circuit Board (Component Side)

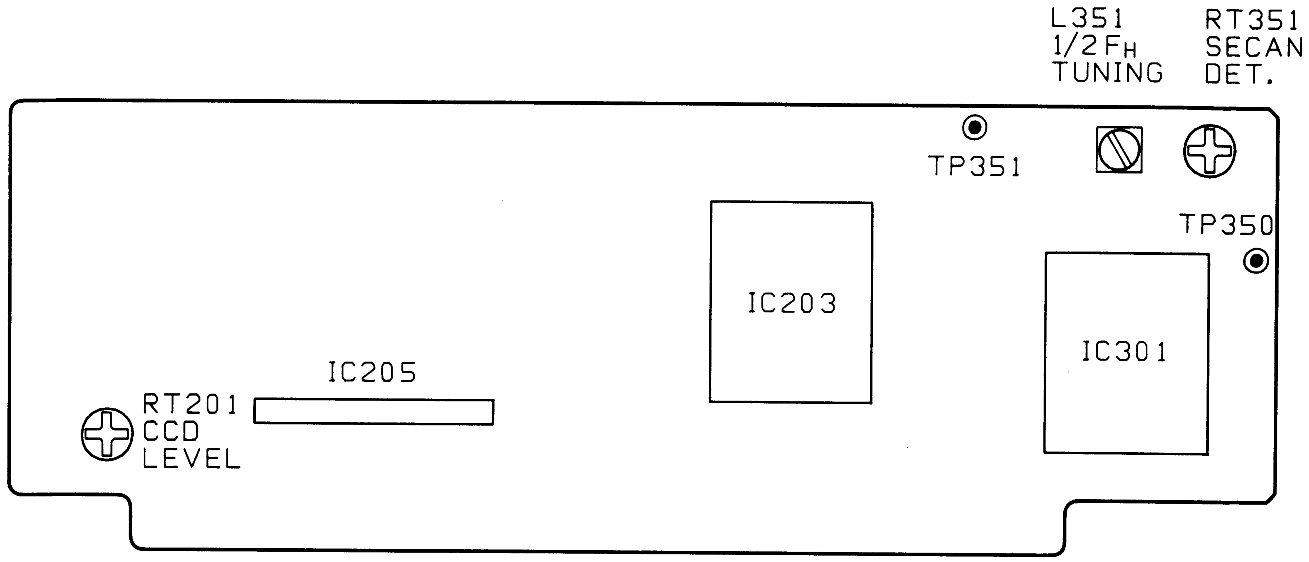

L351
1/2 FH
TUNING
RT351
SECAN
DET.
TP351
TP350
IC203
IC301
IC205
RT201
CCD
LEVEL

Fig. 4 Components on Y/Chroma Circuit Board (Component Side)

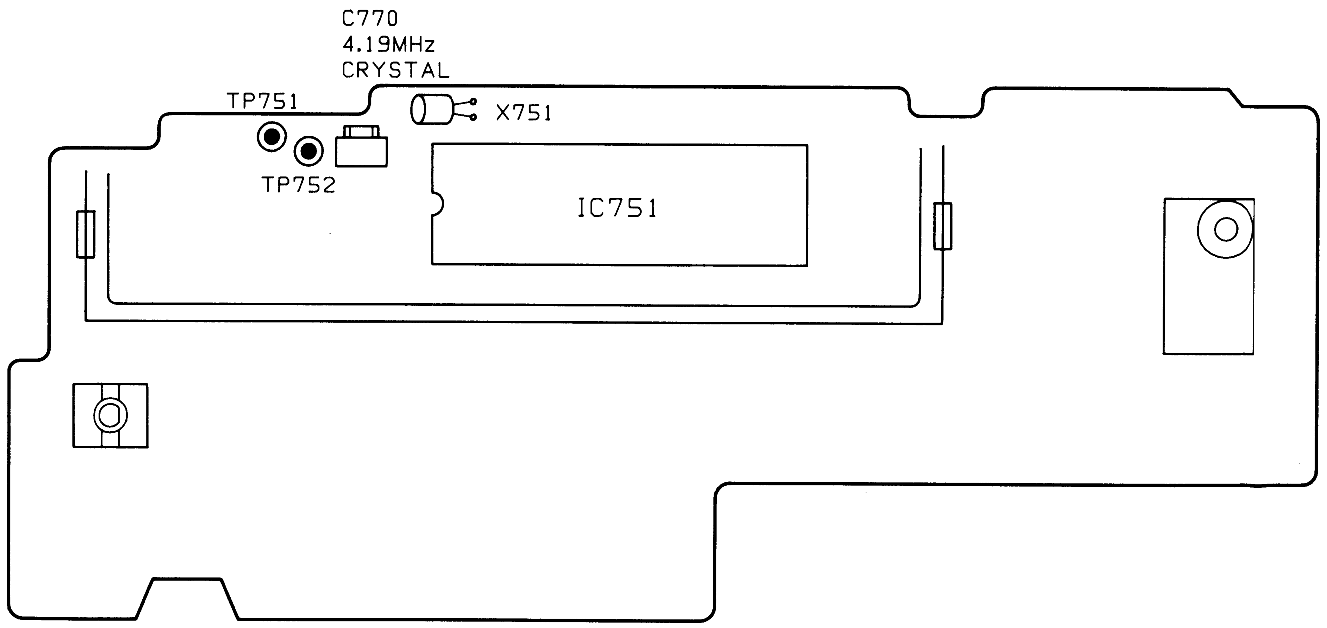

C770
4.19MHz
CRYSTAL
TP751
X751
TP752
IC751

Fig. 5 Components on Timer Circuit Board (Component Side) — VT-110E —

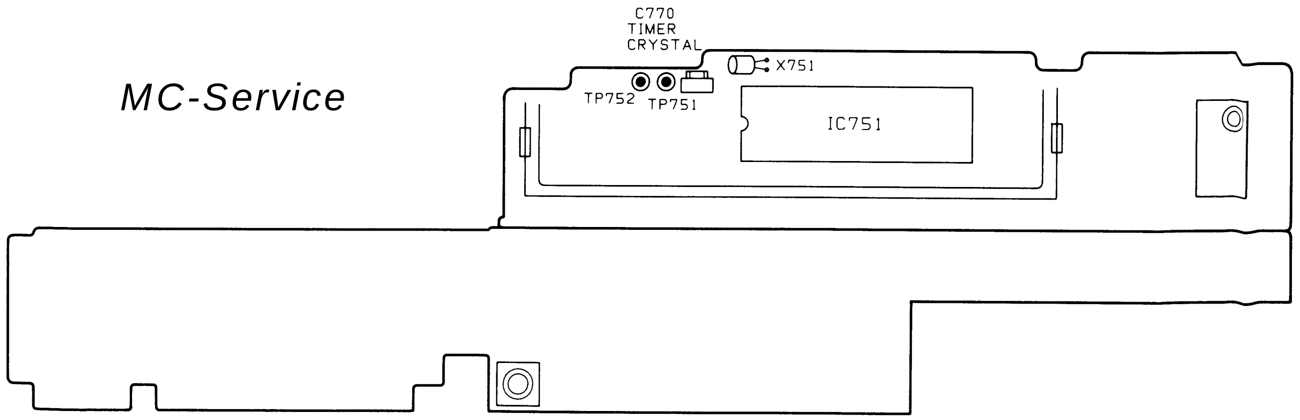

C770
TIMER
CRYSTAL
X751
TP752
TP751
IC751

Fig. 6 Components on Timer Circuit Board (Component Side) — VT-120E —

1. SERVO CIRCUIT ADJUSTMENTS

1. Reference Oscillation Frequency Adjustment

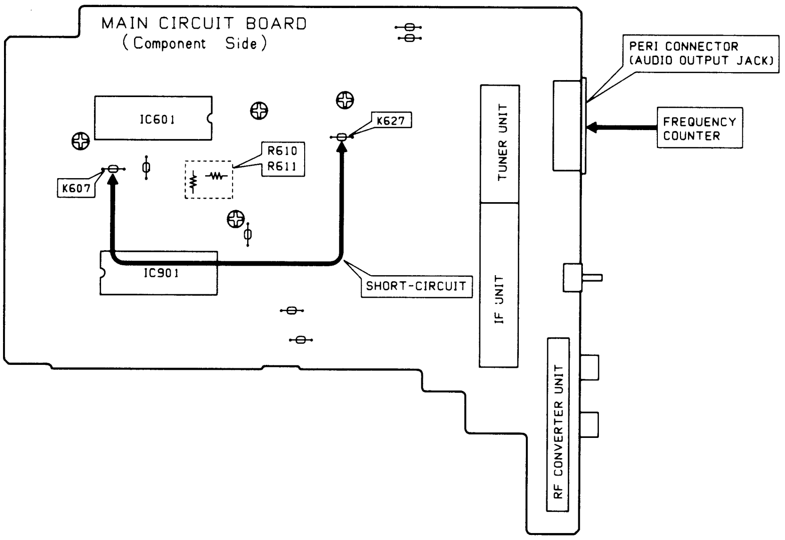
Purpose of adjustment and fault occurring if incomplete

Purpose: Fine tune the reference oscillation frequency (REF25 Hz) in the phase control loop to correct variations in diameters of flywheel, pulley, etc.

Fault: ○ Noise appears in picture.
○ Tracking cannot be optimized.

Test Equipment/Jigs	Test Equipment Connection Points	VTR State	Adjustment point
● Frequency counter ● Alignment tape	● Audio output jack	Alignment tape: Play back 3 kHz portion	● R610 (4.7K) ● R611 (3.9K)

Connection Diagram


MAIN CIRCUIT BOARD
(Component Side)
IC601
R610
R611
K607
K627
IC901
SHORT-CIRCUIT
TUNER UNIT
IF UNIT
RF CONVERTER UNIT
PERI CONNECTOR
(AUDIO OUTPUT JACK)
FREQUENCY
COUNTER

Adjustment Procedure

Readings on frequency counter

3000 Hz ± 15 Hz : Adjustment unnecessary
3015 Hz or higher : Remove R611
2085 Hz or lower : Remove R610

Note: There are some units in which R610 or R611 is removed when shipped from the factory.

2. Switching Point Adjustment

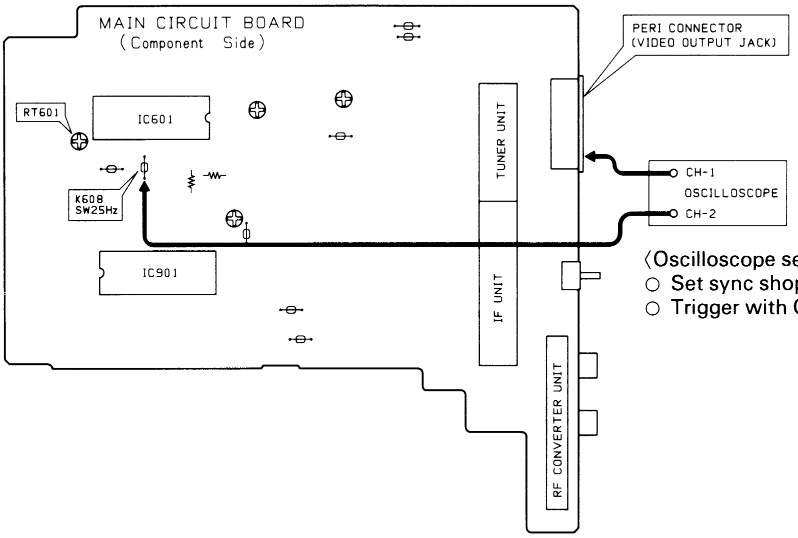
Purpose of adjustment and fault occurring if incomplete

Purpose: Set the video head switching point to almost centre where the CH-1 and CH-2 envelopes overlap each other during playback.

Fault: ○ The vertical sync signal is degraded and vertical jitter occurs.
○ Switching noise occurs in lower part of picture.

Test Equipment/Jigs	Test Equipment Connection Points	VTR State	Adjustment Point
● Oscilloscope ● Alignment tape	● CH-1: video output jack ● CH-2: K608	● Play back alignment tape	● RT601

Connection Diagram

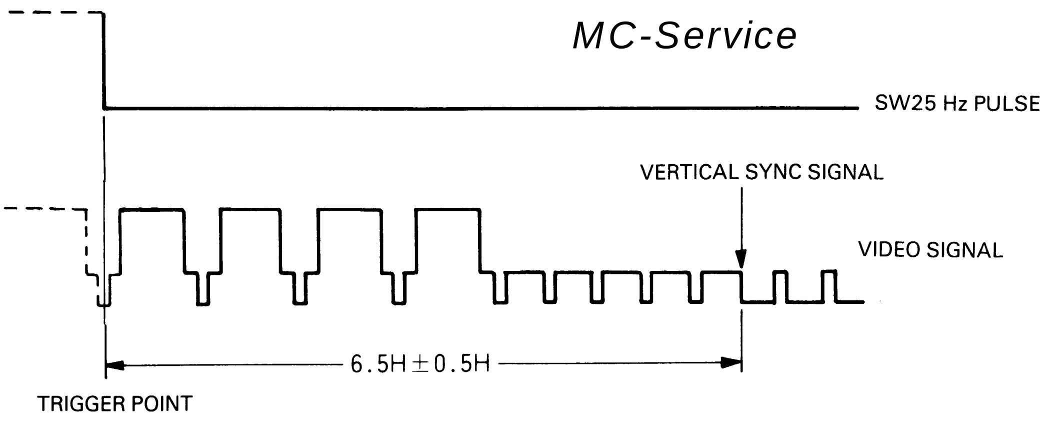

MAIN CIRCUIT BOARD
(Component Side)
PERI CONNECTOR
(VIDEO OUTPUT JACK)
RT601
IC601
K608
SW25Hz
IC901
TUNER UNIT
IF UNIT
RF CONVERTER UNIT
CH-1
OSCILLOSCOPE
CH-2

〈Oscilloscope settings〉
○ Set sync shope switch to "–"
○ Trigger with CH-2

Adjustment Procedure

Vertical sync signal:
6.5H ±0.5H from trailing edge (trigger point) of SW25 Hz pulse.

Waveform


SW25 Hz PULSE
VERTICAL SYNC SIGNAL
VIDEO SIGNAL
6.5H±0.5H
TRIGGER POINT

3. Tracking Preset Adjustment

Purpose of adjustment and fault occurring if incomplete

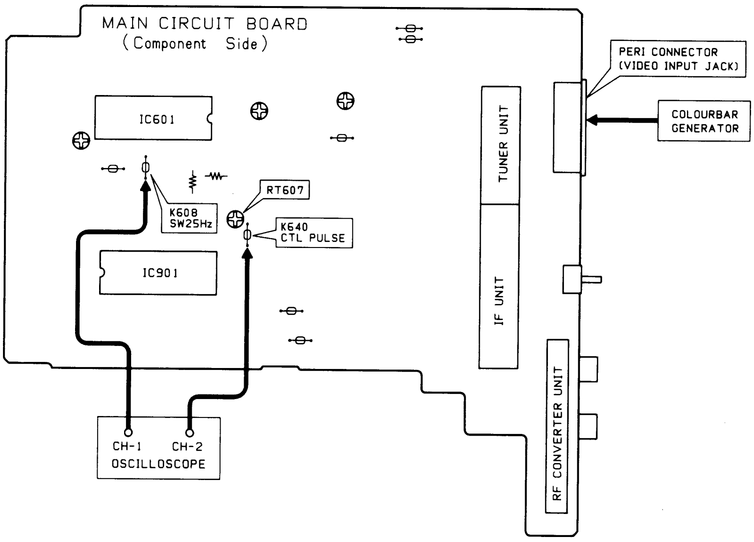
Purpose: Optimize tracking when playing back a tape recorded by this unit.

Fault: ○ Noise occurs even with tracking control centred.

○ Noise cannot be removed by turning the tracking control.

Test Equipment/Jigs	Test Equipment Connection Points	VTR State	Adjustment Point
● Oscilloscope ● Colour bar generator (or receive TV programme) ● Blank tape	● CH-1: K608 ● CH-2: K640	● Record colour bar signal and play it back with this unit.	● RT607

Connection Diagram

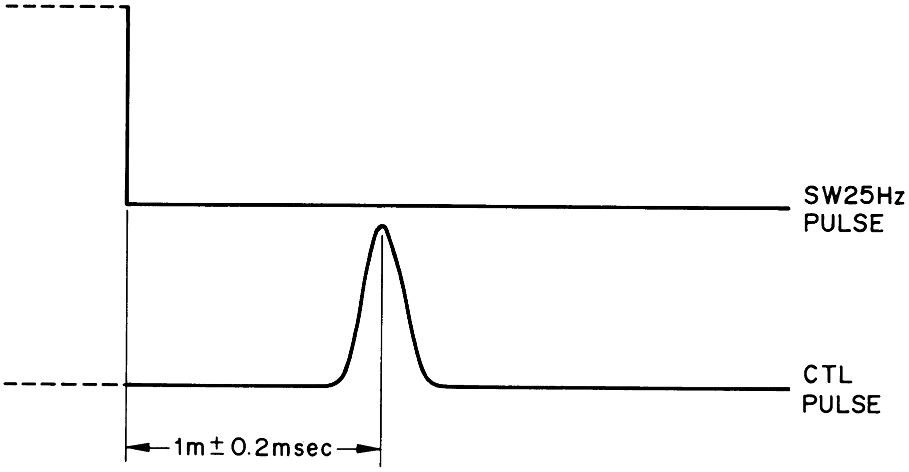

MAIN CIRCUIT BOARD
(Component Side)
PERI CONNECTOR (VIDEO INPUT JACK)
COLOURBAR GENERATOR
IC601
RT607
K608 SW25Hz
K640 CTL PULSE
IC901
TUNER UNIT
IF UNIT
RF CONVERTER UNIT
CH-1
CH-2
OSCILLOSCOPE

Adjustment Procedure

1) Tracking control: centred

2) It is 1 ± 0.2 ms from the fall of SW 25 Hz to the peak of CTL pulse.

Waveform


SW25Hz PULSE
CTL PULSE
1m ± 0.2msec

4. V Jitter Adjustment

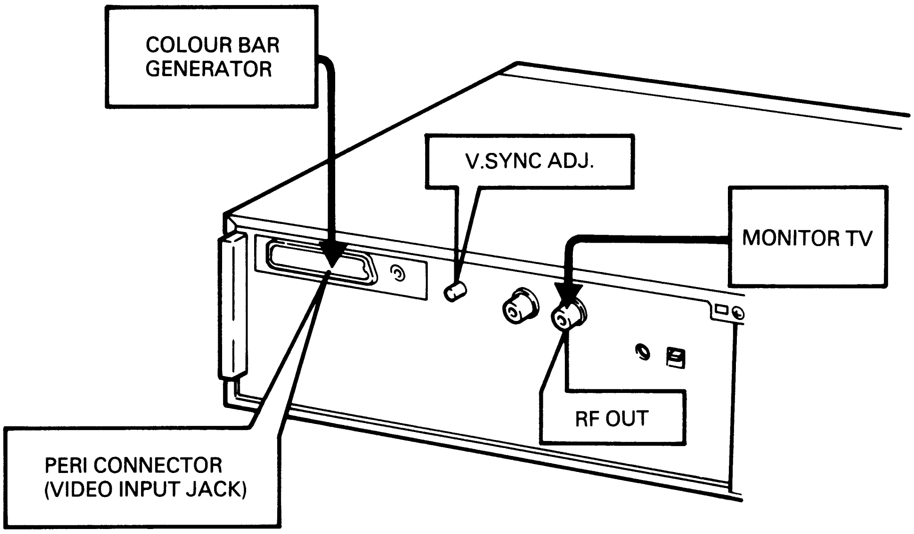
Purpose of adjustment and fault occurring if incomplete

Purpose: Change timing for adding vertical drive pulse and suppress vertical jitter in picture during trick play.

Fault: Vertical jitter during trick play.

Test Equipment/Jigs	Test Equipment Connection Points	VTR State	Adjustment Point
● Monitor TV ● Colour bar generator (or receive TV programme) ● Blank tape	● Check with monitor TV	● Record colour bar signal, play it back with this unit in F.ADV mode.	● RT501

Connection Diagram (Can be adjusted without removing any covers)


COLOUR BAR GENERATOR
V.SYNC ADJ.
MONITOR TV
RF OUT
PERI CONNECTOR (VIDEO INPUT JACK)

Adjustment Procedure

Suppress vertical jitter in picture.

MC-Service

2. AUDIO CIRCUIT ADJUSTMENTS

1. Audio Playback Level Adjustment

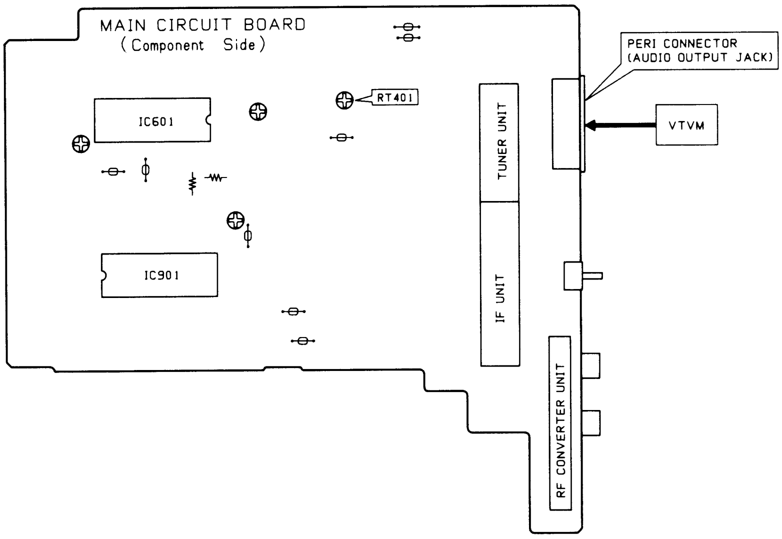
Purpose of adjustment and fault occurring if incomplete

Purpose: Set the audio playback level to the specified value.

Fault:

Test Equipment/Jigs	Test Equipment Connection Points	VTR State	Adjustment Point
● VTVM ● Alignment tape	● Audio output jack	● Play back alignment tape	● RT401

Connection Diagram


MAIN CIRCUIT BOARD
(Component Side)
RT401
IC601
IC901
TUNER UNIT
IF UNIT
RF CONVERTER UNIT
PERI CONNECTOR
(AUDIO OUTPUT JACK)
VTVM

Adjustment Procedure

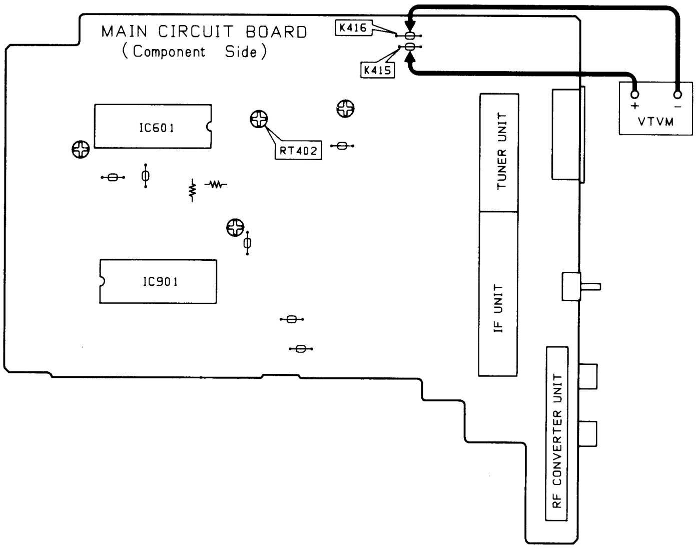
The VTVM reads −8 dBm +1 dBm

2. Audio Bias Level Adjustment

Purpose of adjustment and fault occurring if incomplete
Purpose: Set audio bias during recording to optimum level.
Fault: ○ Bias too deep: High-frequency response deteriorates.
○ Bias too shallow: Sound tends to be distorted.

Test Equipment/Jigs	Test Equipment Connection Points	VTR State	Adjustment Point
● VTVM ● Blank tape	● K415 ● K416	● Non-signal recording	● RT402

Connection Diagram


MAIN CIRCUIT BOARD
(Component Side)
K416
K415
IC601
RT402
IC901
TUNER UNIT
IF UNIT
RF CONVERTER UNIT
+
-
VTVM

Adjustment Procedure
The VTVM reads 2.3 mV ±0.1 mVrms.

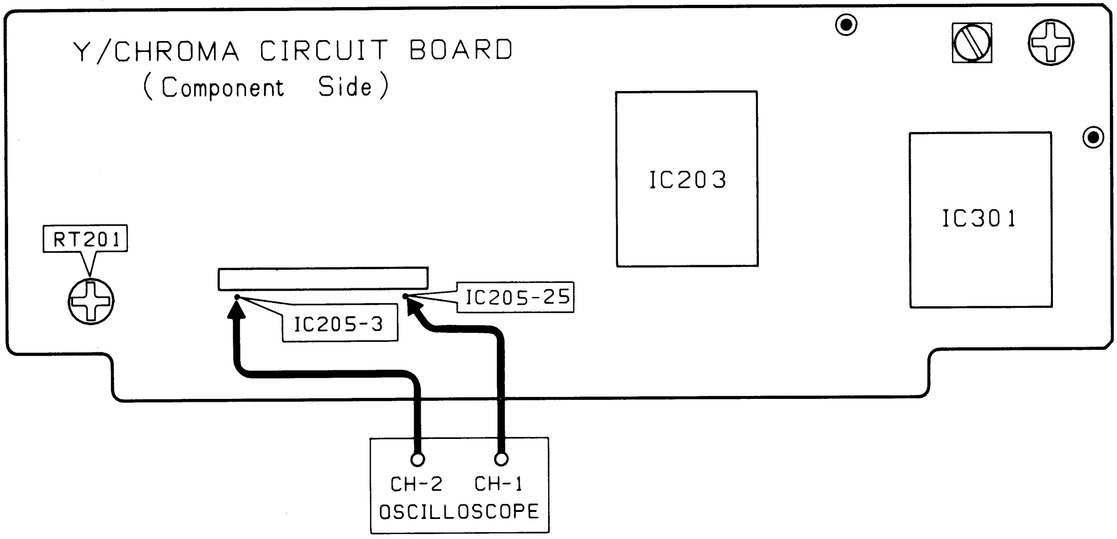
3. Y/CHROMA CIRCUIT ADJUSTMENT

1. CCD Level Adjustment

Purpose of adjustment and fault occurring if incomplete
Purpose:
Fault:

Test Equipment/Jigs	Test Equipment Connection Points	VTR State	Adjustment Point
● Oscilloscope ● Alignment tape	● CH-1: IC205-25 ● CH-2: IC205-3	● Play back alignment tape	● RT201

Connection Diagram


Y/CHROMA CIRCUIT BOARD
(Component Side)
IC203
IC301
RT201
IC205-3
IC205-25
CH-2 CH-1
OSCILLOSCOPE

Adjustment Procedure
Align the CH-1 and CH-2 levels.
CH-2 = CH-1 $^{+0}_{-10}$ mVp-p.

Note: CH-2 level is less than CH-1 level.

MC-Service

2. Secam Detect Level Adjustment

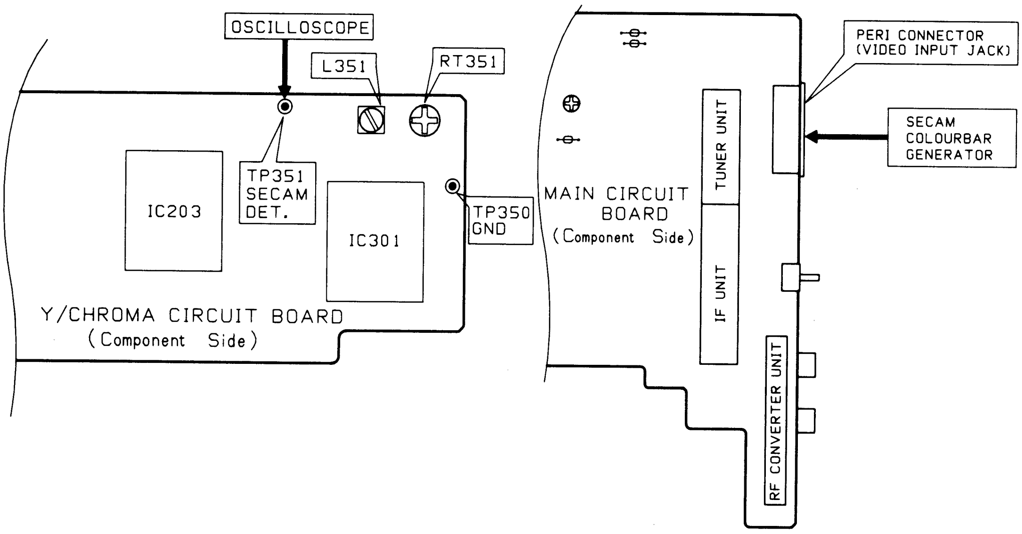
Purpose of adjustment and fault occurring if incomplete

Purpose:

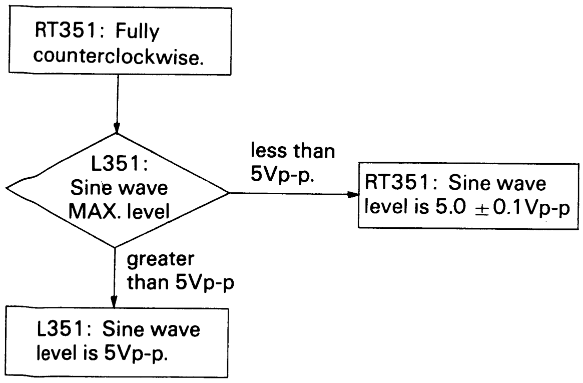
Fault:

Test Equipment/Jigs	Test Equipment Connection Points	VTR State	Adjustment Point
● SECAM colour bar generator ● Oscilloscope	● TP351 ● TP350 (GND)	● REC mode	● RT351

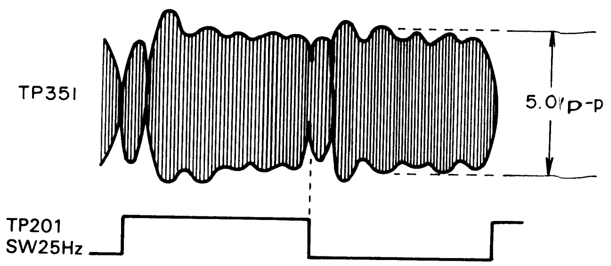
Connection Diagram


OSCILLOSCOPE
L351
RT351
TP351 SECAM DET.
IC203
IC301
TP350 GND
Y/CHROMA CIRCUIT BOARD (Component Side)
MAIN CIRCUIT BOARD (Component Side)
TUNER UNIT
IF UNIT
RF CONVERTER UNIT
PERI CONNECTOR (VIDEO INPUT JACK)
SECAM COLOURBAR GENERATOR

Adjustment Procedure


RT351: Fully counterclockwise.
L351: Sine wave MAX. level
less than 5Vp-p.
RT351: Sine wave level is 5.0 ±0.1Vp-p
greater than 5Vp-p
L351: Sine wave level is 5Vp-p.

Wave form



4. TIMER CIRCUIT ADJUSTMENTS

1. 4.19 MHz Crystal Adjustment

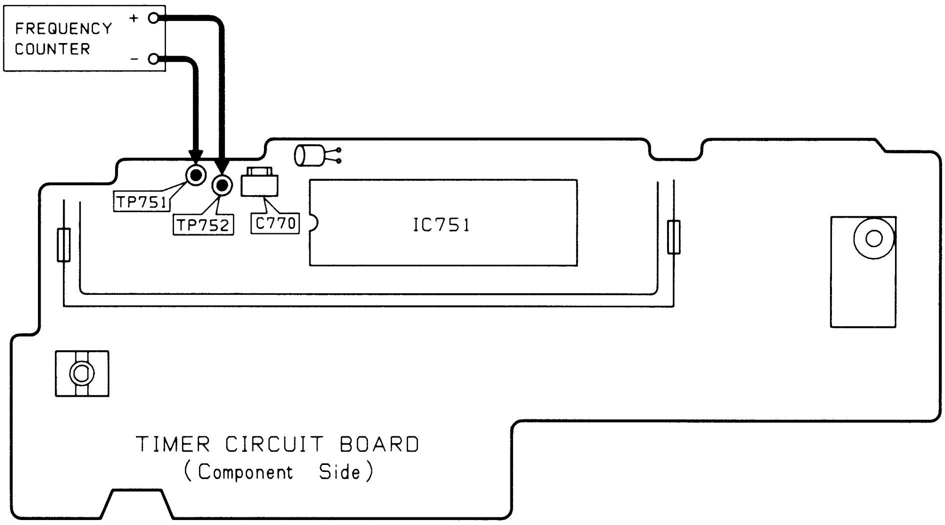
Purpose of adjustment and fault occurring if incomplete

Purpose: Suppress the time gain or lag of the timer less than 0.2 seconds per day.

Fault:

Test Equipment/Jig	Test Equipment Connection Points	VTR State	Adjustment Point
● Frequency counter	● TP751 (–) ● TP752 (+)	● Stop mode	● C770

Connection Diagram



FREQUENCY COUNTER
+
–
TP751
TP752
C770
IC751
TIMER CIRCUIT BOARD
(Component Side)

Adjustment Procedure

1) Set the counter gate time to 10 seconds.
2) The counter reads 4.1941902 MHz.

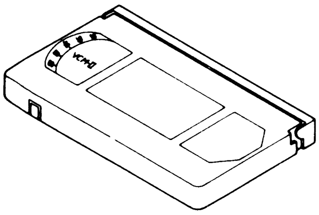
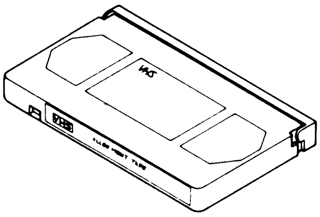
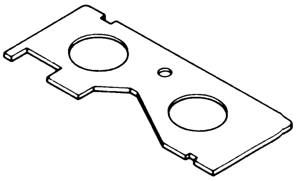
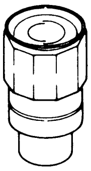
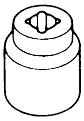
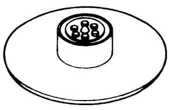
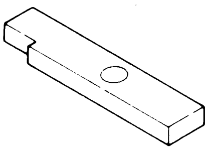
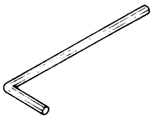
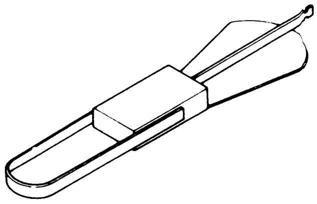
Note: Set the probe to 10 : 1 for use.

MC-Service

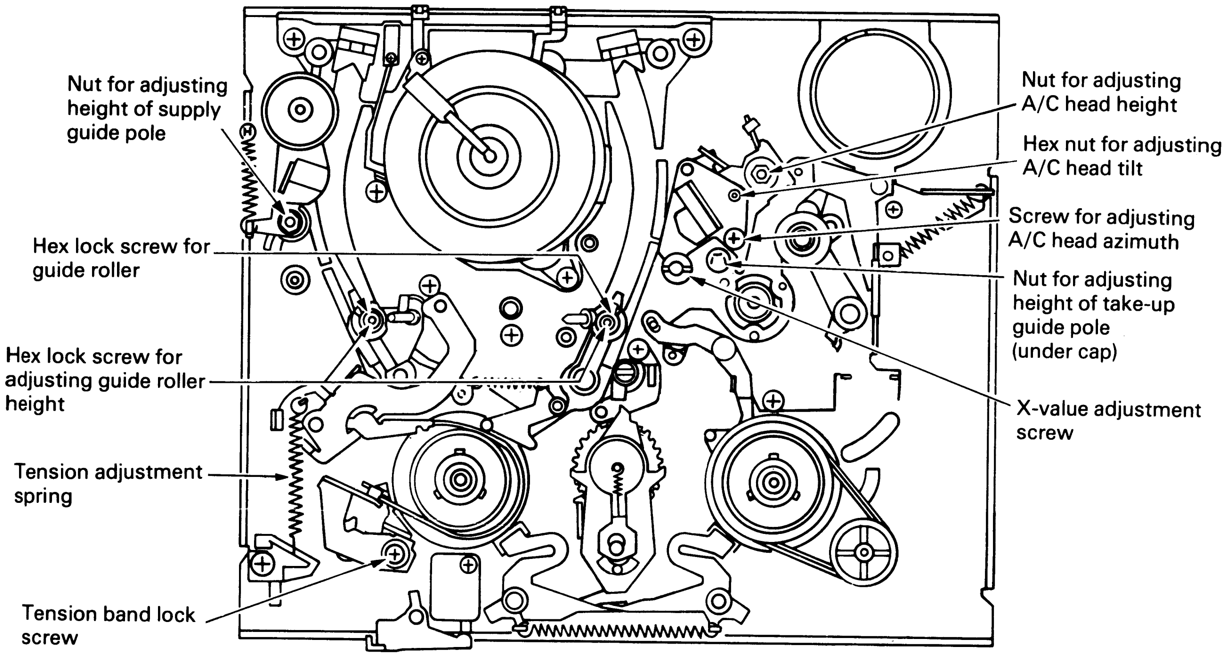
CHAPTER 4

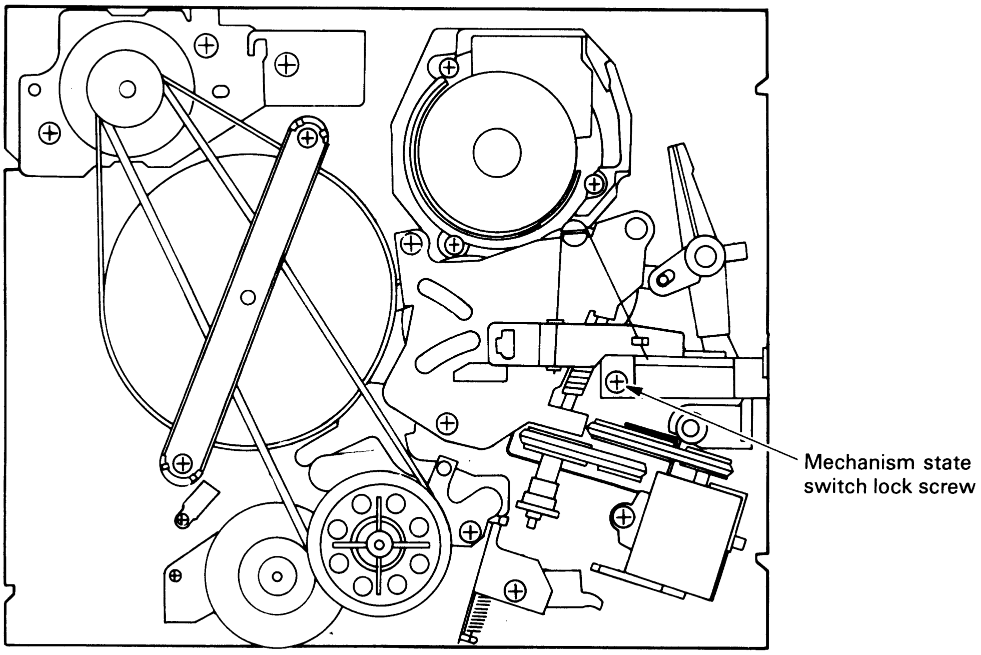
MECHANISM ADJUSTMENT

SERVICING JIGS AND TOOLS

1. Back tension meter Parts No. 7099004 	2. Alignment tape Parts No. 7099052 	3. Height reference plate (master plane) Parts No. 7099041 
4. Torque gauge Parts No. 7099039 	5. Torque gauge adaptor Parts No. 7099035 	6. Dummy reel Parts No. 7099043 
7. Reel disk height jig Parts No. 7099038 	8. 1.5 mm hexagonal wrench 	9. Fan-shaped tension gauge 

LIST OF ADJUSTMENT LOCATIONS


Nut for adjusting height of supply guide pole
Hex lock screw for guide roller
Hex lock screw for adjusting guide roller height
Tension adjustment spring
Tension band lock screw
Nut for adjusting A/C head height
Hex nut for adjusting A/C head tilt
Screw for adjusting A/C head azimuth
Nut for adjusting height of take-up guide pole (under cap)
X-value adjustment screw


Mechanism state switch lock screw

MECHANICAL COMPONENT ADJUSTMENT

1. Mechanism State Switch Adjustment

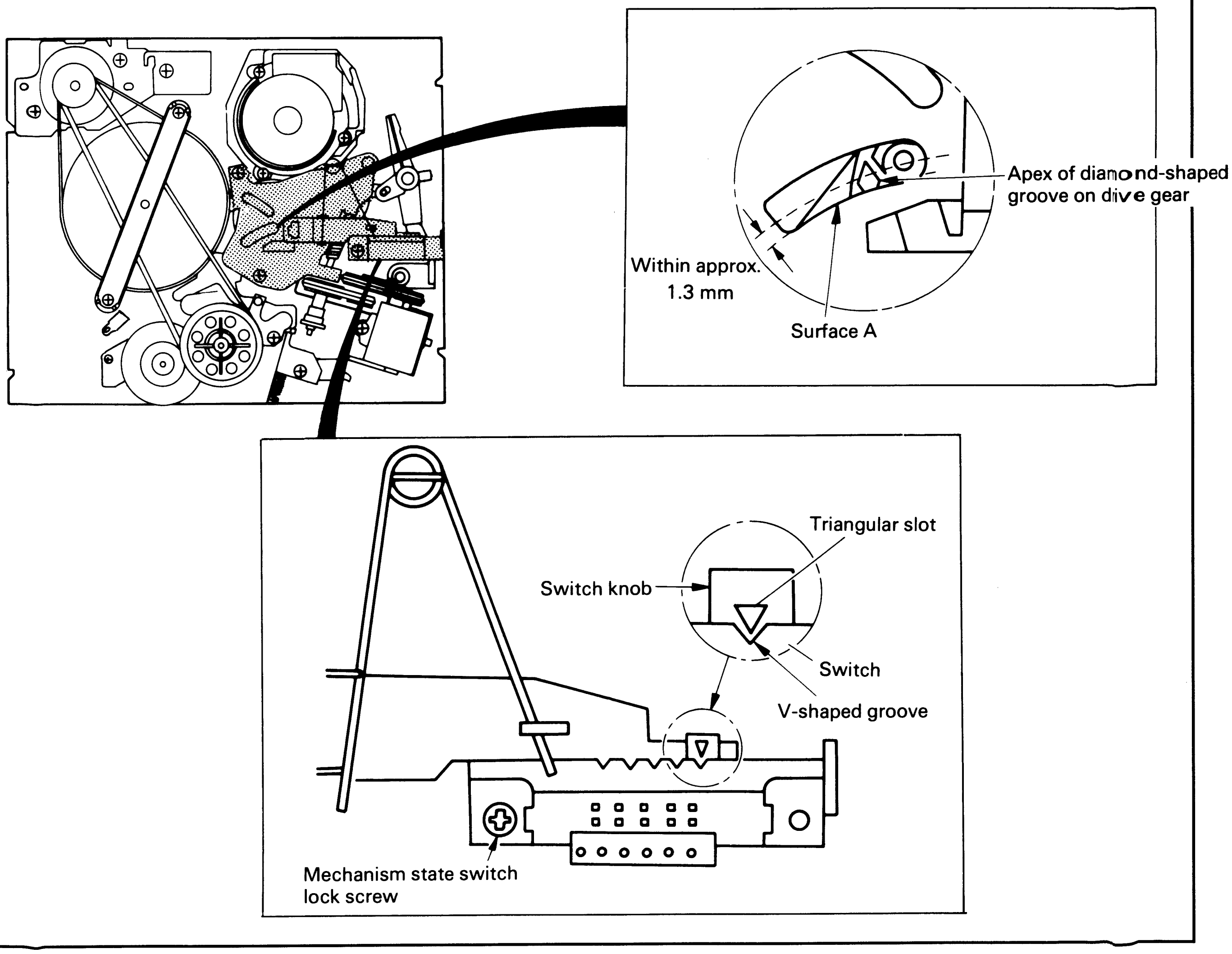
Purpose: Accurately detect mechanism states and prevent malfunction.

Test Equipment/Jigs	VTR State	Adjustment Point
● Blank tape	● Stop mode	● Mechanism state switch lock screw

Adjustment Procedure

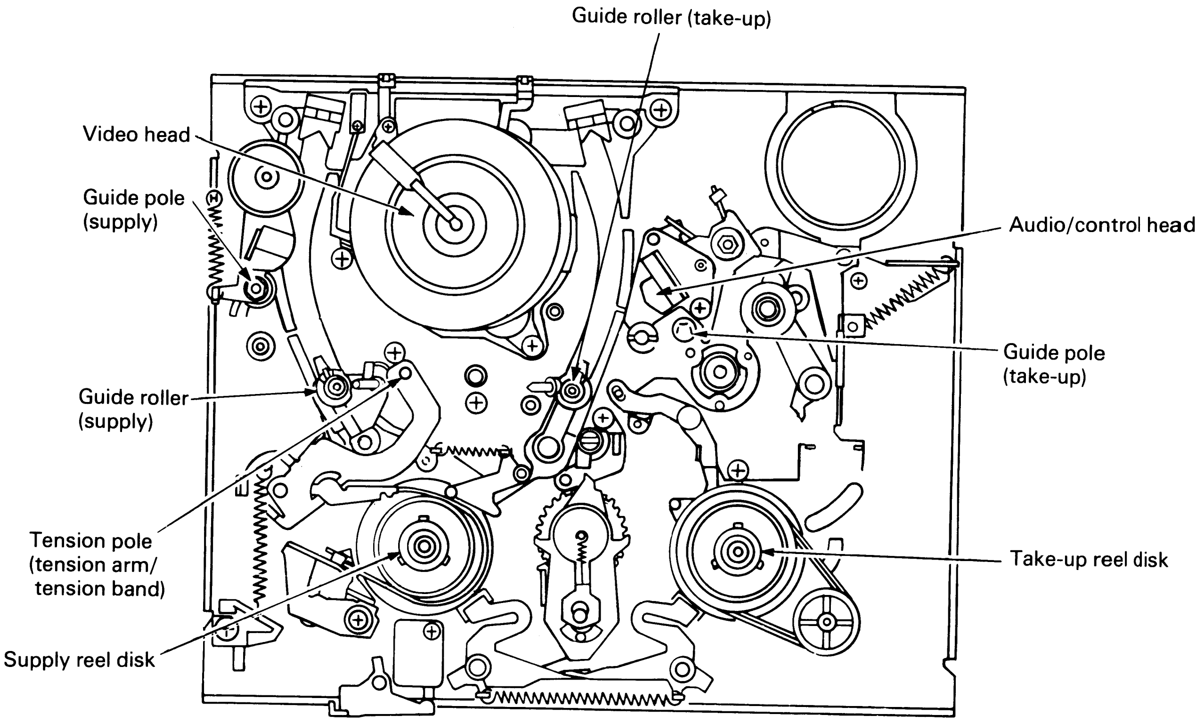
1) Turn the worm pulley by hand. Position the apex of the diamond-shaped groove on the drive gear so that it is within 1.3 mm from the A surface of the gear plate.
2) Loosen the lock screw on the mechanism state switch. Slide the switch so that the apex of the triangular slot on the switch knob is aligned with the V-shaped groove on the extreme outside of the switch.
3) Loosen the lock screw. Insert the blank tape in the cassette holder. Check to make sure that all unloading and loading operations are correct.

Adjustment Diagram


Apex of diamond-shaped groove on drive gear
Within approx. 1.3 mm
Surface A
Triangular slot
Switch knob
Switch
V-shaped groove
Mechanism state switch lock screw

TAPE TRANSPORT SYSTEM ADJUSTMENT

The transport system is the system in which tape moves from the supply reel disk, over the video head and then to the take-up reel disk. The components in the tape transport system must be perfectly clean, particularly those that come in contact with the tape.
These components must have no scratches, no dust, no oil on them. The tape transport system is adjusted at the factory prior to shipping. When components need to be replaced, accurately adjusting the new components ensures that the tape transport system will operate stably.


Guide roller (take-up)
Video head
Guide pole (supply)
Audio/control head
Guide pole (take-up)
Guide roller (supply)
Tension pole (tension arm/ tension band)
Take-up reel disk
Supply reel disk

Components Adjusted in Tape Transport System

1. Reel Disk Height Adjustment

Purpose: Determine correct tape height by setting cassette tape reel to the specified height.

Test Equipment/Jigs	VTR State	Adjustment Point
● Master plane ● Reel disk height jig	1) Remove chassis holder 2) Mount master plane and place reel disk height jig on it.	● Spacers in supply and take-up reel disks.

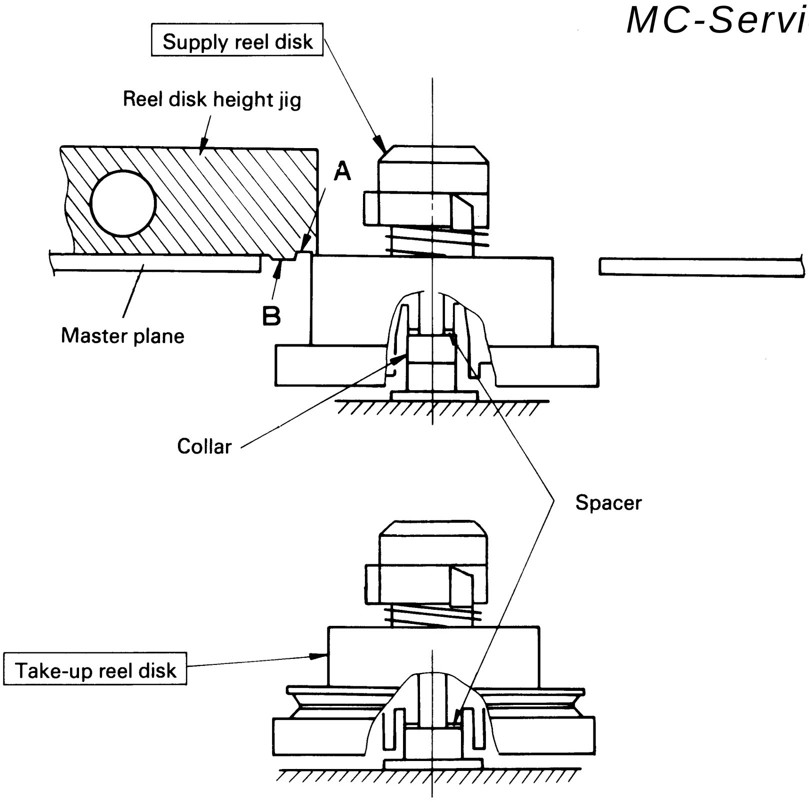
Adjustment Procedure

1) Make sure the reel disk is correctly positioned between points A and B on the reel disk height jig.
2) If the reel disk will not fit between points A and B, replace the spacer in the reel disk or adjust the number of spacers (0.25 mm and 0.5 mm thicknesses).

Caution:

If the tension arm/tension band have been removed, adjust the tension pole's position and tension after reassembling.

Adjustment Diagram


Supply reel disk
Reel disk height jig
A
Master plane
B
Collar
Spacer
Take-up reel disk

2. Tension/Tension Pole Position Adjustments

Purpose: Stabilize contact between video head and tape being supplied so that the tape tension is uniform throughout.

Test Equipment/Jigs	VTR State	Adjustment Point
● Flat-bladed screwdriver ● Tension cassette	1) Remove top cover 2) Place VTR in loading state without cassette insertion (see 4-17). **Tension adjustment** 3) Play tension cassette	**Position adjustment:** Tension band lock screw **Tension:** Tension spring hook position

Adjustment Procedure

Position Adjustment

1) Loosen lock screw on tension band. Insert flat bladed screwdriver in slot in bracket and chassis.
2) Use the screwdriver to slide the bracket for a 1 ~ 2 mm interval between the tension pole and chassis.
3) Tighten the lock screw on the tension band.
4) After adjusting, reload without inserting the tape and recheck the position of the tension pole.

Tension Adjustment

Reading of tension cassette:

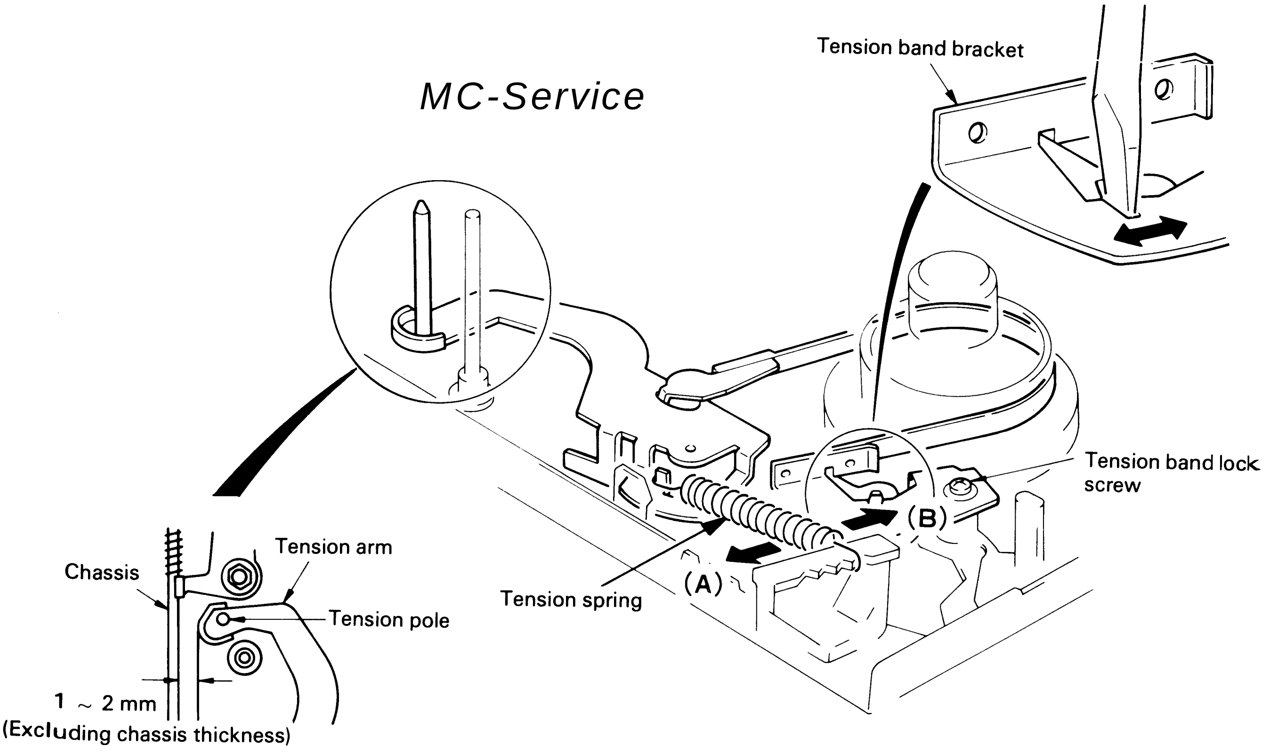
30 ~ 40 g-cm. (reference value)

If tension is higher than the reference value, move the spring in direction A.

If tension is lower than the reference value, move the spring in direction B.

Caution: If a 6 g-cm or larger change is made in tension position, recheck tension pole position. If the position is off, readjust the tension pole's position and tension.

Adjustment Diagram



3. Guide Pole Height Adjustment

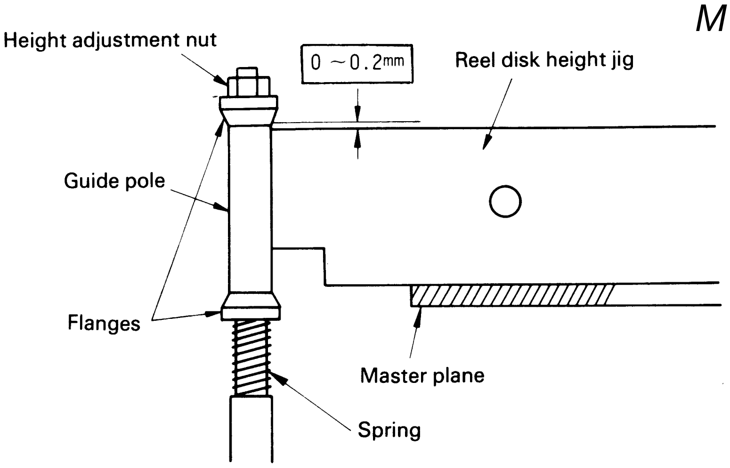
Purpose: Control tape height.

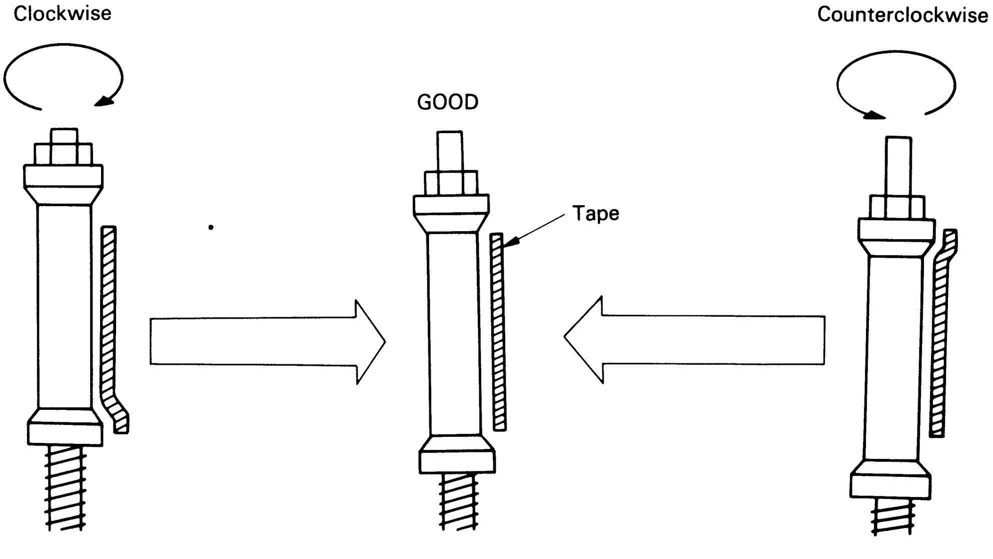
Test Equipment/Jigs	VTR State	Adjustment Point
● Master plane ● Reel disk height jig ● Blank tape	1) Remove chassis holder 2) Mount master plane and place the reel disk height jig on it.	● Nut for adjusting height of supply and take-up guide poles (take-up pole is under cap).

Adjustment Procedure

1) Adjust gap between guide pole's upper flange and reel disk height jig to 0 ~ 0.2 mm.
2) Load and run the blank tape. Check to make sure the tape does not ride over the pole's upper or lower flange.
3) If the tape does ride over, adjust guide pole height.
   If tape rides over upper flange, turn adjustment nut counterclockwise.
   If tape rides over lower flange, turn adjustment nut clockwise.

Adjustment Diagram


Height adjustment nut
0 ~ 0.2mm
Reel disk height jig
Guide pole
Flanges
Master plane
Spring


Clockwise
GOOD
Tape
Counterclockwise

4. Guide Roller Height Adjustments

Purpose: Control tape height so the tape's bottom edge runs along the cylinder's tape guideline.

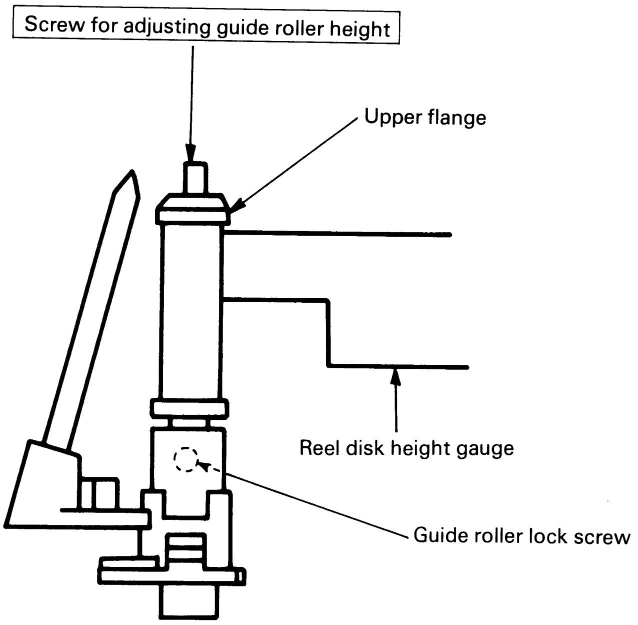
Coarse Adjustment

Test Equipment/Jigs	VTR State	Adjustment Point
● Master plane ● Reel disk height jig ● 1.5 mm hexagonal wrench	1) Remove chassis holder 2) Mount master plane and place reel disk height jig on it.	● Screws for adjusting height of supply and take-up guide roller

Adjustment Procedure

1) Loosen guide roller lock screw so that the guide roller does not turn during loading, unloading and playback.
2) Set the upper edge of the reel disk height jig to the same level as the guide roller's upper flange.
3) Now make precision adjustments.

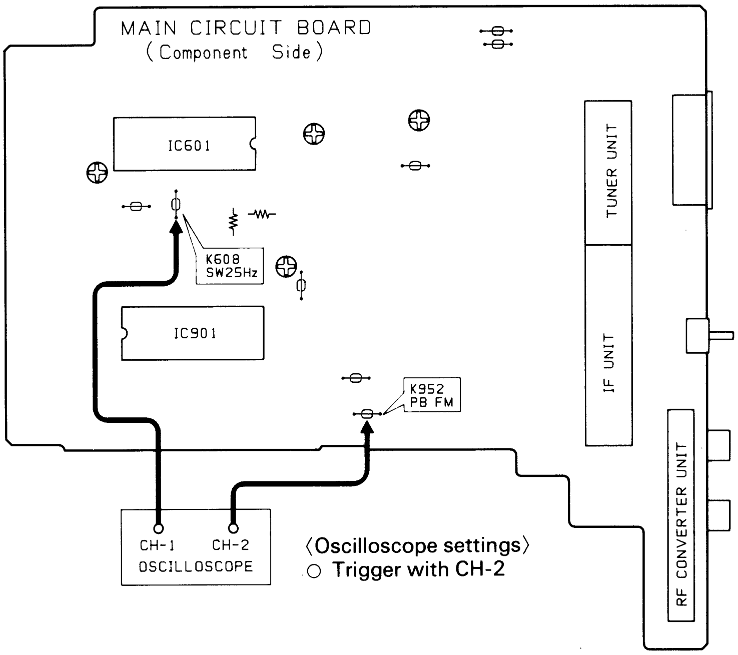
Adjustment Diagram


Screw for adjusting guide roller height
Upper flange
Reel disk height gauge
Guide roller lock screw

Precision Adjustment

Test Equipment/Jigs	Test Equipment Connection Point	VTR State	Adjustment Point
● Oscilloscope ● Alignment tape ● Hexagonal wrench	● CH-1: K952 ● CH-2: K608	● Playback alignment tape	● Screw for adjusting guide roller height

Connection Diagram

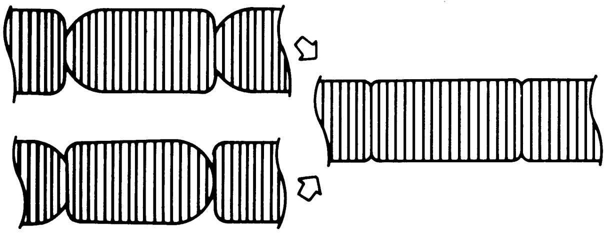

MAIN CIRCUIT BOARD
(Component Side)
IC601
K608
SW25Hz
IC901
K952
PB FM
TUNER UNIT
IF UNIT
RF CONVERTER UNIT
CH-1
CH-2
OSCILLOSCOPE

〈Oscilloscope settings〉
○ Trigger with CH-2

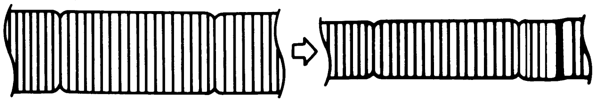
Adjustment Procedure

1) Tracking control: centered (when making this adjustment after replacing the cylinder, set the tracking control so the FM output is maximum.
2) Turn height adjustment screw to flatten the FM waveform.
3) Turn the tracking control clockwise.
4) Make sure that FM drops at the head and tail.
5) Tighten lock screw.

Waveform



Turn guide roller height adjustment screw a little at a time to flatten waveform.

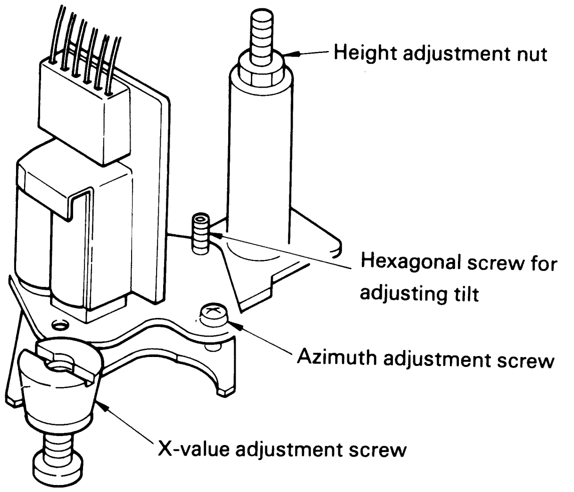


Tracking control centred

Turn tracking control clockwise

5. Audio and Control Head

Purpose: Ensure uniform contact between tape and head to record and play a prescribed track.


Height adjustment nut
Hexagonal screw for adjusting tilt
Azimuth adjustment screw
X-value adjustment screw

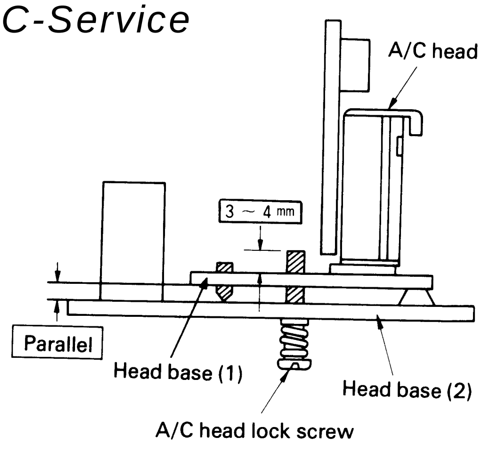
Coarse Adjustment

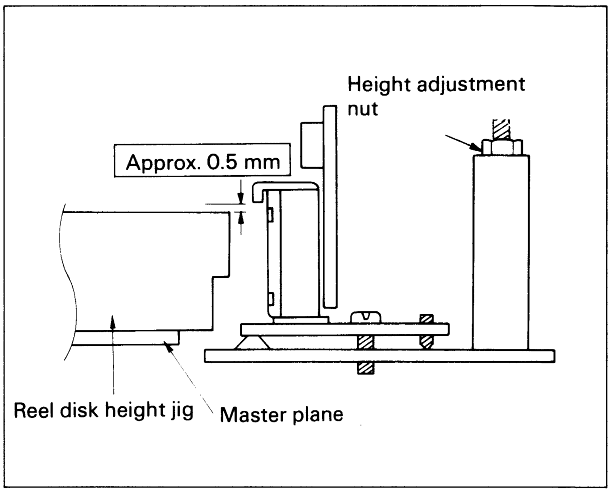
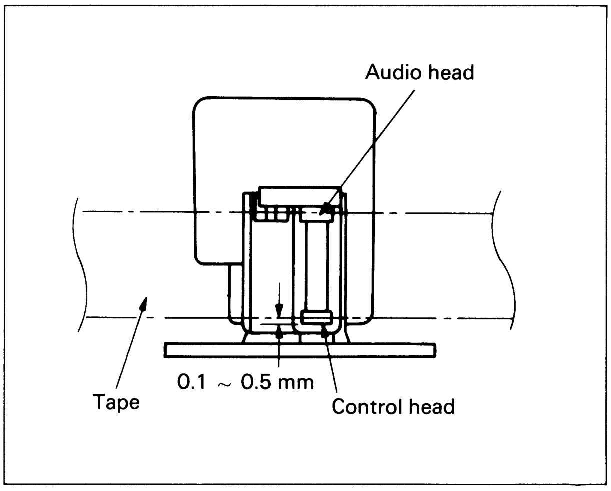
Test Equipment/Jigs	VTR State	Adjustment Point
● Master plane ● Reel disk height jig ● Blank tape ● Hexagonal wrench	1) Remove chassis holder 2) Mount master plane and place reel disk height jig on it.	● Azimuith adjustment screw ● Height adjustment nut ● Tilt adjustment screw

Adjustment Procedure

1) Tighten the A/C head lock screw through the spring from the bottom of head base (2) until the screw tip protrudes 3 ~ 4 mm from the top surface of head base (1).
2) Turn the tilt adjustment hexagonal screw and the azimuth adjustment screw so that head base (1) and head base (2) are parallel.

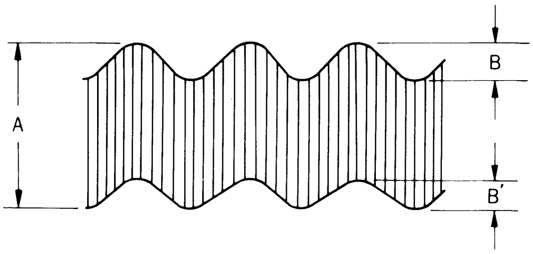
Adjustment Diagram


A/C head
3 ~ 4 mm
Parallel
Head base (1)
Head base (2)
A/C head lock screw

Adjustment Procedure	Adjustment Diagram
3) Turn the height adjustment nut until the gap between reel disk height jig and A/C head is approx. 0.5 mm.	 Height adjustment nut Approx. 0.5 mm Reel disk height jig Master plane
4) Remove the adjustment jigs and insert a blank tape. Place in playback mode. Make sure the tape does not curl or ride over around the A/C head. If the tape curls or rides over, readjust the tilt adjustment hex screw, the azimuth adjustment screw and the height adjustment nut. The ideal A/C head height is with the tap's bottom edge 0.1 ~ 0.15 mm from the bottom edge of the control head's core. 5) Now move on to precision adjustments.	

Precision Adjustment

Test Equipment/Jigs	Test Equipment Connection Point	VTR State	Adjustment Point
● Hexagonal wrench ● Oscilloscope ● Alignment tape	● Audio output jack	● Playback alignment tape (7 kHz portion)	● Azimuth adjustment screw ● Height adjustment nut ● Tilt adjustment screw

Adjustment Procedure	Waveform Diagram
1) Alternate turning, a little at a time, of the azimuth adjustment screw, the height adjustment nut and the tilt adjustment hex screw to both maximize and flatten audio output (minimize fluctuation).	 A: maximum BB': minimum

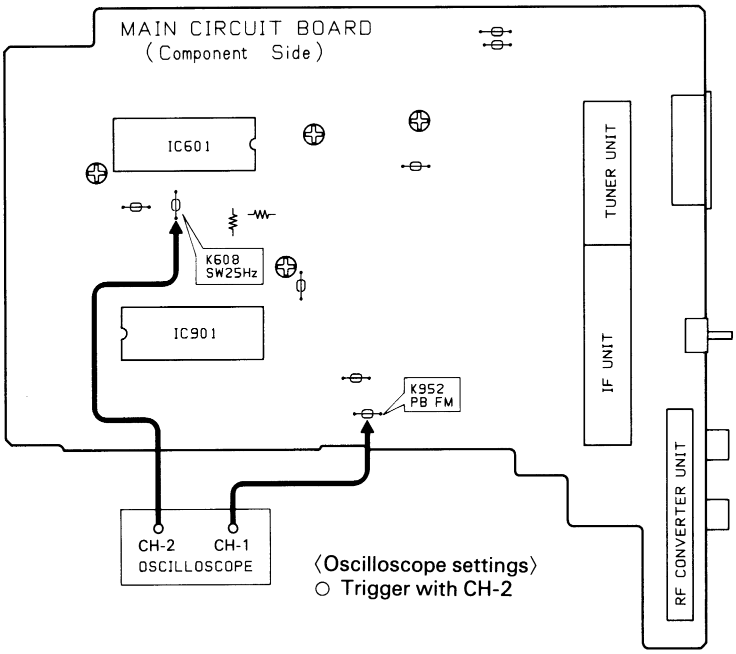
6. X Value Adjustment

Purpose: Ensure compatibility with other VTRs.

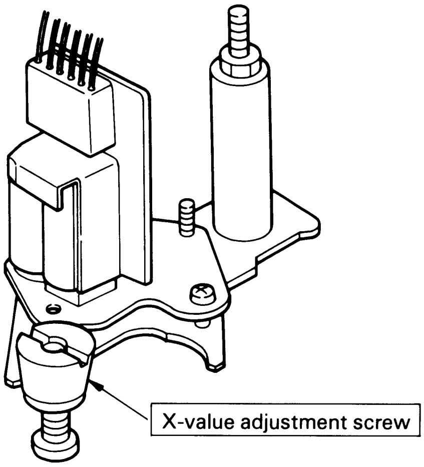
Caution: Be sure to adjust the tracking preset before making this adjustment.

Test Equipment/Jigs	Test Equipment Connection Point	VTR State	Adjustment Point
● Oscilloscope ● Alignment tape ● X-value adjustment screwdriver	● CH-1 : K952 ● CH-2 : K608	● Play back alignment tape	● X-value adjustment screw

Connections Diagram

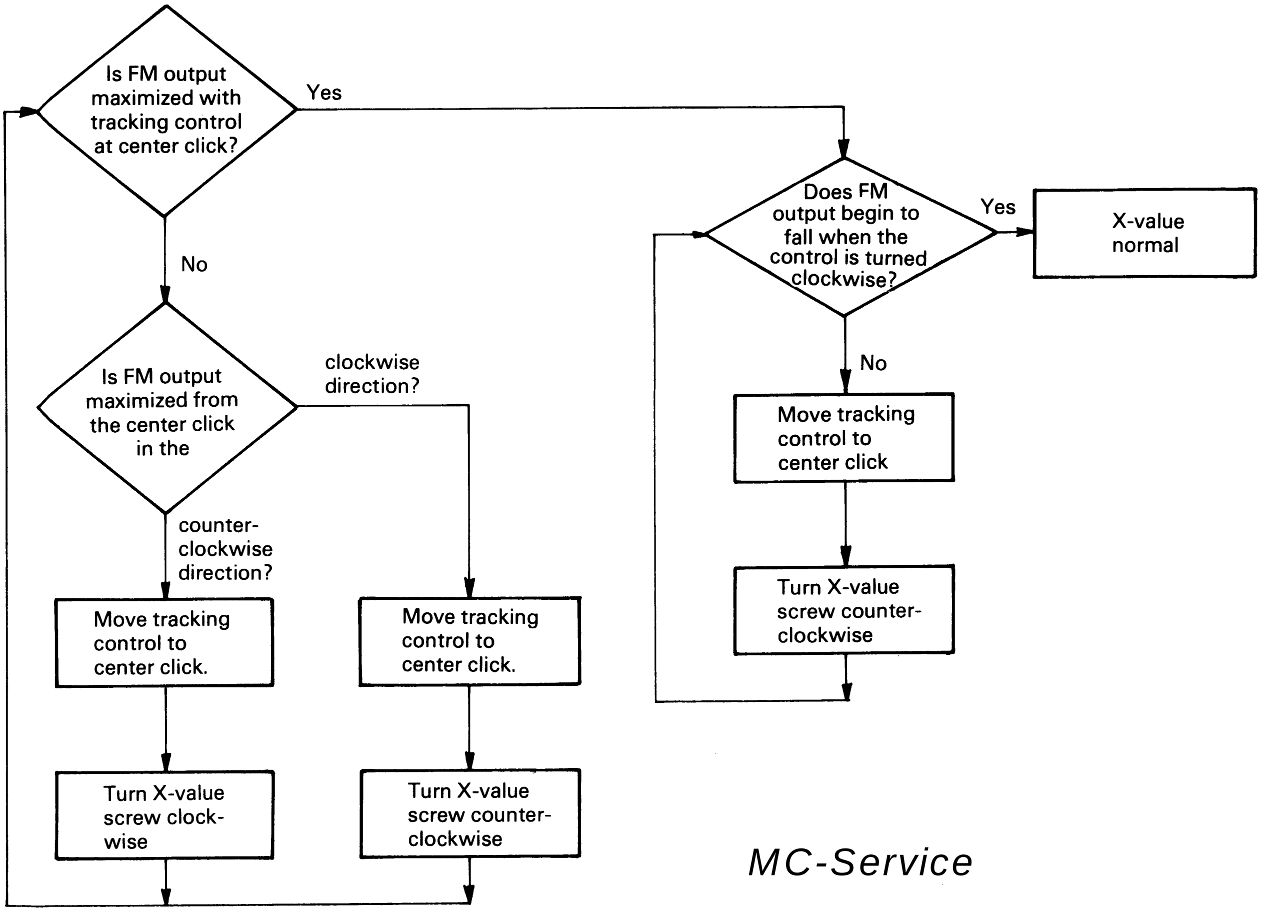

MAIN CIRCUIT BOARD
(Component Side)
IC601
K608
SW25Hz
IC901
K952
PB FM
TUNER UNIT
IF UNIT
RF CONVERTER UNIT
CH-2
CH-1
OSCILLOSCOPE

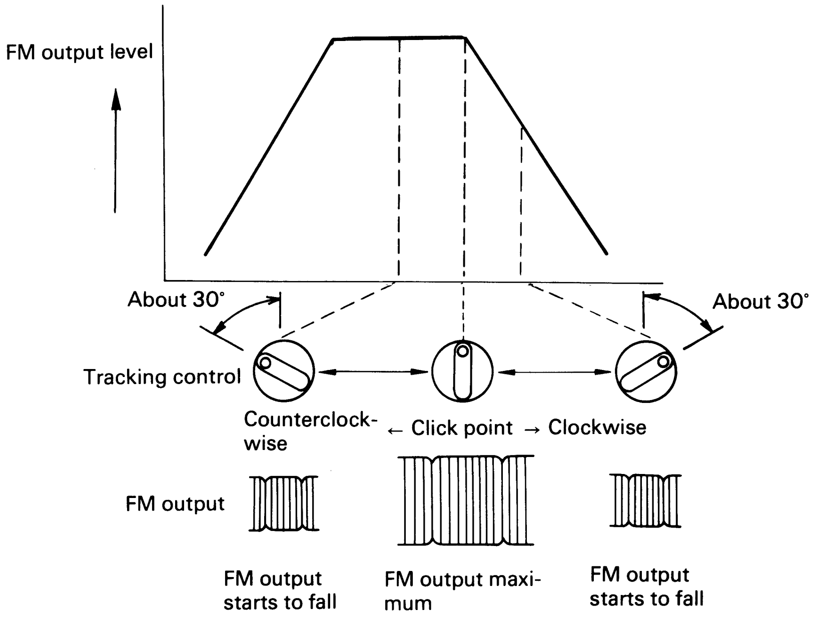
⟨Oscilloscope settings⟩
○ Trigger with CH-2


X-value adjustment screw

Adjustment Procedure

Since the 65 μm head will trace over 49 μm width track, center tracking control and make adjustments to maximize FM output, or turn the control clockwise about 30° and adjust so that FM output begins to fall. (Is FM output maximized with tracking control at center click?)


Is FM output maximized with tracking control at center click?
Yes
No
Is FM output maximized from the center click in the
clockwise direction?
counter-clockwise direction?
Move tracking control to center click.
Turn X-value screw clockwise
Move tracking control to center click.
Turn X-value screw counter-clockwise
Does FM output begin to fall when the control is turned clockwise?
Yes
X-value normal
No
Move tracking control to center click
Turn X-value screw counter-clockwise

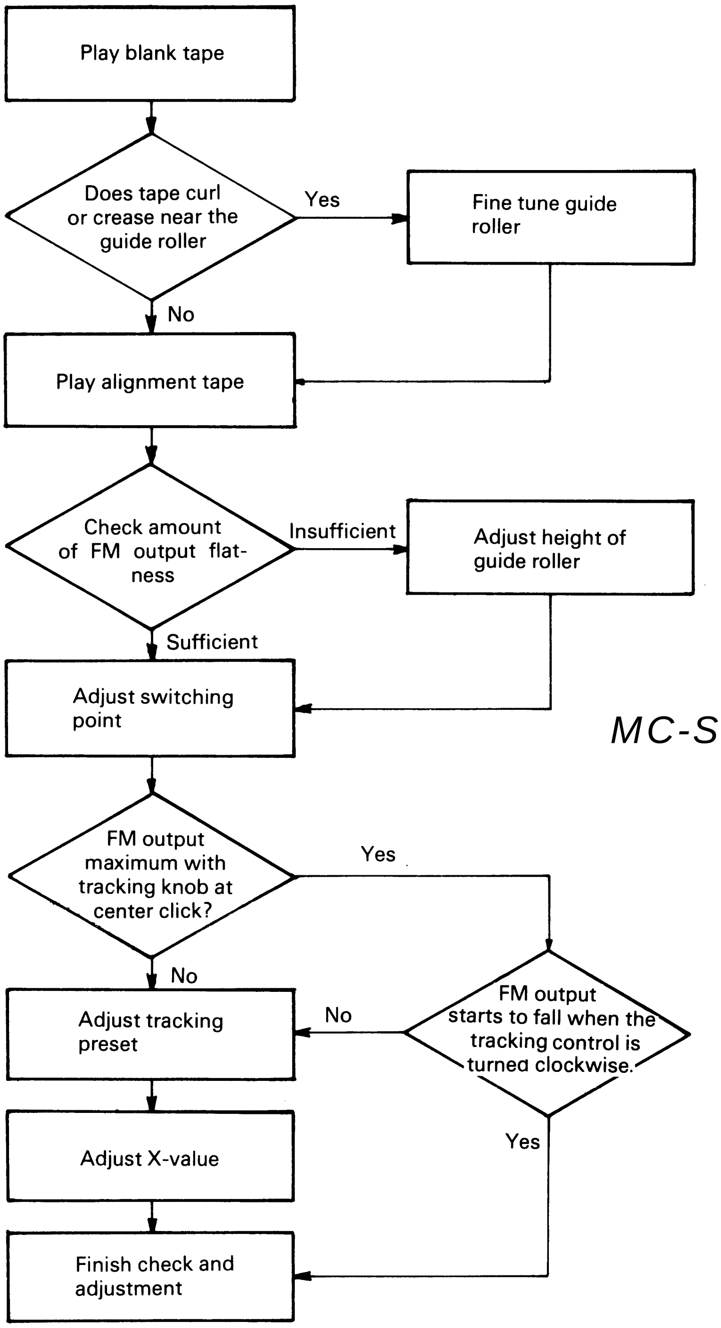

FM output level
About 30°
About 30°
Tracking control
Counterclockwise ← Click point → Clockwise
FM output
FM output starts to fall
FM output maximum
FM output starts to fall

7. Adjustments after replacing Cylinder (Video Head)

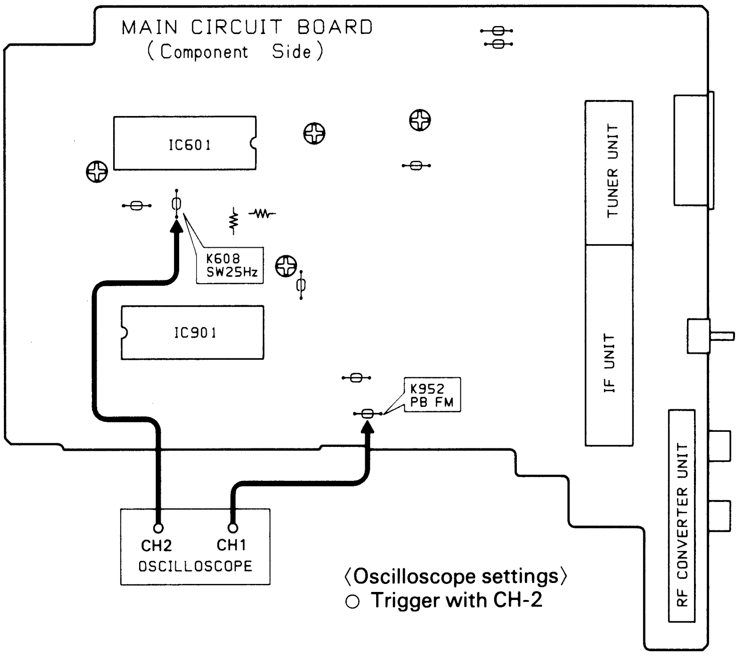
Purpose: A new replacement cylinder will differ with the guide roller in X-value and relative height. But, correct replacement procedures will reduce this disparity to a minimum.

Test Equipment/Jigs	Test Equipment Connection Points	Adjustment Points
● Oscilloscope ● Alignment tape ● Blank tape ● Hexagonal wrench ● X-value adjustment screwdriver	● Check amount of flattening ● CH-1 : K952 ● CH-2 : K608	● Guide roller (see precision adjustment on page 4-9) ● Switching point (see section 3) ● Tracking preset (see section 3) ● X-value (see page 4-12)

Check and Adjustment Procedures


Play blank tape
Does tape curl or crease near the guide roller
Yes
Fine tune guide roller
No
Play alignment tape
Check amount of FM output flatness
Insufficient
Adjust height of guide roller
Sufficient
Adjust switching point
FM output maximum with tracking knob at center click?
Yes
No
Adjust tracking preset
No
FM output starts to fall when the tracking control is turnea clockwise.
Yes
Adjust X-value
Finish check and adjustment

Connection Diagram

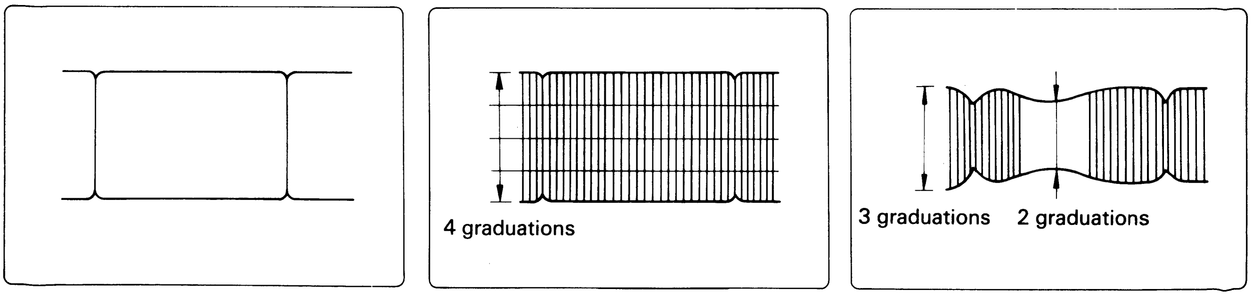

MAIN CIRCUIT BOARD
(Component Side)
IC601
K608
SW25Hz
IC901
K952
PB FM
TUNER UNIT
IF UNIT
RF CONVERTER UNIT
CH2
CH1
OSCILLOSCOPE

〈Oscilloscope settings〉
○ Trigger with CH-2

Procedures for checking amount of fluctuations and flatness in FM output

1) Use tracking control to maximize FM output.
2) Fine tune the oscilloscope's voltage level range to adjust FM output to 4 graduations.
3) Turn the tracking control to set the FM output's maximum amplitude at 3 graduations.
4) Make sure the minimum amplitude at this time is at 2 graduations or higher.
5) Make sure the difference between maximum and minimum level fluctuation is 13% or less.

Waveform Diagram


4 graduations
3 graduations
2 graduations

8. Checking Tension and Torque

Purpose: Checking tension torque and pressure on the components that wind and move the tape is necessary to ensure smooth tape run and fulfill the VTR's basic functions. Make this check when tape run is rough or tape speed is incorrect.

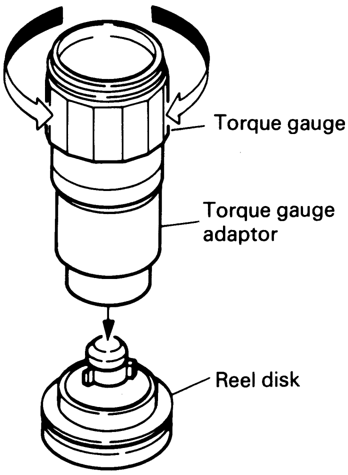
Test equipment/jigs	VTR state
● Torque gauge ● Torque gauge adaptor ● Fan-shaped tension gauge ● Dummy reel	● Operate VTR without loading tape cassette (see page 4-17)

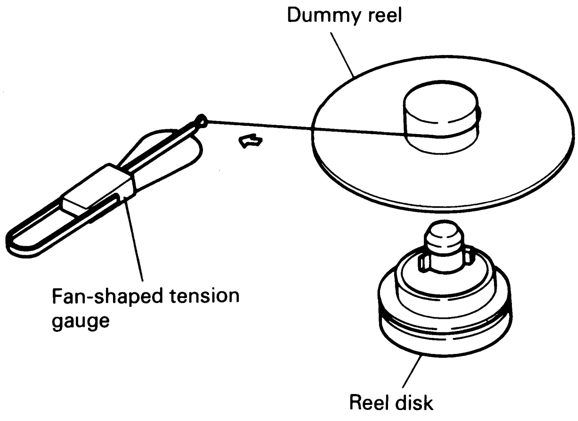
Item	VTR Operation mode	Measurement reel	Measurement values	Remarks
Main brake torque	Stop	Supply and take-up reels	170 g·cm or more	Note 1
Slack removal torque	Unloading	Supply reel	90 ~ 190 g·cm	Note 1
Fast forward torque	Fast forward	Take-up reel	400 g·cm or more	Note 1
Rewind torque	Rewind	Supply reel	400 g·cm or more	Note 1
Reel winding torque	Play	Take-up reel	90 ~ 180 g·cm	Note 1
Back-tension torque	Fast forward	Supply reel	4 ~ 15 g·cm	Note 2
	Rewind	Take-up reel		

Note: 1. Value when using torque gauge and torque gauge adaptor for measurement with torque gauge sliding at 0.8 rps. However, main brake torque indicates measurement values during manual rotation of take-up reel, counterclockwise, and supply reel, clockwise, at 0.8 rps.

Note: 2. Indicates the value when the dummy reel and fan-shaped tension gauge are used to measure the take-up reel disk pulling counterclockwise and the supply reel disk pulling clockwise at 50 mm/s.

Adjustment Diagram





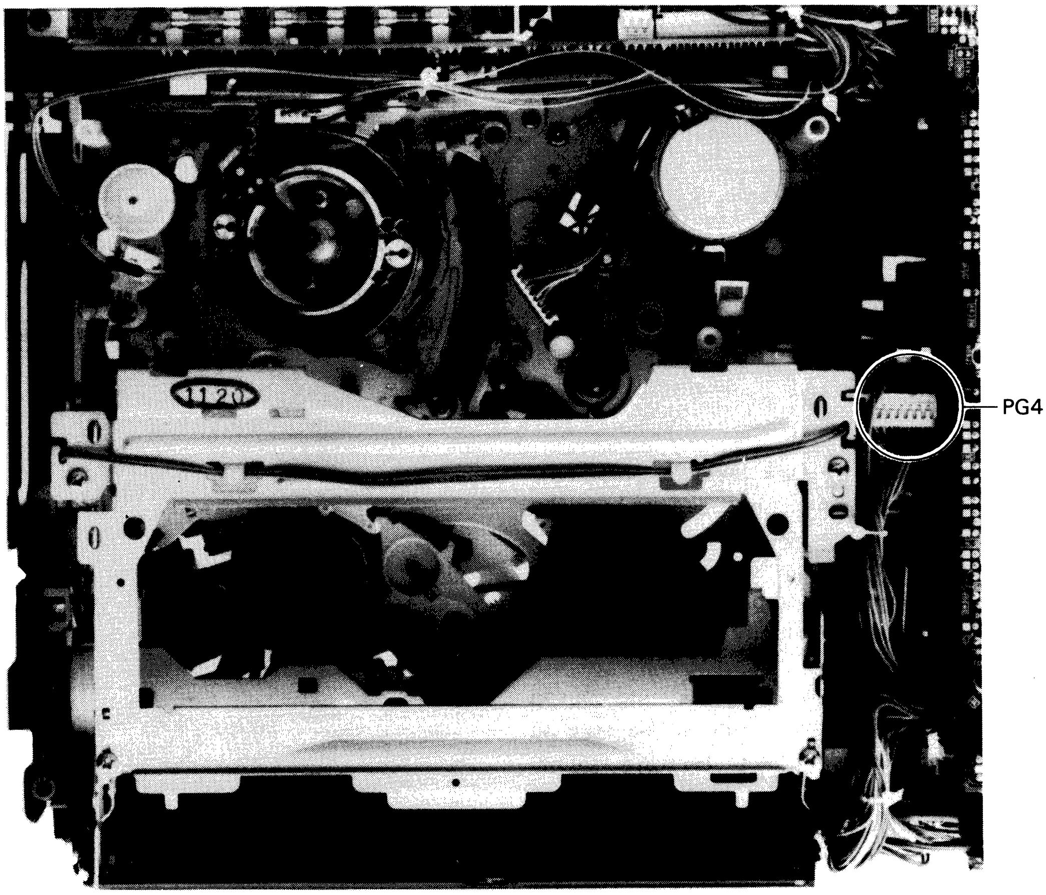
Note: Method with VTR in loading state and no tape cassette inserted.

1) Remove top cover.
2) Remove AC plug from wall socket.
3) Disconnect the connector from the plug (PG-4) on the cassette loading motor circuit board.
4) Short-circuit pins 2 and 5 of the connector.
5) Insert AC plug into wall socket.
6) Turn VTR power on.
   In this state, the VTR will accept all modes. However, rewind can be performed for only a few seconds because the take-up disk is in stop state and reel pulses cannot be detected.

[Caution]

After the above operations, always use the following steps to return to the original modes.

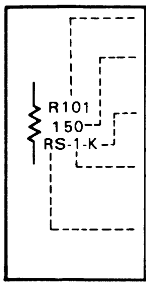
1) Remove short-circuit from connector and insert in plug.
2) Remove the AC plug from the wall socket once to reset the system control microprocessor.



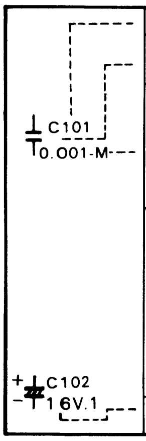
SCHEMATIC/CIRCUIT BOARD DIAGRAMS

Note

1. Voltage measured at base of chassis with minimum volume control and no signal.
   ( ) are shown in recording condition.
2. Nomenclature of Resistors and Capacitors.



Circuit No.	
Value	No indicated Ω (Ohm) M : 1000kΩ
Tolerance	No indicated ±5% K: ±10% M: ±20%
Wattage	No indicated ¼ W
Sort	No indicated Carbon film RC : Composition RW : Wire wound RS : Oxide metal film RN : Fixed metal film

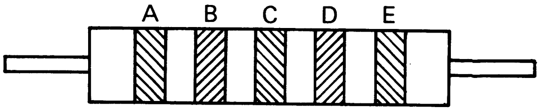


Circuit No.		
Value	No indicated μF P : PF	
Tolerance	No indicated ±10% J : ± 5% M: ±20% Z : +80%, −20% D : ±0.5pF C : ±0.25pF	
Sort	╪	Ceramic
	+ ╪ −	Electrolitic
	M ╪	Mylar
	P ╪	Polyester
	S ╪	Styrol
Voltage	No indicated 50WV	

3. Be sure to make your orders of resistors and capacitors with value, voltage, tolerance and sort.
4. When replacing capacitors marked with * use specified ones stated on parts list since required temperature characteristics.

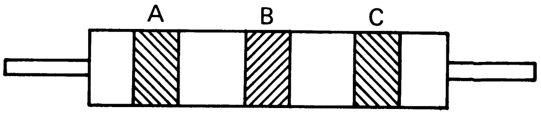
HOW TO READ CAPACITY AND INDUCTANCE OF RESISTOR SHAPE CAPACITORS AND COILS

CAPACITOR



CAPACITY: (10A+B)xC [PF]
TOLERANCE: D
RATED VOLTAGE: BODY COLOR
Pink: 25V
Green: 50V
CHARACTERISTICS: E

COIL



INDUCTANCE: (10A+B)xC [μH]

COLOR	A, B	C	D	E
Black	0	10^0	±20%	For temperature compensation
Brown	1	10^1		
Red	2	10^2		
Orange	3	10^3		
Yellow	4	10^4		
Green	5	10^5		
Blue	6			
Violet	7			
Grey	8		±30%	High dielectric constant type
White	9			For temperature compensation
Gold		10^{-1}	± 5%	
Silver		10^{-2}	±10%	High dielectric constant type

Cautions on use of MOS IC

1. The MOS IC is inserted in black foam for shipment. This foam is a conductor which short-circuits between the leads to prevent damage. Do not remove ICs from this foam during their storage. Avoid removing ICs from this foam, placing them on plastic which is likely to be charged with static electricity or inserting them into styrol foam.
2. High voltages may be applied during soldering caused by leakages from the soldering iron, so be sure to ground the tip of the soldering iron or use a low voltage soldering iron.
3. The human body, clothes made of synthetic fibres or nylon gloves may be charged with several thousands volts of static electricity because of friction, so a worker should be grounded.
4. Be sure to ground measuring instruments such as oscilloscopes, VTVMs, etc. used for repairs.

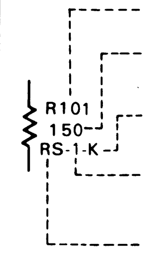
MC-Service

KAPITEL 5

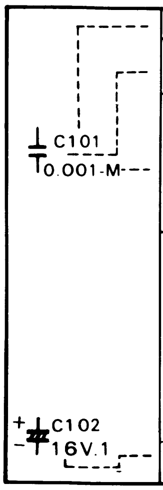
SCHALTPLAN/LEITERPLATTEN-DIAGRAMM

Hinweise:

1. Die aufgeführten Spannungswerte wurden bei auf Minimum gestelltem Lautstärkeregler und ohne Signal gemessen. Die in Klammern ( ) gestellten Werte gelten für den Aufnahmemodus.
2. Bezeichnung der Widerstände und Kondensatoren



Schaltkreis-Nr.	
Wert	Keine Angabe: Ohm M: 1000 kOhm
Toleranz	Keine Angabe: ± 5% K: ±10% M: ±20%
Wattzahl	Keine Angabe: 1/4W
Bauart	Keine Angabe: Kohlefilm RC: Verbundbauweise RW: Drahtspule RS: Metalloxidfilm RN: Fester Metallfilm



Schaltkreis-Nr.		
Wert	Keine Angabe: µF P : PF	
Toleranz	Keine Angabe: ±10% J : ± 5% M : ±20% Z : +80%, −20% D : ±0.5pF C : ±0.25pF	
Bauart		Keramik
	+ −	Electrolyt
	M	Mylar
	P	Polyester
	S	Styrol
Spannung	Keine Angabe: 50V	

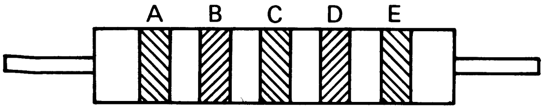
3. Bei der Bestellung von Widerständen und Kondensatoren unbedingt Wert, Spannung und Bauart angeben.
4. Werden die mit "*" markierten Kondensatoren ausgetauscht, dann müssen due in der Stückliste spezifizierten Kondensatoren verwendet werden, da diese spezielle Temperatureigenschaften aufweisen.

Vorsichtsmaßnahmen bei der Verwendung von MOS-ICs

1. Die MOC-ICs werden für den Versand in schwarzem Schaumstoff verpackt. Dieser Schaumstoff ist elektrisch leitend und schließt die Leiter kurz, um Beschädigungen zu vermeiden. Die ICs während der Lagerung niemals aus der Schaumstoffverpackung entfernen. Die ICs nur unmittelbar vor der Verwendung auspacken und niemals auf Plastikteilen ablegen (statische Elektrizität!) bzw. in Styrol-Schaumstoff einsetzen.
2. Aufgrund von Leckagen am Lötkolben kann es während des Lötens zu Hochspannungen kommen; daher immer die Spitze des Lötkolbens erden und nur einen Niederspannungs-Lötkolben verwenden.
3. Statische Elektrizität von einigen tausend Volt kann sich aufgrund von Reibung im menschlichen Körper bzw. in aus Kunstfasern hergestellten Kleidern und Handschuhen aufbauen. Daher sollten auch die mit der Handhabung von ICs betrauten Personen geerdet werden.
4. Unbedingt die für die Reparaturen verwendeten Meßinstrumente wie Oszilloskop, Röhrenvoltmeter usw. erden.

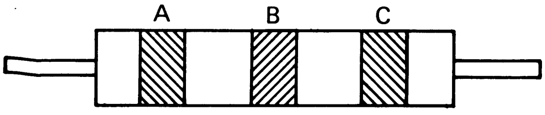
Ablesen der Kapazität und Induktivität der in Form von Widerständen ausgeführten Kondensatoren und Spulen

Kondensator



Kapazität: (10A+B)xC (pF)
Toleranz: D
Nennspannung: Farbe Rosa: 25V
Grün: 50V
Kennlinie: E

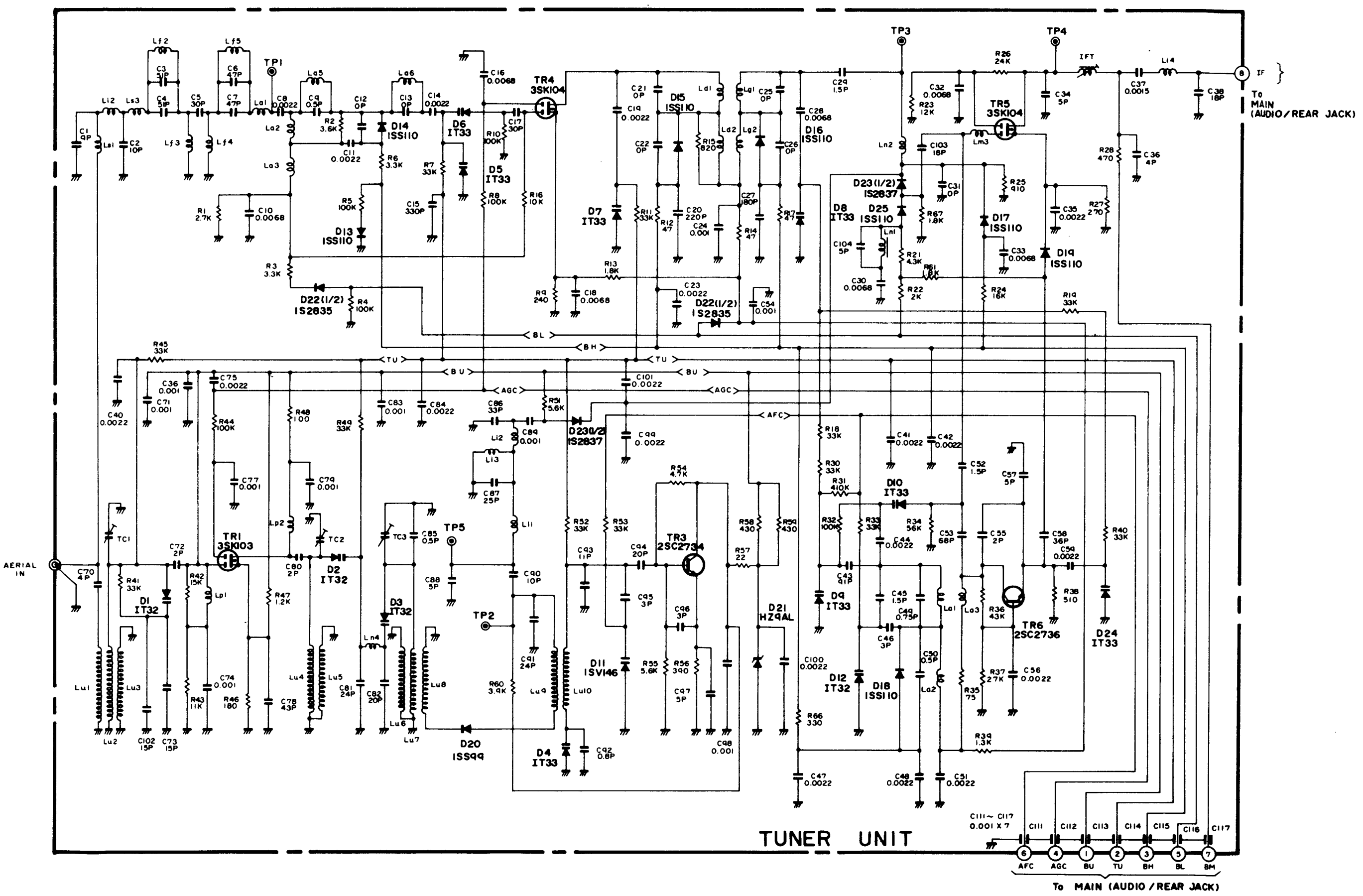
Spule



Induktivität: (10A+B)xC (µH)

Farbe	A, B	C	D	E
Schwarz	0	10^0	±20%	Für Temperature-Kompensation
Braun	1	10^1		
Rot	2	10^2		
Orange	3	10^3		
Gelb	4	10^4		
Grün	5	10^5		
Blau	6			
Violett	7			
Grau	8		±30%	Bauart mit hoher Dielektrizitätskonstanter
Weiß	9			Für Temperatur-Kompen sation
Gold		10^{-1}	± 5%	
Silber		10^{-2}	±10%	Bauart mit hoher Dielektrizitätskonstanter

TUNER UNIT/(TUNER-EINHEIT)


TUNER UNIT
AERIAL IN
TP1
TP2
TP3
TP4
TP5
TR1 3SK103
TR3 2SC2734
TR4 3SK104
TR5 3SK104
TR6 2SC2736
D1 IT32
D2 IT32
D3 IT32
D4 IT33
D5 IT33
D6 IT33
D7 IT33
D8 IT33
D9 IT33
D10 IT33
D11 1SV146
D12 IT32
D13 1SS110
D14 1SS110
D15 1SS110
D16 1SS110
D17 1SS110
D18 1SS110
D19 1SS110
D20 1SS99
D21 HZ9AL
D22(1/2) 1S2835
D23(1/2) 1S2837
D24 IT33
D25 1SS110
IFT
L14
IF
To MAIN (AUDIO/REAR JACK)
TU
BU
BH
BL
AGC
AFC
C111~C117 0.001 X 7
C111
C112
C113
C114
C115
C116
C117
To MAIN (AUDIO/REAR JACK)

SCHEMATIC DIAGRAM	PAGE
TUNER UNIT	5-2
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TIMER/OPERATION SWITCH -VT-110E-	5-11
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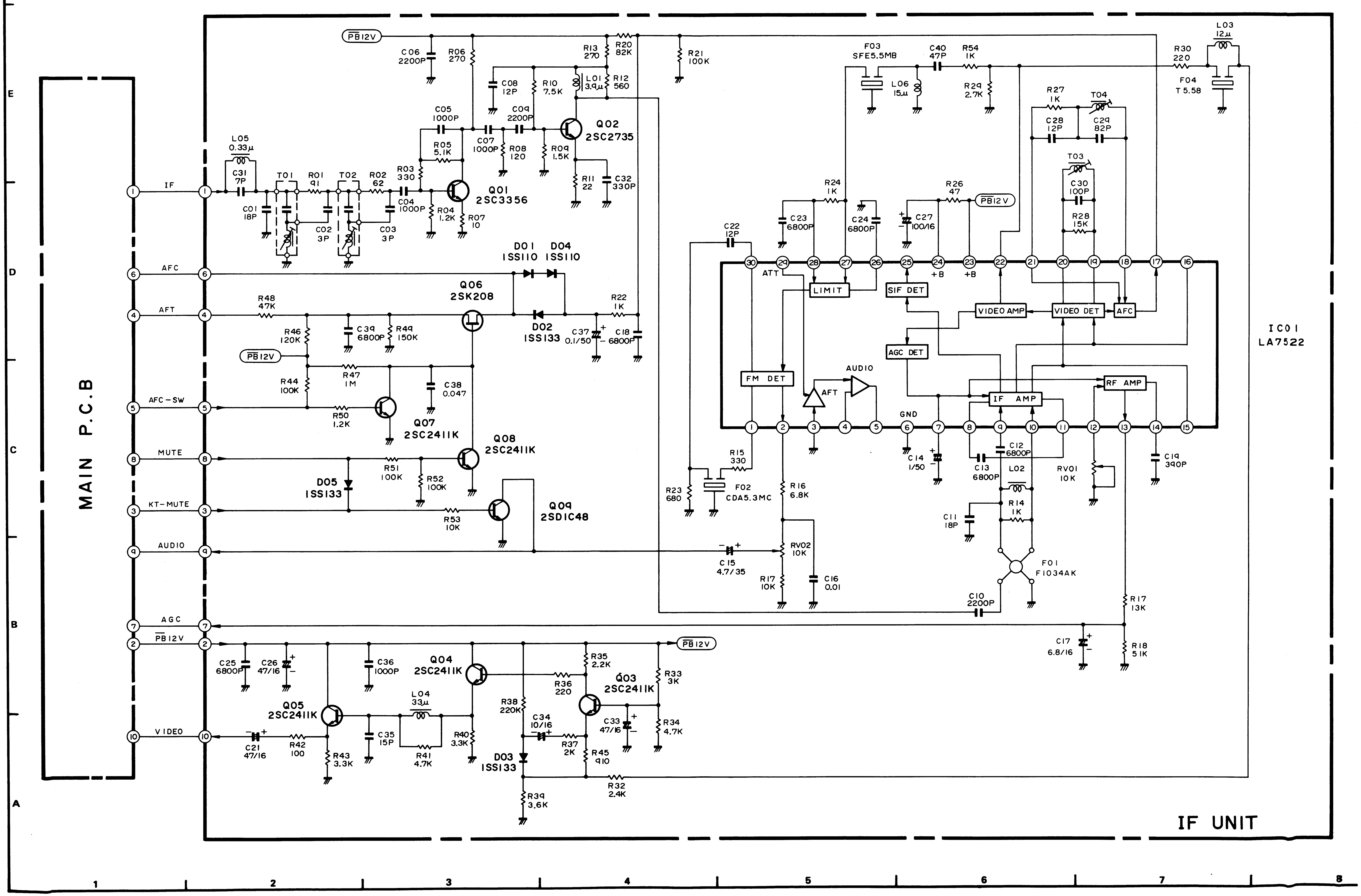
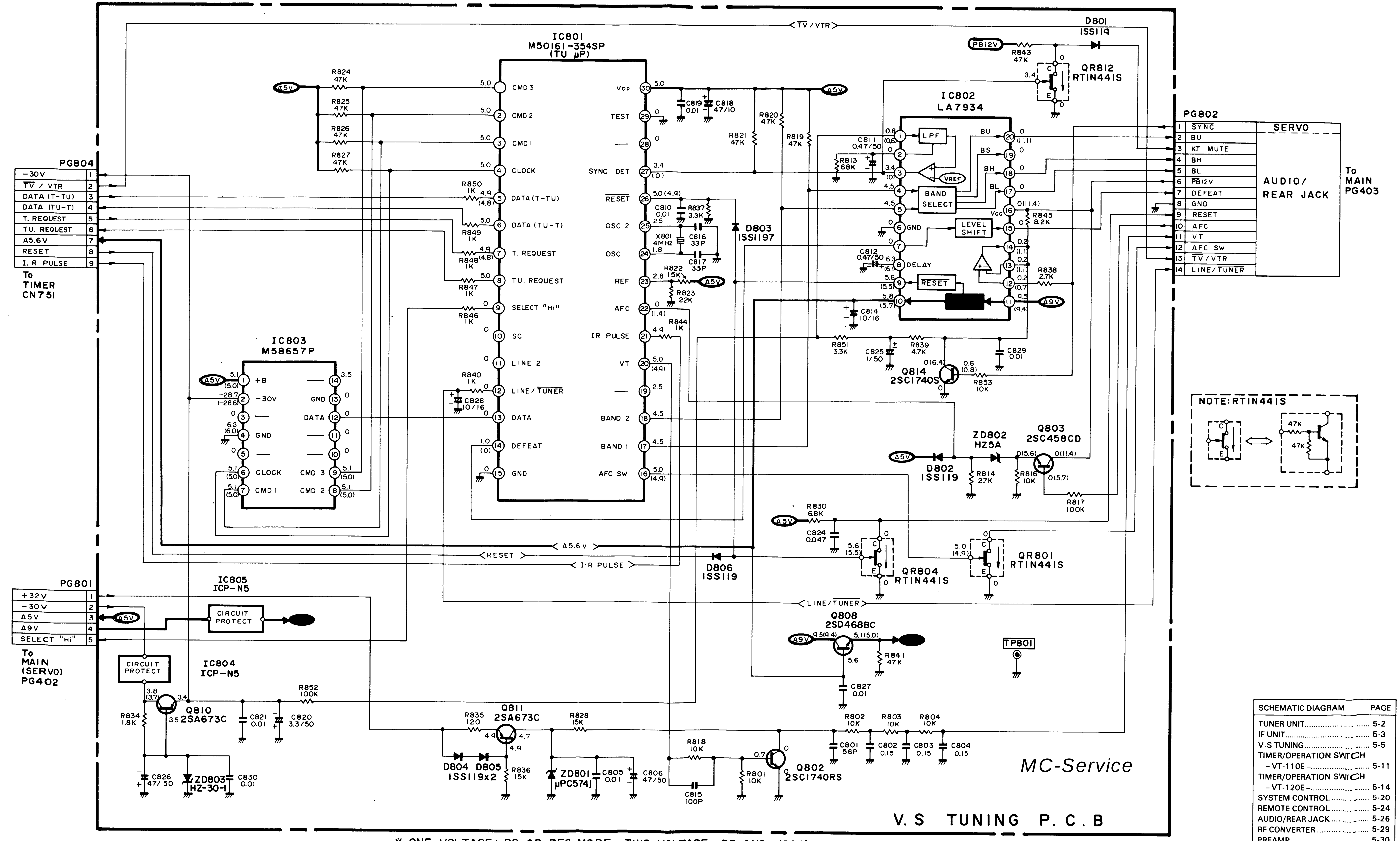
PREAMP	5-30
SERVO	5-39
Y/CHROMA	5-42
REGULATOR	5-51
INTERNAL WIRING DIAGRAM	5-55

IF UNIT (ZF-EINHEIT)


MAIN P.C.B
IF UNIT
IF
AFC
AFT
AFC-SW
MUTE
KT-MUTE
AUDIO
AGC
PB12V
VIDEO
L05 0.33μ
C31 7P
C01 18P
T01
R01 91
T02
R02 62
C02 3P
C03 3P
R03 330
C04 1000P
R04 1.2K
R07 10
C05 1000P
R05 5.1K
Q01 2SC3356
C06 2200P
R06 270
C07 1000P
R08 120
C08 12P
R10 7.5K
C09 2200P
R09 1.5K
Q02 2SC2735
R11 22
C32 330P
R13 270
R20 82K
L01 3.9μ
R12 560
R21 100K
D01 1SS110
D04 1SS110
Q06 2SK208
R48 47K
R46 120K
C39 6800P
R49 150K
D02 1SS133
R22 1K
C37 0.1/50
C18 6800P
R47 1M
R44 100K
C38 0.047
R50 1.2K
Q07 2SC2411K
Q08 2SC2411K
R51 100K
R52 100K
D05 1SS133
R53 10K
Q09 2SD1C48
F03 SFE5.5MB
L06 15μ
C40 47P
R54 1K
R29 2.7K
R30 220
L03 12μ
F04 T5.58
R27 1K
T04
C28 12P
C29 82P
T03
C30 100P
R28 15K
R24 1K
R26 47
C23 6800P
C24 6800P
C27 100/16
C22 12P
ATT
LIMIT
SIF DET
+B
VIDEO AMP
VIDEO DET
AFC
AGC DET
FM DET
AUDIO
AFT
GND
IF AMP
RF AMP
IC01 LA7522
R15 330
R23 680
F02 CDA5.3MC
R16 6.8K
C14 1/50
C13 6800P
C12 6800P
L02
C11 18P
R14 1K
RV01 10K
C19 390P
C15 4.7/35
RV02 10K
R17 10K
C16 0.01
F01 F1034AK
C10 2200P
R17 13K
C17 6.8/16
R18 5.1K
C25 6800P
C26 47/16
C36 1000P
Q04 2SC2411K
R35 2.2K
R33 3K
R36 220
Q03 2SC2411K
Q05 2SC2411K
L04 33μ
R38 220K
C34 10/16
C33 47/16
R34 4.7K
C21 47/16
R42 100
C35 15P
R41 4.7K
R40 3.3K
R37 2K
R45 910
R43 3.3K
D03 1SS133
R32 2.4K
R39 3.6K
A
B
C
D
E
1
2
3
4
5
6
7
8

V·S TUNING (SPANNUNGSSYNTHESIZER-TUNER)


IC801
M50161-354SP
(TU µP)
CMD 3
CMD 2
CMD 1
CLOCK
DATA (T-TU)
DATA (TU-T)
T. REQUEST
TU. REQUEST
SELECT "Hi"
SC
LINE 2
LINE/TUNER
DATA
DEFEAT
GND
VDD
TEST
SYNC DET
RESET
OSC 2
OSC 1
REF
AFC
IR PULSE
VT
BAND 2
BAND 1
AFC SW
IC802
LA7934
LPF
VREF
BAND SELECT
LEVEL SHIFT
DELAY
RESET
BU
BS
BH
BL
Vcc
IC803
M58657P
+B
-30V
GND
DATA
CLOCK
CMD 1
CMD 3
CMD 2
IC805
ICP-N5
CIRCUIT PROTECT
IC804
ICP-N5
CIRCUIT PROTECT
PG804
-30V
TV / VTR
DATA (T-TU)
DATA (TU-T)
T. REQUEST
TU. REQUEST
A5.6V
RESET
I. R PULSE
To TIMER CN751
PG801
+32V
-30V
A5V
A9V
SELECT "Hi"
To MAIN (SERVO) PG402
PG802
SYNC
BU
KT MUTE
BH
BL
PB12V
DEFEAT
GND
RESET
AFC
VT
AFC SW
TV/VTR
LINE/TUNER
SERVO
AUDIO/ REAR JACK
To MAIN PG403
D801 ISS119
QR812 RTIN441S
D803 ISS197
X801 4MHz
Q814 2SC1740S
ZD802 HZ5A
Q803 2SC458CD
D802 ISS119
QR804 RTIN441S
QR801 RTIN441S
D806 ISS119
Q808 2SD468BC
TP801
Q810 2SA673C
Q811 2SA673C
D804 D805 ISS119x2
ZD803 HZ-30-1
ZD801 µPC574J
Q802 2SC1740RS
A5V
A9V
PB12V
A5.6V
RESET
I·R PULSE
LINE/TUNER
TV / VTR
NOTE:RTIN441S
47K
47K
V. S TUNING P. C. B
E
D
C
B
A
1
2
3
4
5
6
7
8

※ ONE VOLTAGE: PB OR REC MODE, TWO VOLTAGE: PB AND (REC) MODES.

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PREAMP	5-30
SERVO	5-39
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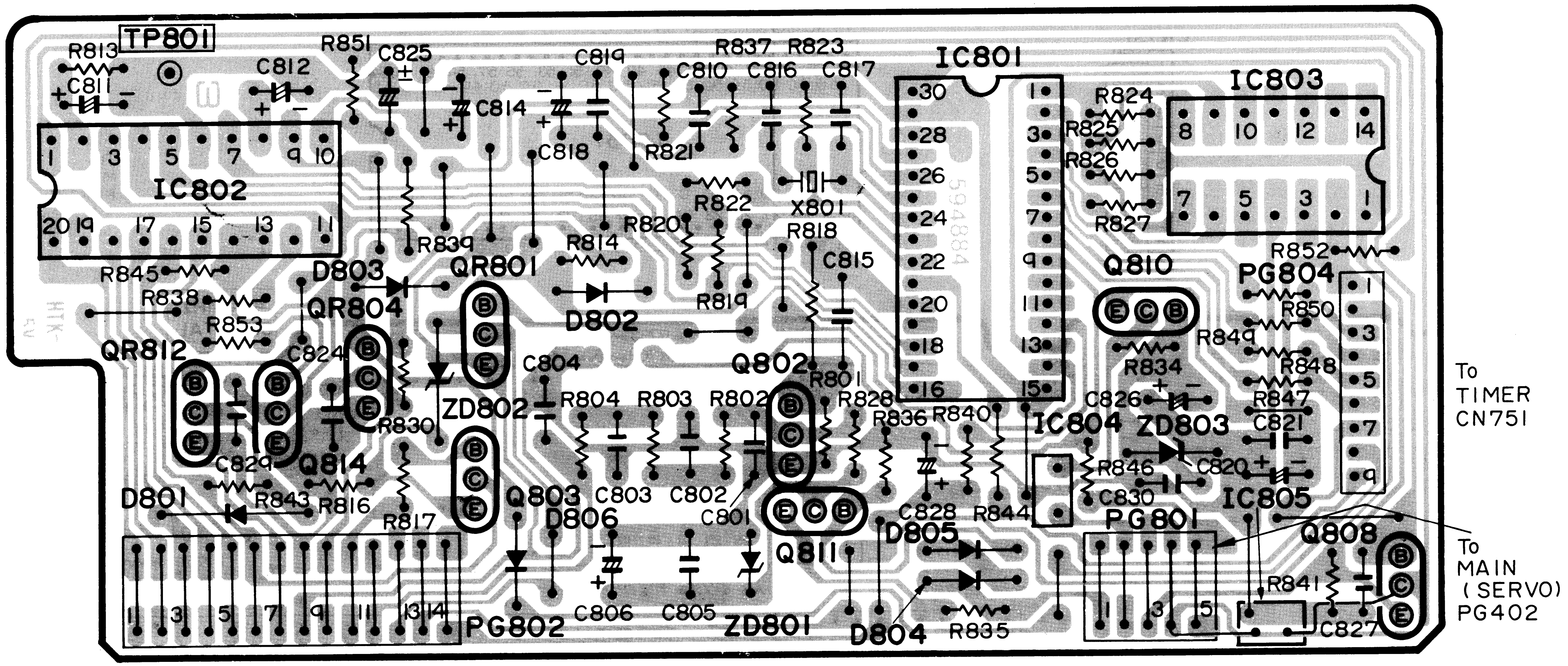
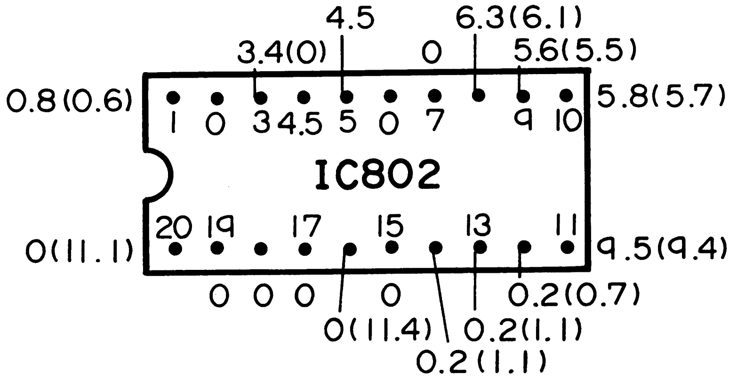
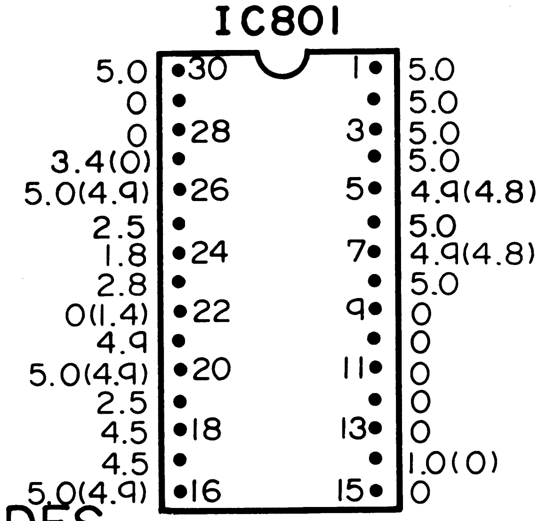
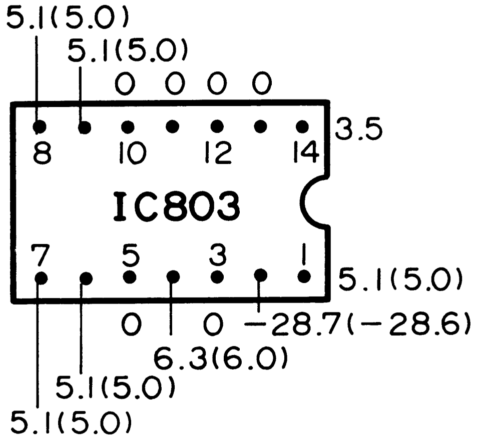
REGULATOR	5-51
INTERNAL WIRING DIAGRAM	5-55


TP801
R813
C811
C812
R851
C825
C819
R837
R823
C810
C816
C817
C814
C818
R821
R822
X801
R820
R818
C815
R814
R819
IC802
IC801
IC803
R824
R825
R826
R827
R839
R845
R838
R853
D803
QR801
QR804
D802
QR812
C824
C804
ZD802
R830
R804
R803
R802
Q802
R801
R828
R836
R840
IC804
ZD803
C826
R834
R849
R850
R848
R847
C821
R846
C820
C830
R852
PG804
Q810
C829
Q814
R843
R816
R817
D801
Q803
D806
C803
C802
C801
C828
R844
D805
IC805
PG801
Q808
R841
C827
C806
C805
ZD801
Q811
D804
R835
PG802
To TIMER CN751
To MAIN (SERVO) PG402
To MAIN PG403

V.S TUNING P.C.B

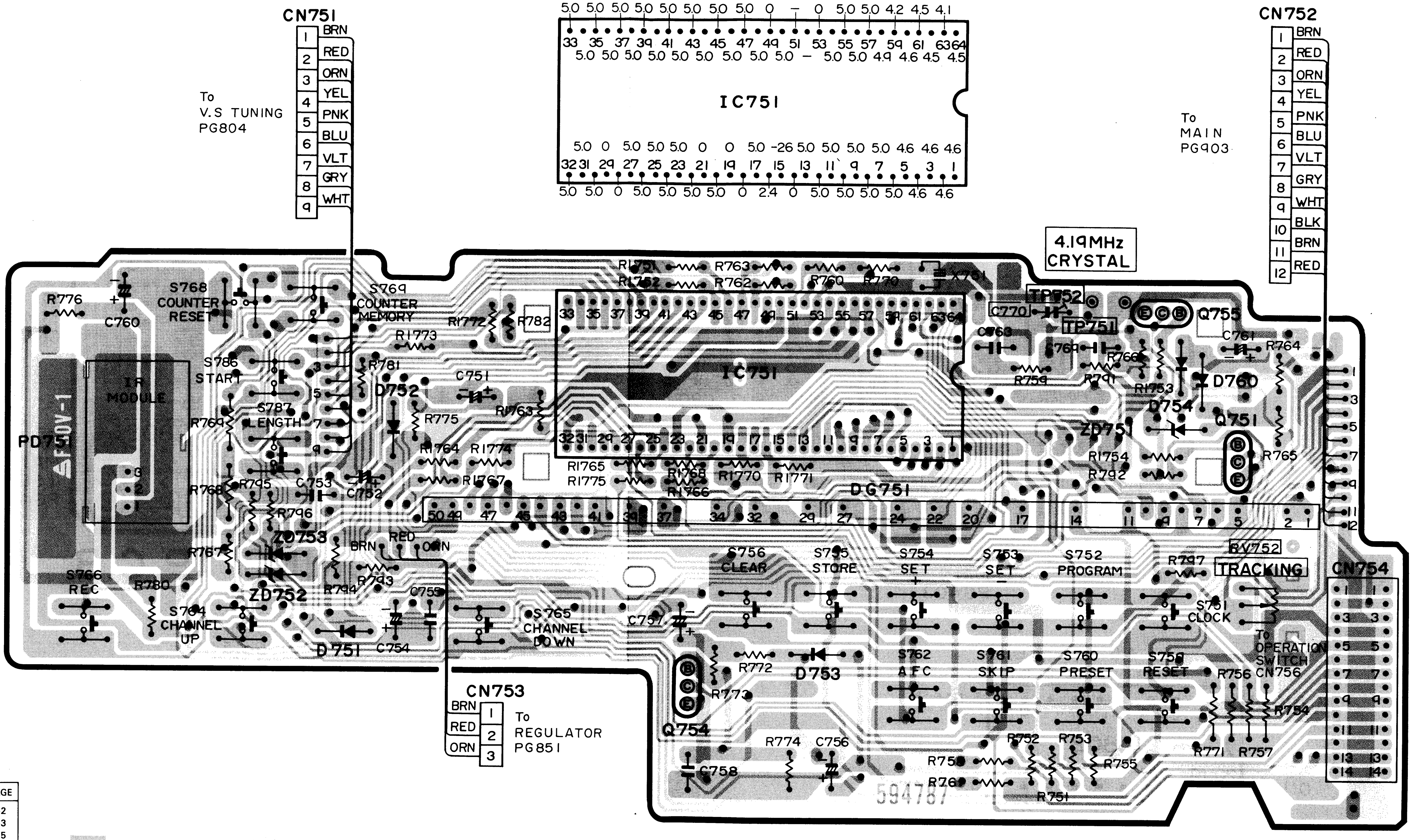

IC802
0.8(0.6)
3.4(0)
4.5
0
6.3(6.1)
5.6(5.5)
5.8(5.7)
1 0 3 4.5 5 0 7 9 10
20 19 17 15 13 11
0(11.1)
9.5(9.4)
0 0 0
0
0(11.4)
0.2(1.1)
0.2(1.1)
0.2(0.7)


IC801
5.0 30
0
0 28
3.4(0)
5.0(4.9) 26
2.5
1.8 24
2.8
0(1.4) 22
4.9
5.0(4.9) 20
2.5
4.5 18
4.5
5.0(4.9) 16
1 5.0
5.0
3 5.0
5.0
5 4.9(4.8)
5.0
7 4.9(4.8)
5.0
9 0
0
11 0
0
13 0
1.0(0)
15 0


IC803
5.1(5.0)
5.1(5.0)
0 0 0 0
8 10 12 14
3.5
7 5 3 1
5.1(5.0)
0
0
-28.7(-28.6)
6.3(6.0)
5.1(5.0)
5.1(5.0)

※ ONE VOLTAGE : PB OR REC MODE,
TWO VOLTAGES : PB AND (REC) MODES.

TIMER –VT-110E–


CN751
BRN
RED
ORN
YEL
PNK
BLU
VLT
GRY
WHT
1
2
3
4
5
6
7
8
9
To
V.S TUNING
PG804
5.0 5.0 5.0 5.0 5.0 5.0 5.0 5.0 0 – 0 5.0 5.0 4.2 4.5 4.1
33 35 37 39 41 43 45 47 49 51 53 55 57 59 61 6364
5.0 5.0 5.0 5.0 5.0 5.0 5.0 5.0 5.0 – 5.0 5.0 4.9 4.6 4.5 4.5
IC751
5.0 0 5.0 5.0 5.0 0 0 5.0 -26 5.0 5.0 5.0 5.0 4.6 4.6 4.6
32 31 29 27 25 23 21 19 17 15 13 11 9 7 5 3 1
5.0 5.0 0 5.0 5.0 5.0 5.0 0 2.4 0 5.0 5.0 5.0 5.0 4.6 4.6
CN752
BRN
RED
ORN
YEL
PNK
BLU
VLT
GRY
WHT
BLK
BRN
RED
10
11
12
To
MAIN
PG903
4.19MHz
CRYSTAL
R776
C760
S768
COUNTER
RESET
S769
COUNTER
MEMORY
R1772
R782
R1773
R1751
R1752
R763
R762
R760
R770
X761
TP752
C770
TP751
C763
C769
R766
R759
R791
R1753
C761
R764
Q755
D760
D754
Q751
ZD751
R1754
R792
R765
S786
START
R781
D752
C751
R1763
R775
S787
LENGTH
R769
IR
MODULE
PD751
R1764
R1774
R1767
R1765
R1775
R1768
R1770
R1771
R1766
DG751
R768
R795
C753
C752
R796
ZD753
R767
ZD752
BRN
RED
ORN
R793
R794
C755
S766
REC
R780
S764
CHANNEL
UP
D751
C754
S765
CHANNEL
DOWN
C757
S756
CLEAR
S755
STORE
S754
SET
+
S753
SET
–
S752
PROGRAM
R797
RV752
TRACKING
CN754
S751
CLOCK
To
OPERATION
SWITCH
CN756
R772
D753
R773
Q754
S762
AFC
S761
SKIP
S760
PRESET
S759
RESET
R756
R754
R774
C756
C758
R752
R753
R758
R761
R755
R751
R771
R757
594787
CN753
BRN
RED
ORN
To
REGULATOR
PG851
E
D
C
B
A
1
2
3
4
5
6
7
8

▨ Solderd side   ☐ Parts side   ● Through hole

TIMER P.C.B

※VOLTAGES : ARE AS MEASURED IN THE STOP MODE

MC-Service

SCHEMATIC DIAGRAM	PAGE
TUNER UNIT	5-2
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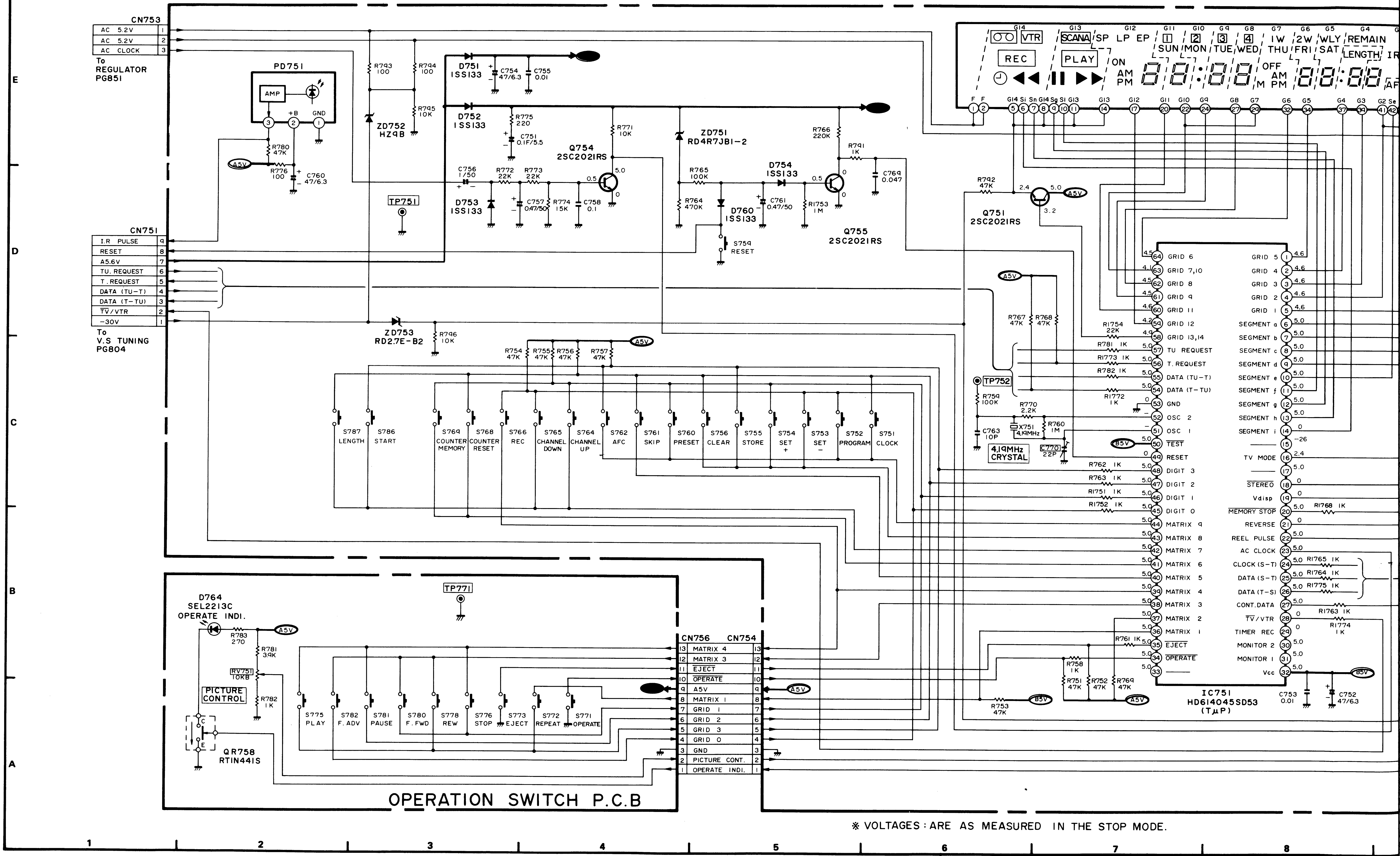
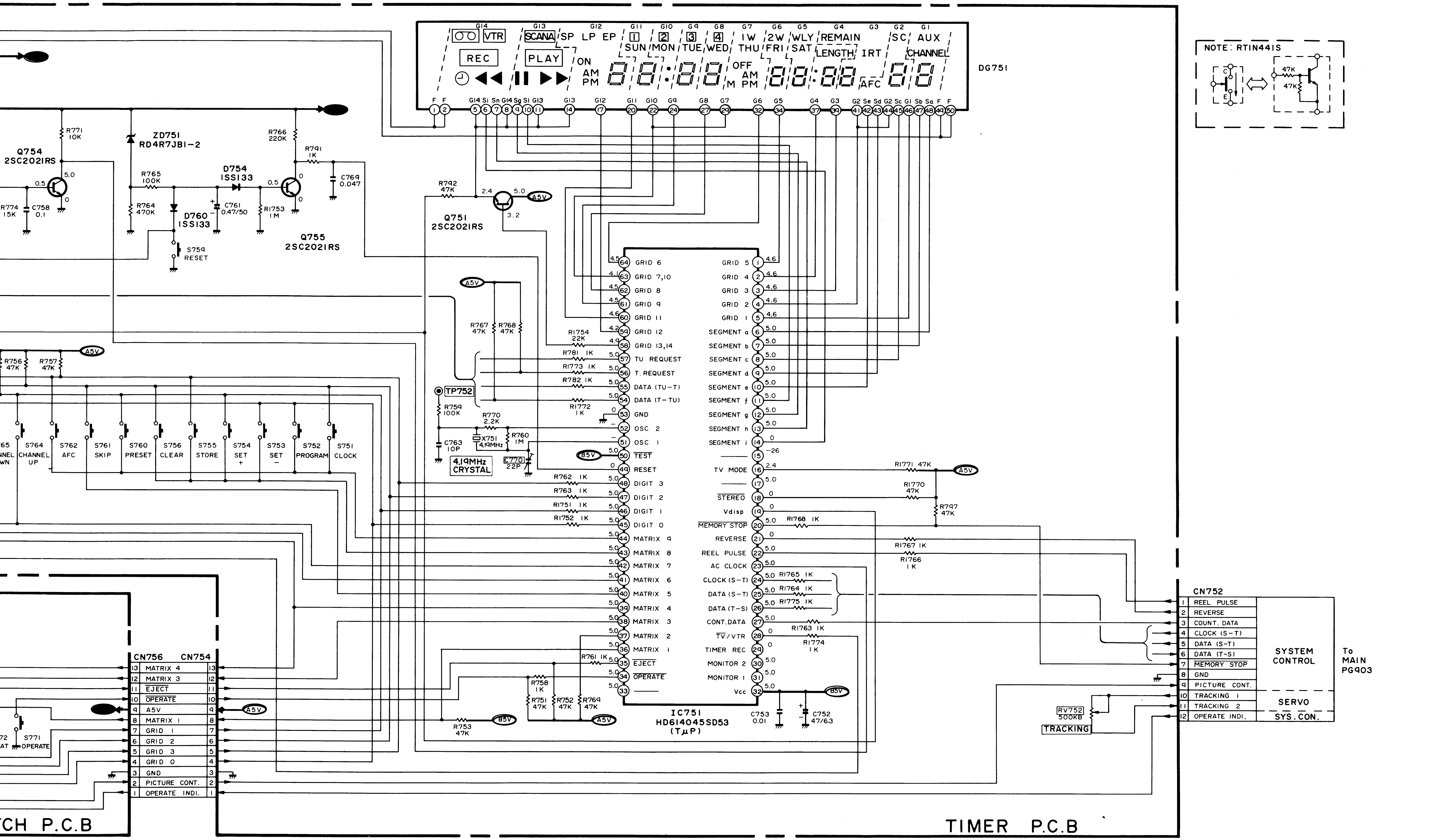
TIMER/OPERATION SWITCH (TIMER/FUNKTIONSSCHALTER)
-VT-110E-

MC-Service


CN753
AC 5.2V
AC 5.2V
AC CLOCK
To REGULATOR PG851
PD751
AMP
+B
GND
R780 47K
R776 100
C760 47/6.3
A5V
CN751
I.R PULSE
RESET
A5.6V
TU. REQUEST
T. REQUEST
DATA (TU-T)
DATA (T-TU)
TV/VTR
-30V
To V.S TUNING PG804
R793 100
R794 100
R795 10K
ZD752 HZ9B
D751 1SS133
C754 47/6.3
C755 0.01
D752 1SS133
R775 220
C751 0.1F/5.5
C756 1/50
R772 22K
R773 22K
D753 1SS133
C757 047/50
R774 15K
C758 0.1
Q754 2SC2021RS
R771 10K
TP751
ZD751 RD4R7JB1-2
R765 100K
R764 470K
D760 1SS133
D754 1SS133
C761 0.47/50
R1753 1M
R766 220K
R791 1K
C769 0.047
Q755 2SC2021RS
S759 RESET
R792 47K
Q751 2SC2021RS
ZD753 RD2.7E-B2
R796 10K
R754 47K
R755 47K
R756 47K
R757 47K
S787 LENGTH
S786 START
S769 COUNTER MEMORY
S768 COUNTER RESET
S766 REC
S765 CHANNEL DOWN
S764 CHANNEL UP
S762 AFC
S761 SKIP
S760 PRESET
S756 CLEAR
S755 STORE
S754 SET +
S753 SET -
S752 PROGRAM
S751 CLOCK
R767 47K
R768 47K
TP752
R759 100K
C763 10P
R770 2.2K
X751 4.19MHz
R760 1M
4.19MHz CRYSTAL
C770 22P
B5V
R1754 22K
R781 1K
R1773 1K
R782 1K
R1772 1K
R762 1K
R763 1K
R1751 1K
R1752 1K
R761 1K
R758 1K
R751 47K
R752 47K
R769 47K
R753 47K
GRID 6
GRID 7,10
GRID 8
GRID 9
GRID 11
GRID 12
GRID 13,14
TU REQUEST
T. REQUEST
DATA (TU-T)
DATA (T-TU)
GND
OSC 2
OSC 1
TEST
RESET
DIGIT 3
DIGIT 2
DIGIT 1
DIGIT 0
MATRIX 9
MATRIX 8
MATRIX 7
MATRIX 6
MATRIX 5
MATRIX 4
MATRIX 3
MATRIX 2
MATRIX 1
EJECT
OPERATE
GRID 5
GRID 4
GRID 3
GRID 2
GRID 1
SEGMENT a
SEGMENT b
SEGMENT c
SEGMENT d
SEGMENT e
SEGMENT f
SEGMENT g
SEGMENT h
SEGMENT i
TV MODE
STEREO
Vdisp
MEMORY STOP
REVERSE
REEL PULSE
AC CLOCK
CLOCK (S-T)
DATA (S-T)
DATA (T-S)
CONT.DATA
TV/VTR
TIMER REC
MONITOR 2
MONITOR 1
Vcc
R1768 1K
R1765 1K
R1764 1K
R1775 1K
R1763 1K
R1774 1K
IC751 HD614045SD53 (TμP)
C753 0.01
C752 47/6.3
VTR
REC
PLAY
SCANA
SP LP EP
SUN MON TUE WED THU FRI SAT
1W 2W WLY REMAIN
LENGTH
ON
OFF
AM PM
D764 SEL2213C OPERATE INDI.
R783 270
R781 3.9K
RV751 10KB
PICTURE CONTROL
R782 1K
QR758 RTIN441S
TP771
S775 PLAY
S782 F.ADV
S781 PAUSE
S780 F.FWD
S778 REW
S776 STOP
S773 EJECT
S772 REPEAT
S771 OPERATE
CN756
CN754
MATRIX 4
MATRIX 3
EJECT
OPERATE
A5V
MATRIX 1
GRID 1
GRID 2
GRID 3
GRID 0
GND
PICTURE CONT.
OPERATE INDI.
OPERATION SWITCH P.C.B
E
D
C
B
A
1
2
3
4
5
6
7
8

※ VOLTAGES : ARE AS MEASURED IN THE STOP MODE.

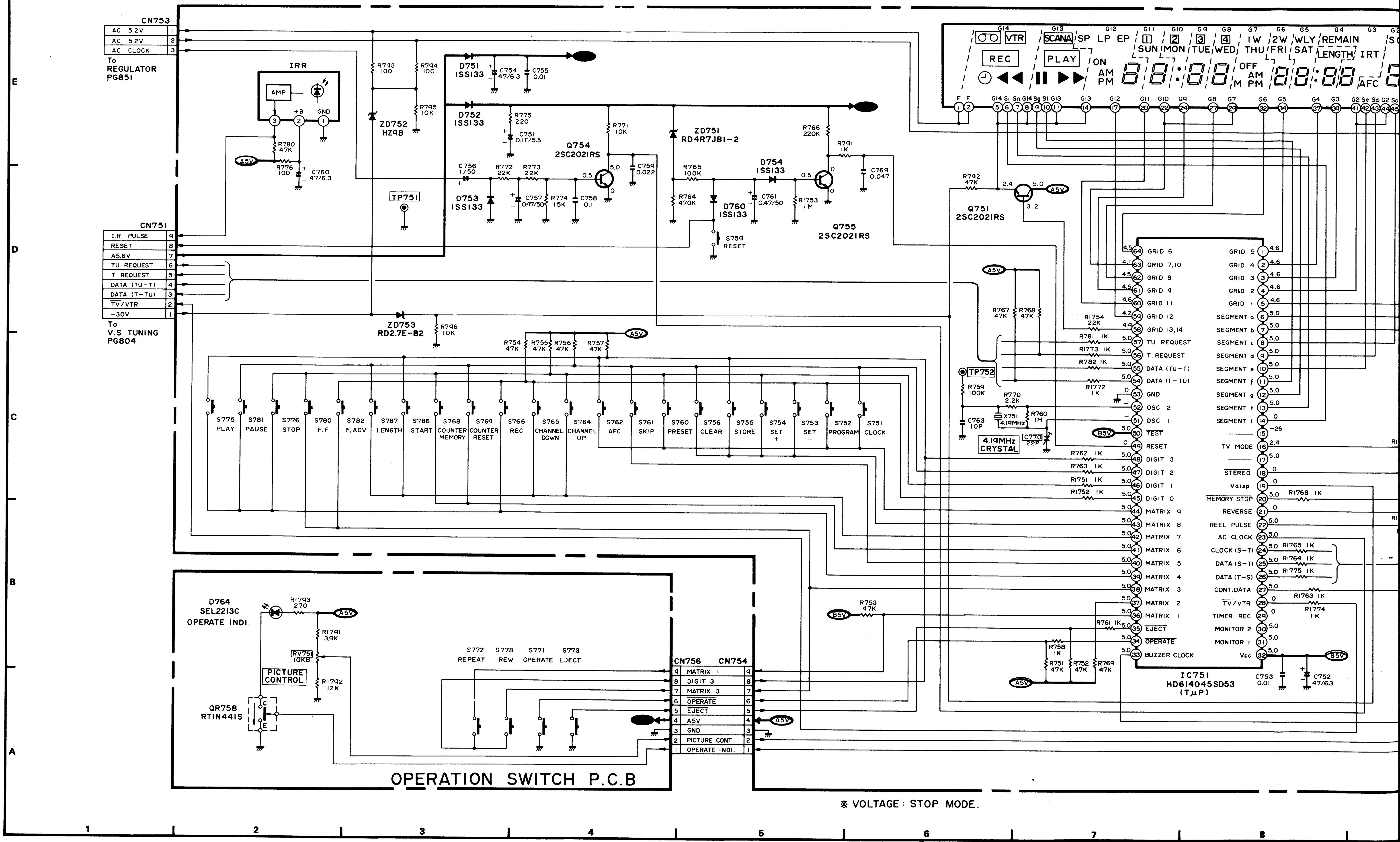
LTER)


DG751
G14 G13 G12 G11 G10 G9 G8 G7 G6 G5 G4 G3 G2 G1
VTR
SCANA SP LP EP
SUN MON TUE WED THU FRI SAT
1W 2W WLY REMAIN
SC AUX
LENGTH IRT
CHANNEL
REC
PLAY
ON AM PM
OFF AM PM
AFC
NOTE: RTIN441S
47K
47K
R771 10K
ZD751 RD4R7JB1-2
R766 220K
R791 1K
C769 0.047
Q754 2SC2021RS
R765 100K
D754 1SS133
R764 470K
D760 1SS133
C761 0.47/50
R1753 1M
Q755 2SC2021RS
R774 15K
C758 0.1
S759 RESET
R792 47K
Q751 2SC2021RS
A5V
B5V
R767 47K
R768 47K
R1754 22K
R781 1K
R1773 1K
R782 1K
R1772 1K
TP752
R759 100K
R770 2.2K
X751 4.19MHz
R760 1M
C763 10P
4.19MHz CRYSTAL
C770 22P
R762 1K
R763 1K
R1751 1K
R1752 1K
R756 47K
R757 47K
S764 CHANNEL UP
S762 AFC
S761 SKIP
S760 PRESET
S756 CLEAR
S755 STORE
S754 SET +
S753 SET −
S752 PROGRAM
S751 CLOCK
S771 OPERATE
IC751 HD614045SD53 (TμP)
GRID 6
GRID 7,10
GRID 8
GRID 9
GRID 11
GRID 12
GRID 13,14
TU REQUEST
T. REQUEST
DATA (TU−T)
DATA (T−TU)
GND
OSC 2
OSC 1
TEST
RESET
DIGIT 3
DIGIT 2
DIGIT 1
DIGIT 0
MATRIX 9
MATRIX 8
MATRIX 7
MATRIX 6
MATRIX 5
MATRIX 4
MATRIX 3
MATRIX 2
MATRIX 1
EJECT
OPERATE
GRID 5
GRID 4
GRID 3
GRID 2
GRID 1
SEGMENT a
SEGMENT b
SEGMENT c
SEGMENT d
SEGMENT e
SEGMENT f
SEGMENT g
SEGMENT h
SEGMENT i
TV MODE
STEREO
Vdisp
MEMORY STOP
REVERSE
REEL PULSE
AC CLOCK
CLOCK (S−T)
DATA (S−T)
DATA (T−S)
CONT. DATA
TV/VTR
TIMER REC
MONITOR 2
MONITOR 1
Vcc
R1771 47K
R1770 47K
R797 47K
R1768 1K
R1767 1K
R1766 1K
R1765 1K
R1764 1K
R1775 1K
R1763 1K
R1774 1K
R761 1K
R758 1K
R751 47K
R752 47K
R769 47K
R753 47K
C753 0.01
C752 47/6.3
CN756 CN754
MATRIX 4
MATRIX 3
EJECT
OPERATE
A5V
MATRIX 1
GRID 1
GRID 2
GRID 3
GRID 0
GND
PICTURE CONT.
OPERATE INDI.
CN752
REEL PULSE
REVERSE
COUNT. DATA
CLOCK (S−T)
DATA (S−T)
DATA (T−S)
MEMORY STOP
GND
PICTURE CONT.
TRACKING 1
TRACKING 2
OPERATE INDI.
SYSTEM CONTROL
SERVO
SYS. CON.
To MAIN PG903
RV752 500KB
TRACKING
CH P.C.B
TIMER P.C.B

※ VOLTAGES : ARE AS MEASURED IN THE STOP MODE.

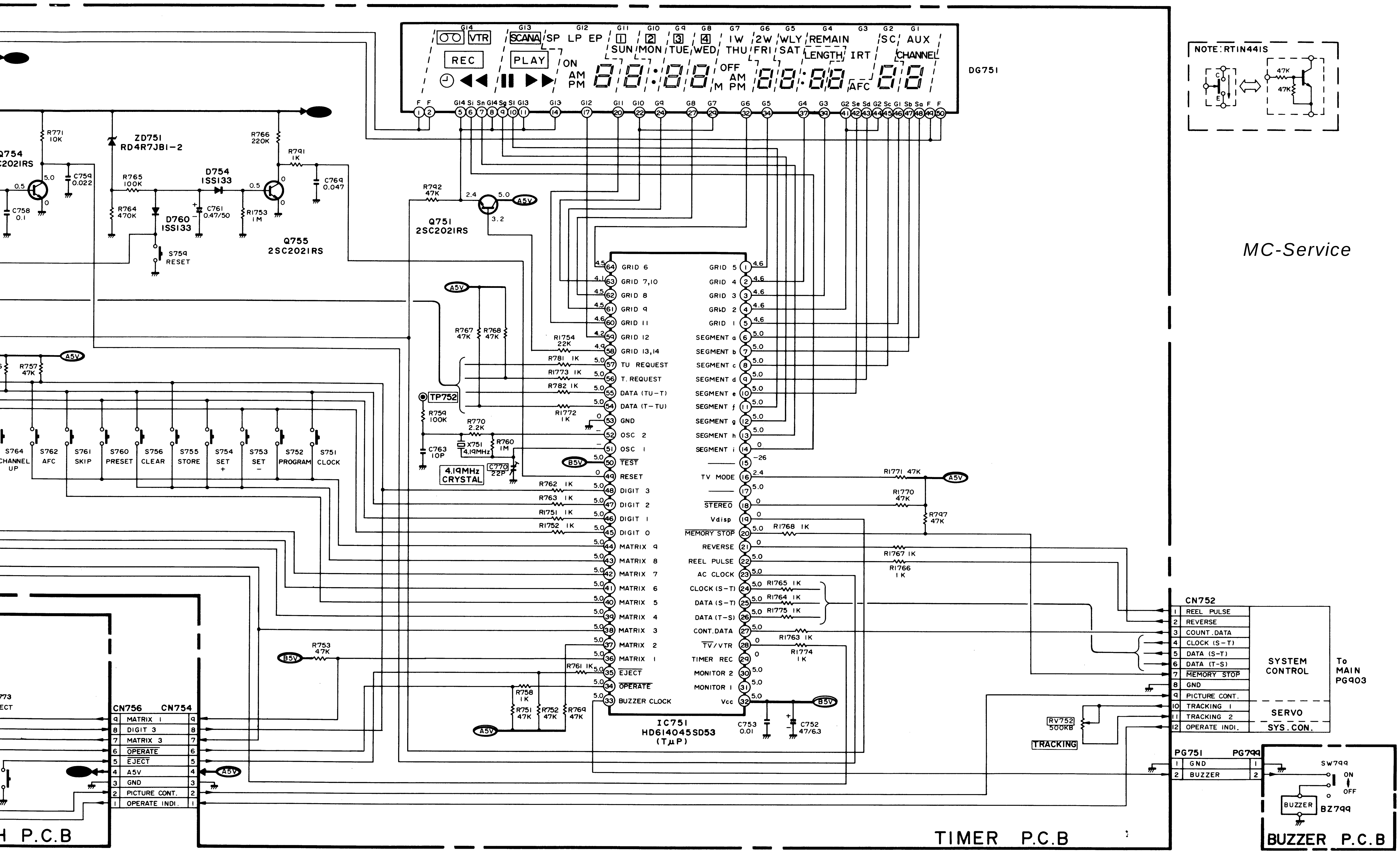
4 5 6 7 8 9 10 11

TIMER/OPERATION SWITCH (TIMER/FUNKTIONSSCHALTER)
– VT-120E –


CN753
AC 5.2V
AC 5.2V
AC CLOCK
To REGULATOR PG851
IRR
AMP
+B
GND
R780 47K
R776 100
C760 47/6.3
A5V
R793 100
R794 100
R795 10K
ZD752 HZ9B
TP751
D751 1SS133
C754 47/6.3
C755 0.01
D752 1SS133
R775 220
C751 0.1F/5.5
Q754 2SC2021RS
R771 10K
C759 0.022
C756 1/50
R772 22K
R773 22K
D753 1SS133
C757 0.47/50
R774 15K
C758 0.1
ZD751 RD4R7JB1-2
R765 100K
R764 470K
D760 1SS133
D754 1SS133
C761 0.47/50
R1753 1M
S759 RESET
R766 220K
R791 1K
C769 0.047
Q755 2SC2021RS
R792 47K
Q751 2SC2021RS
CN751
I.R PULSE
RESET
A5.6V
TU. REQUEST
T. REQUEST
DATA (TU-T)
DATA (T-TU)
TV/VTR
-30V
To V.S TUNING PG804
ZD753 RD2.7E-B2
R796 10K
R754 47K
R755 47K
R756 47K
R757 47K
S775 PLAY
S781 PAUSE
S776 STOP
S780 F.F
S782 F.ADV
S787 LENGTH
S786 START
S768 COUNTER MEMORY
S769 COUNTER RESET
S766 REC
S765 CHANNEL DOWN
S764 CHANNEL UP
S762 AFC
S761 SKIP
S760 PRESET
S756 CLEAR
S755 STORE
S754 SET +
S753 SET −
S752 PROGRAM
S751 CLOCK
G14 G13 G12 G11 G10 G9 G8 G7 G6 G5 G4 G3
VTR
SCAN
SP LP EP
SUN MON TUE WED THU FRI SAT
1W 2W WLY
REMAIN
LENGTH
IRT
REC
PLAY
ON
OFF
AM PM
AFC
TP752
R767 47K
R768 47K
R1754 22K
R781 1K
R1773 1K
R782 1K
R1772 1K
R759 100K
R770 2.2K
X751 4.19MHz
R760 1M
C763 10P
C770 22P
4.19MHz CRYSTAL
B5V
R762 1K
R763 1K
R1751 1K
R1752 1K
GRID 6
GRID 7,10
GRID 8
GRID 9
GRID 11
GRID 12
GRID 13,14
TU REQUEST
T. REQUEST
DATA (TU-T)
DATA (T-TU)
GND
OSC 2
OSC 1
TEST
RESET
DIGIT 3
DIGIT 2
DIGIT 1
DIGIT 0
MATRIX 9
MATRIX 8
MATRIX 7
MATRIX 6
MATRIX 5
MATRIX 4
MATRIX 3
MATRIX 2
MATRIX 1
EJECT
OPERATE
BUZZER CLOCK
GRID 5
GRID 4
GRID 3
GRID 2
GRID 1
SEGMENT a
SEGMENT b
SEGMENT c
SEGMENT d
SEGMENT e
SEGMENT f
SEGMENT g
SEGMENT h
SEGMENT i
TV MODE
STEREO
Vdisp
MEMORY STOP
REVERSE
REEL PULSE
AC CLOCK
CLOCK (S-T)
DATA (S-T)
DATA (T-S)
CONT.DATA
TV/VTR
TIMER REC
MONITOR 2
MONITOR 1
Vcc
R1768 1K
R1765 1K
R1764 1K
R1775 1K
R1763 1K
R1774 1K
IC751 HD614045SD53 (TμP)
C753 0.01
C752 47/6.3
R753 47K
R761 1K
R758 1K
R751 47K
R752 47K
R769 47K
D764 SEL2213C OPERATE INDI.
R1793 270
R1791 3.9K
RV751 10KB
PICTURE CONTROL
R1792 12K
QR758 RTIN441S
S772 REPEAT
S778 REW
S771 OPERATE
S773 EJECT
CN756
CN754
MATRIX 1
DIGIT 3
MATRIX 3
OPERATE
EJECT
A5V
GND
PICTURE CONT.
OPERATE INDI.
OPERATION SWITCH P.C.B
1 2 3 4 5 6 7 8
E D C B A

※ VOLTAGE : STOP MODE.

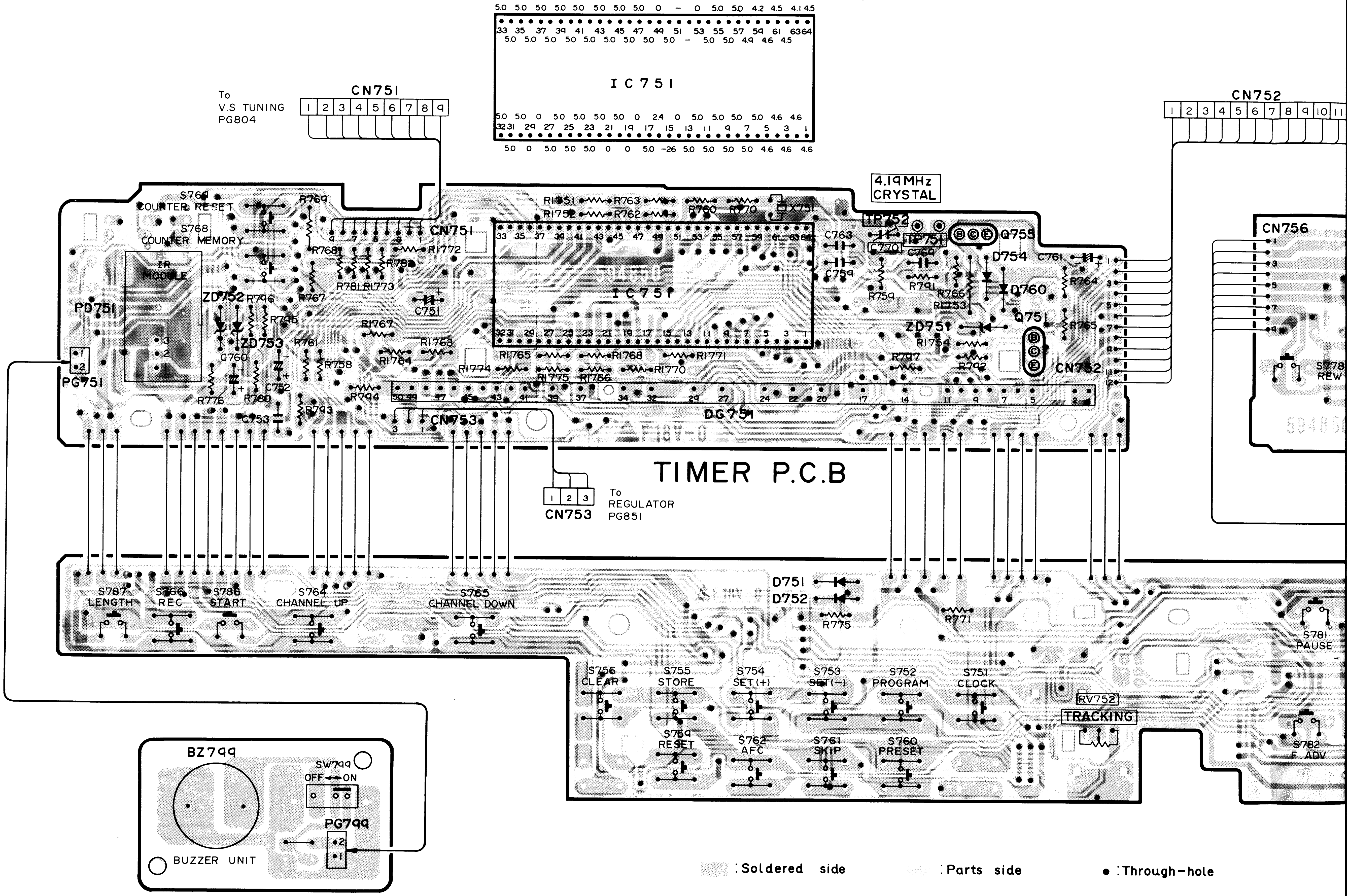
ER)



DG751
NOTE: RTIN441S
47K
47K
C
E
G14 G13 G12 G11 G10 G9 G8 G7 G6 G5 G4 G3 G2 G1
VTR
SCANA
SP LP EP
SUN MON TUE WED THU FRI SAT
1W 2W WLY REMAIN
LENGTH IRT
SC AUX
CHANNEL
REC
PLAY
ON
AM
PM
OFF
AM
PM
M
AFC
R771 10K
ZD751 RD4R7JB1-2
R766 220K
R791 1K
Q754 2SC2021RS
C759 0.022
C758 0.1
R765 100K
D754 1SS133
C769 0.047
R764 470K
D760 1SS133
C761 0.47/50
R1753 1M
Q755 2SC2021RS
S759 RESET
R792 47K
Q751 2SC2021RS
A5V
B5V
R767 47K
R768 47K
R1754 22K
R781 1K
R1773 1K
R782 1K
R1772 1K
TP752
R759 100K
R770 2.2K
X751 4.19MHz
R760 1M
C763 10P
4.19MHz CRYSTAL
C770 22P
R757 47K
S764 CHANNEL UP
S762 AFC
S761 SKIP
S760 PRESET
S756 CLEAR
S755 STORE
S754 SET +
S753 SET −
S752 PROGRAM
S751 CLOCK
R762 1K
R763 1K
R1751 1K
R1752 1K
GRID 6
GRID 7,10
GRID 8
GRID 9
GRID 11
GRID 12
GRID 13,14
TU REQUEST
T. REQUEST
DATA (TU−T)
DATA (T−TU)
GND
OSC 2
OSC 1
TEST
RESET
DIGIT 3
DIGIT 2
DIGIT 1
DIGIT 0
MATRIX 9
MATRIX 8
MATRIX 7
MATRIX 6
MATRIX 5
MATRIX 4
MATRIX 3
MATRIX 2
MATRIX 1
EJECT
OPERATE
BUZZER CLOCK
GRID 5
GRID 4
GRID 3
GRID 2
GRID 1
SEGMENT a
SEGMENT b
SEGMENT c
SEGMENT d
SEGMENT e
SEGMENT f
SEGMENT g
SEGMENT h
SEGMENT i
TV MODE
STEREO
Vdisp
MEMORY STOP
REVERSE
REEL PULSE
AC CLOCK
CLOCK (S−T)
DATA (S−T)
DATA (T−S)
CONT.DATA
TV/VTR
TIMER REC
MONITOR 2
MONITOR 1
Vcc
IC751 HD614045SD53 (TμP)
C753 0.01
C752 47/6.3
R1771 47K
R1770 47K
R797 47K
R1768 1K
R1767 1K
R1766 1K
R1765 1K
R1764 1K
R1775 1K
R1763 1K
R1774 1K
R753 47K
R761 1K
R758 1K
R751 47K
R752 47K
R769 47K
CN752
REEL PULSE
REVERSE
COUNT.DATA
CLOCK (S−T)
DATA (S−T)
DATA (T−S)
MEMORY STOP
GND
PICTURE CONT.
TRACKING 1
TRACKING 2
OPERATE INDI.
SYSTEM CONTROL
SERVO
SYS.CON.
To MAIN PG903
RV752 500KB
TRACKING
PG751
PG799
GND
BUZZER
SW799
ON
OFF
BUZZER
BZ799
BUZZER P.C.B
CN756
CN754
MATRIX 1
DIGIT 3
MATRIX 3
OPERATE
EJECT
A5V
GND
PICTURE CONT.
OPERATE INDI.
773
ECT
H P.C.B
TIMER P.C.B

※ VOLTAGE : STOP MODE.

4 5 6 7 8 9 10 11


IC751
CN751
To V.S TUNING PG804
CN752
CN753
To REGULATOR PG851
CN756
4.19MHz CRYSTAL
S769 COUNTER RESET
S768 COUNTER MEMORY
IR MODULE
PD751
PG751
DG751
TIMER P.C.B
S787 LENGTH
S766 REC
S786 START
S764 CHANNEL UP
S765 CHANNEL DOWN
D751
D752
S756 CLEAR
S755 STORE
S754 SET (+)
S753 SET (−)
S752 PROGRAM
S751 CLOCK
S759 RESET
S762 AFC
S761 SKIP
S760 PRESET
RV752 TRACKING
S778 REW
S781 PAUSE
S782 F. ADV
BZ799
SW799 OFF ↔ ON
PG799
BUZZER UNIT
▨ :Soldered side
▨ :Parts side
● :Through-hole

BUZZER P.C.B

※ VOLTAGE : STOP MODE.

SCHEMATIC DIAGRAM	PAGE
TUNER UNIT	5-2
IF UNIT	5-3
V·S TUNING	5-5
TIMER/OPERATION SWITCH – VT-110E –	5-11
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RF CONVERTER	5-29
PREAMP	5-30
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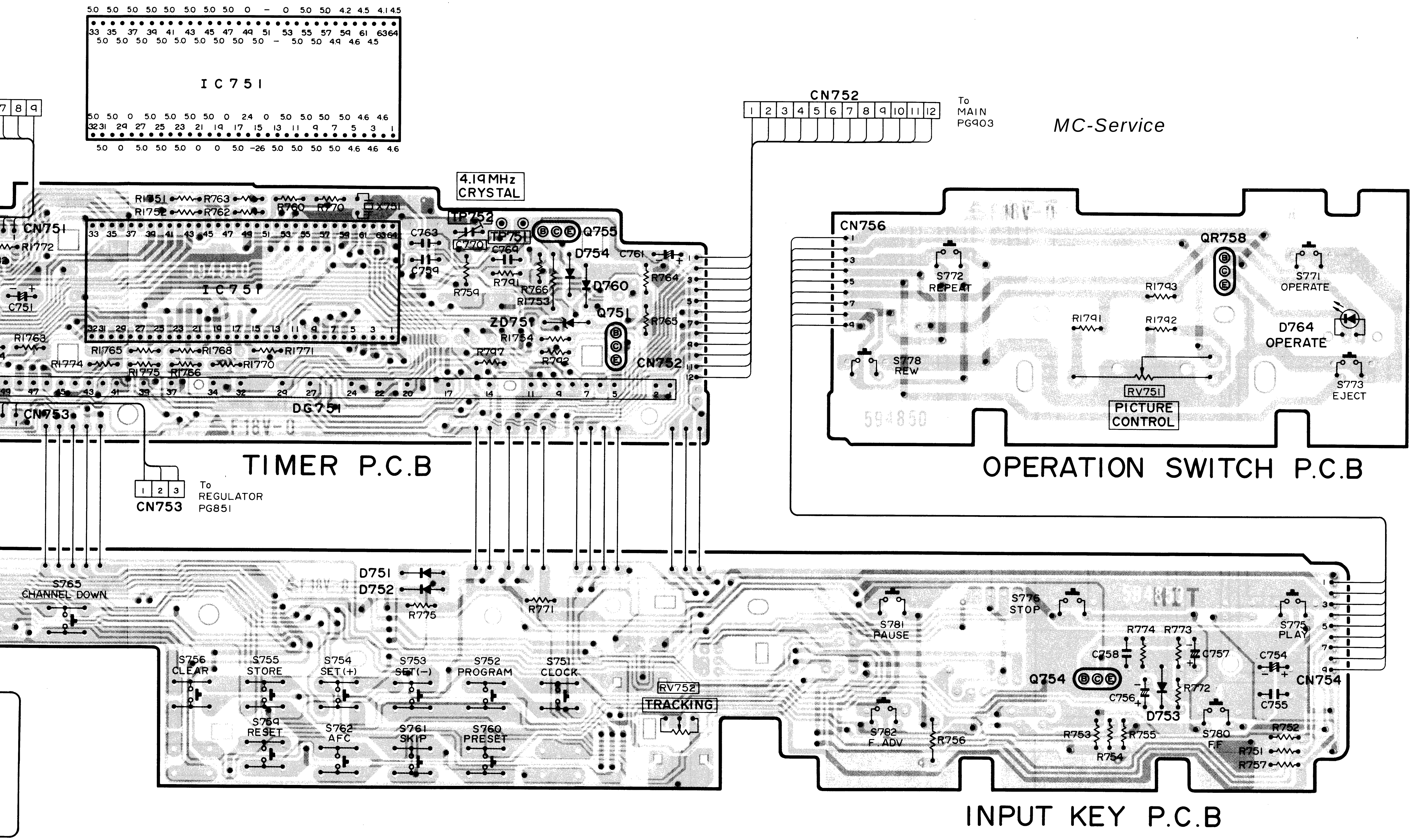
INTERNAL WIRING DIAGRAM	5-55

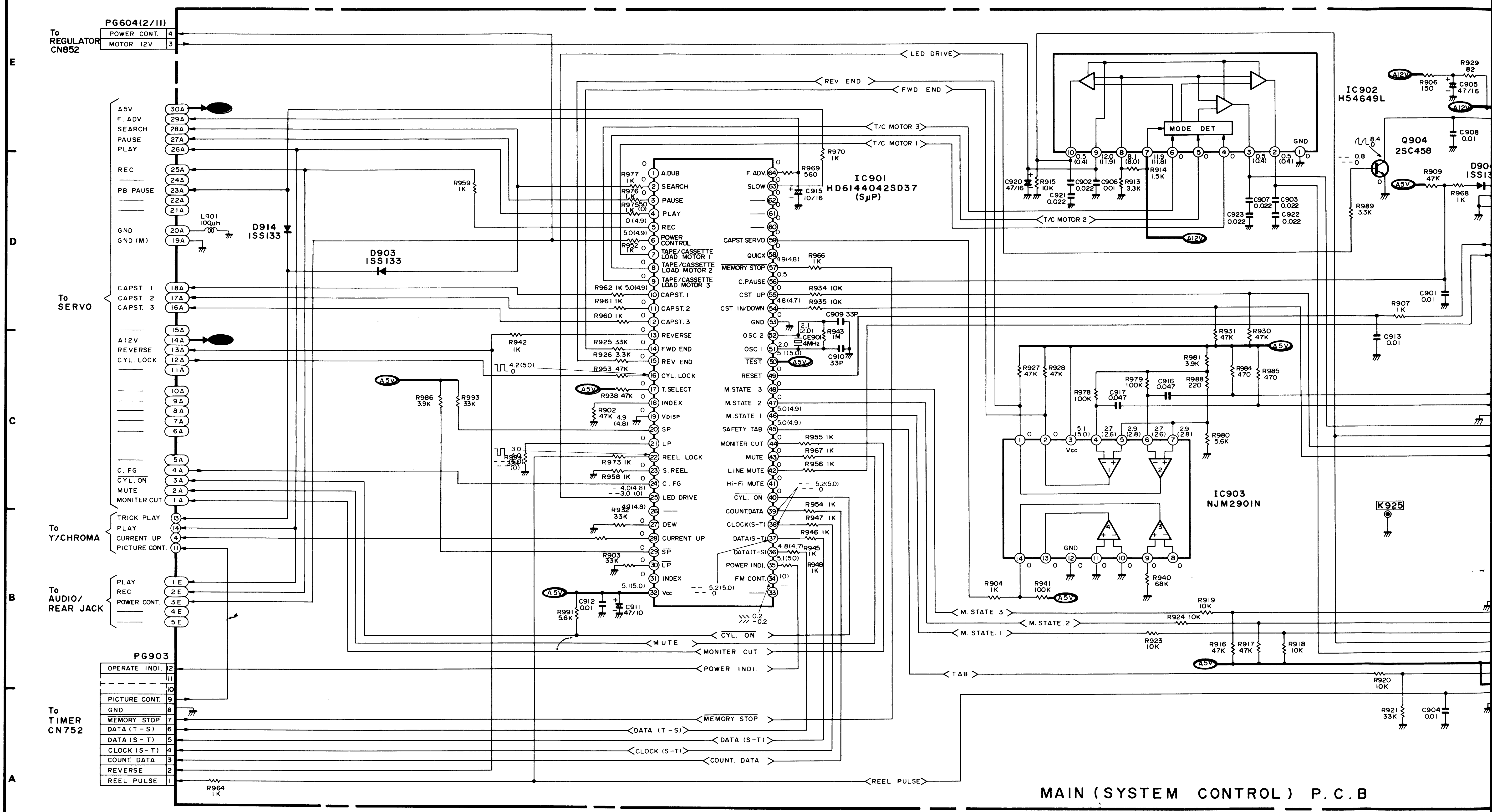


IC751
5.0 5.0 5.0 5.0 5.0 5.0 5.0 5.0 0 – 0 5.0 5.0 4.2 4.5 4.1 4.5
33 35 37 39 41 43 45 47 49 51 53 55 57 59 61 63 64
5.0 5.0 5.0 5.0 5.0 5.0 5.0 5.0 5.0 – 5.0 5.0 4.9 4.6 4.5
5.0 5.0 0 5.0 5.0 5.0 5.0 0 2.4 0 5.0 5.0 5.0 5.0 4.6 4.6
32 31 29 27 25 23 21 19 17 15 13 11 9 7 5 3 1
5.0 0 5.0 5.0 5.0 0 0 5.0 -26 5.0 5.0 5.0 5.0 4.6 4.6 4.6
CN752
1 2 3 4 5 6 7 8 9 10 11 12
To MAIN PG903
4.19MHz CRYSTAL
R1751 R1752 R763 R762 R760 R770 X751
CN751 R1772 C751 R1763 R1765 R1768 R1771 R1774 R1775 R1766 R1770
TP752 C770 TP751 C763 C759 C769 R759 R791 R766 R1753 Q755 D754 D760 C761 R764 R765
ZD751 R1754 R797 R792 Q751 CN752
DG751
CN753
TIMER P.C.B
1 2 3
CN753
To REGULATOR PG851
CN756
QR758
S772 REPEAT
S771 OPERATE
R1793 R1791 R1792
D764 OPERATE
S778 REW
S773 EJECT
RV751
PICTURE CONTROL
OPERATION SWITCH P.C.B
S765 CHANNEL DOWN
D751 D752 R775 R771
S756 CLEAR
S755 STORE
S754 SET(+)
S753 SET(−)
S752 PROGRAM
S751 CLOCK
S769 RESET
S762 AFC
S761 SKIP
S760 PRESET
RV752 TRACKING
S781 PAUSE
S776 STOP
S775 PLAY
R774 R773 C758 C757 C754 C755
Q754
C756 D753 R772
S782 F.ADV R756
R753 R755 R754
S780 FF
R752 R751 R757
CN754
INPUT KEY P.C.B

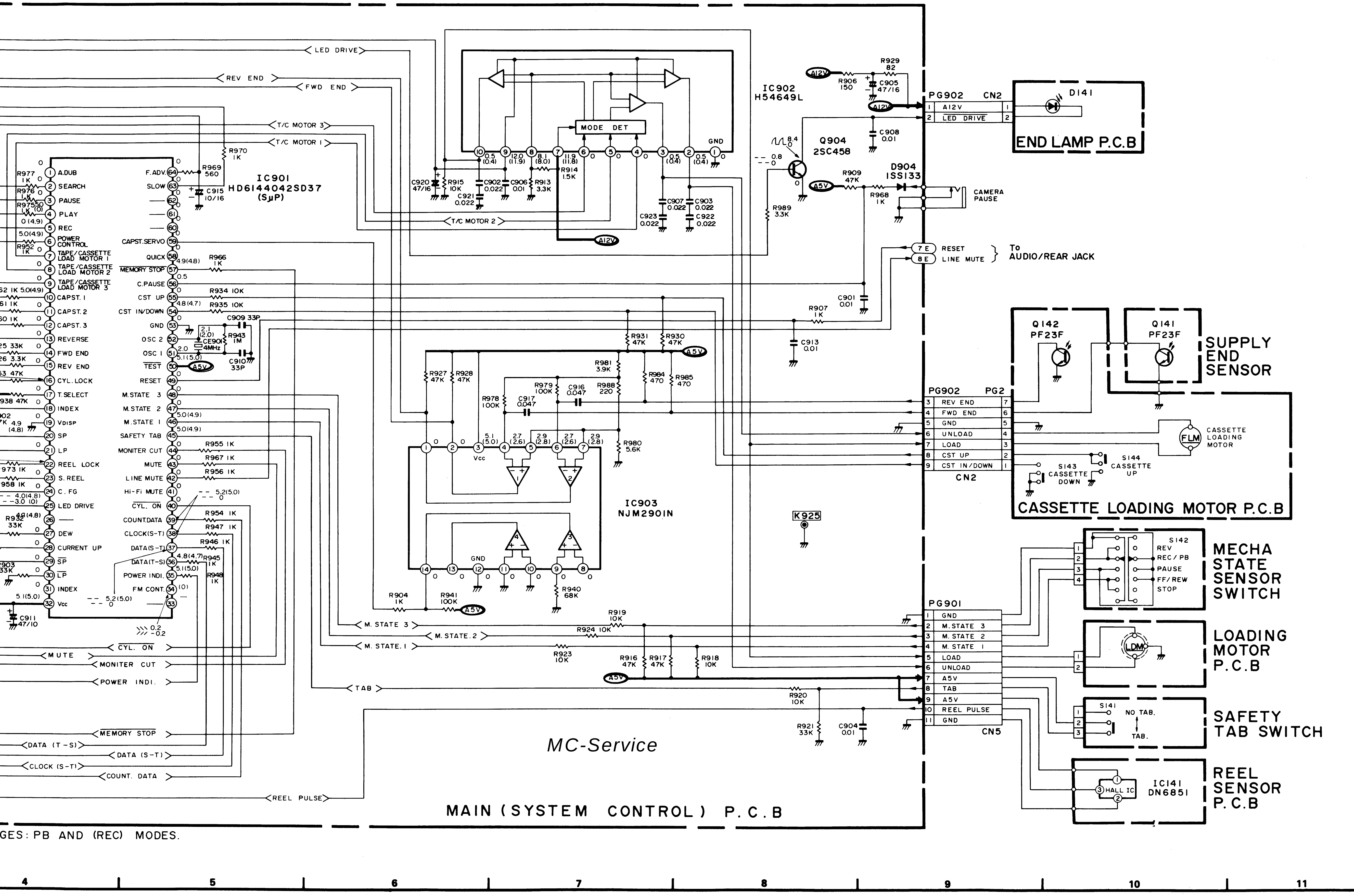
▨ : Soldered side ░ : Parts side ● : Through-hole

※ VOLTAGE : STOP MODE.

SYSTEM CONTROL (SYSTEMREGELUNG)


PG604(2/11)
To REGULATOR CN852
POWER CONT. 4
MOTOR 12V 3
To SERVO
A5V 30A
F. ADV 29A
SEARCH 28A
PAUSE 27A
PLAY 26A
REC 25A
PB PAUSE 23A
GND 20A
GND (M) 19A
CAPST. 1 18A
CAPST. 2 17A
CAPST. 3 16A
A12V 14A
REVERSE 13A
CYL. LOCK 12A
C. FG 4A
CYL. ON 3A
MUTE 2A
MONITER CUT 1A
To Y/CHROMA
TRICK PLAY 13
PLAY 14
CURRENT UP 4
PICTURE CONT. 11
To AUDIO/REAR JACK
PLAY 1E
REC 2E
POWER CONT. 3E
PG903
To TIMER CN752
OPERATE INDI. 12
PICTURE CONT. 9
GND 8
MEMORY STOP 7
DATA (T-S) 6
DATA (S-T) 5
CLOCK (S-T) 4
COUNT. DATA 3
REVERSE 2
REEL PULSE 1
L901 100μH
D914 1SS133
D903 1SS133
IC901 HD6144042SD37 (SμP)
A.DUB
SEARCH
PAUSE
PLAY
REC
POWER CONTROL
TAPE/CASSETTE LOAD MOTOR 1
TAPE/CASSETTE LOAD MOTOR 2
TAPE/CASSETTE LOAD MOTOR 3
CAPST. 1
CAPST. 2
CAPST. 3
REVERSE
FWD END
REV END
CYL. LOCK
T. SELECT
INDEX
VDISP
SP
LP
REEL LOCK
S. REEL
C. FG
LED DRIVE
DEW
CURRENT UP
SP
LP
INDEX
Vcc
F. ADV.
SLOW
CAPST. SERVO
QUICK
MEMORY STOP
C. PAUSE
CST UP
CST IN/DOWN
GND
OSC 2
OSC 1
TEST
RESET
M. STATE 3
M. STATE 2
M. STATE 1
SAFETY TAB
MONITER CUT
MUTE
LINE MUTE
Hi-Fi MUTE
CYL. ON
COUNT. DATA
CLOCK(S-T)
DATA(S-T)
DATA(T-S)
POWER INDI.
FM CONT.
CE901 4MHz
LED DRIVE
REV END
FWD END
T/C MOTOR 3
T/C MOTOR 1
T/C MOTOR 2
IC902 H54649L
MODE DET
GND
Q904 2SC458
IC903 NJM2901N
K925
M. STATE 3
M. STATE 2
M. STATE 1
TAB
CYL. ON
MUTE
MONITER CUT
POWER INDI.
MEMORY STOP
DATA (T-S)
DATA (S-T)
CLOCK (S-T)
COUNT. DATA
REEL PULSE
A5V
A12V
MAIN (SYSTEM CONTROL) P.C.B
E
D
C
B
A

※ ONE VOLTAGE: PB OR REC MODE, TWO VOLTAGES: PB AND (REC) MODES.


MAIN (SYSTEM CONTROL) P.C.B
MC-Service
IC901
HD6144042SD37
(SμP)
IC902
H54649L
IC903
NJM2901N
MODE DET
Q904
2SC458
D904
1SS133
CAMERA PAUSE
RESET
LINE MUTE
To AUDIO/REAR JACK
LED DRIVE
REV END
FWD END
T/C MOTOR 3
T/C MOTOR 1
T/C MOTOR 2
A12V
A5V
K925
PG902
CN2
A12V
LED DRIVE
D141
END LAMP P.C.B
Q142
PF23F
Q141
PF23F
SUPPLY END SENSOR
PG902
PG2
REV END
FWD END
GND
UNLOAD
LOAD
CST UP
CST IN/DOWN
CN2
FLM
CASSETTE LOADING MOTOR
S143 CASSETTE DOWN
S144 CASSETTE UP
CASSETTE LOADING MOTOR P.C.B
S142
REV
REC/PB
PAUSE
FF/REW
STOP
MECHA STATE SENSOR SWITCH
PG901
GND
M.STATE 3
M.STATE 2
M.STATE 1
LOAD
UNLOAD
A5V
TAB
A5V
REEL PULSE
GND
CN5
LDM
LOADING MOTOR P.C.B
S141
NO TAB.
TAB.
SAFETY TAB SWITCH
IC141
DN6851
HALL IC
REEL SENSOR P.C.B
A.DUB
SEARCH
PAUSE
PLAY
REC
POWER CONTROL
TAPE/CASSETTE LOAD MOTOR 1
TAPE/CASSETTE LOAD MOTOR 2
TAPE/CASSETTE LOAD MOTOR 3
CAPST. 1
CAPST. 2
CAPST. 3
REVERSE
FWD END
REV END
CYL. LOCK
T. SELECT
INDEX
VDISP
SP
LP
REEL LOCK
S. REEL
C. FG
LED DRIVE
DEW
CURRENT UP
SP
LP
INDEX
Vcc
F. ADV.
SLOW
CAPST. SERVO
QUICK
MEMORY STOP
C. PAUSE
CST UP
CST IN/DOWN
GND
OSC 2
OSC 1
TEST
RESET
M. STATE 3
M. STATE 2
M. STATE 1
SAFETY TAB
MONITER CUT
MUTE
LINE MUTE
Hi-Fi MUTE
CYL. ON
COUNT. DATA
CLOCK(S-T)
DATA(S-T)
DATA(T-S)
POWER INDI.
FM CONT
M. STATE 3
M. STATE 2
M. STATE 1
TAB
MUTE
CYL. ON
MONITER CUT
POWER INDI.
MEMORY STOP
DATA (T-S)
DATA (S-T)
CLOCK (S-T)
COUNT. DATA
REEL PULSE
4
5
6
7
8
9
10
11

GES: PB AND (REC) MODES.

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REMOTE CONTROL	5-24
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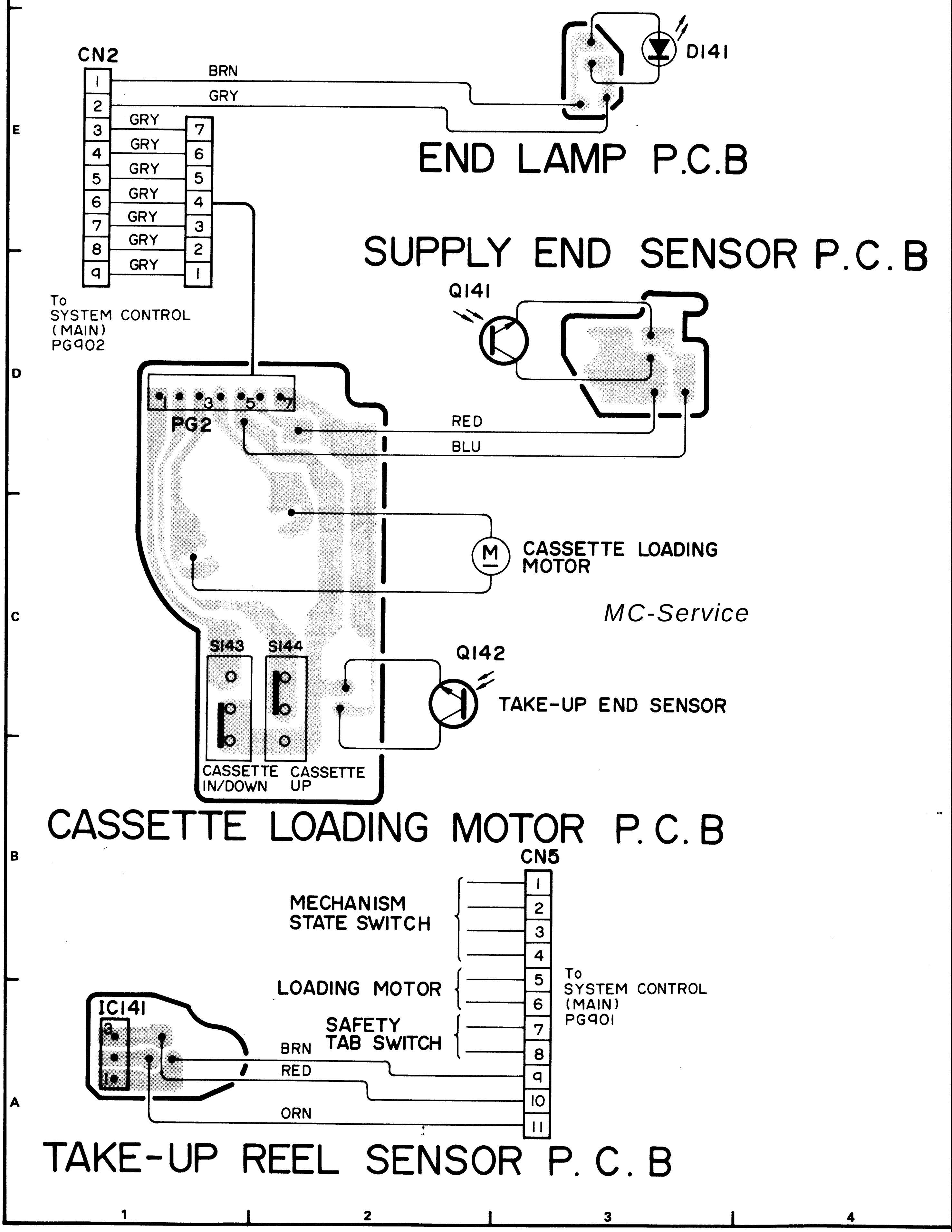
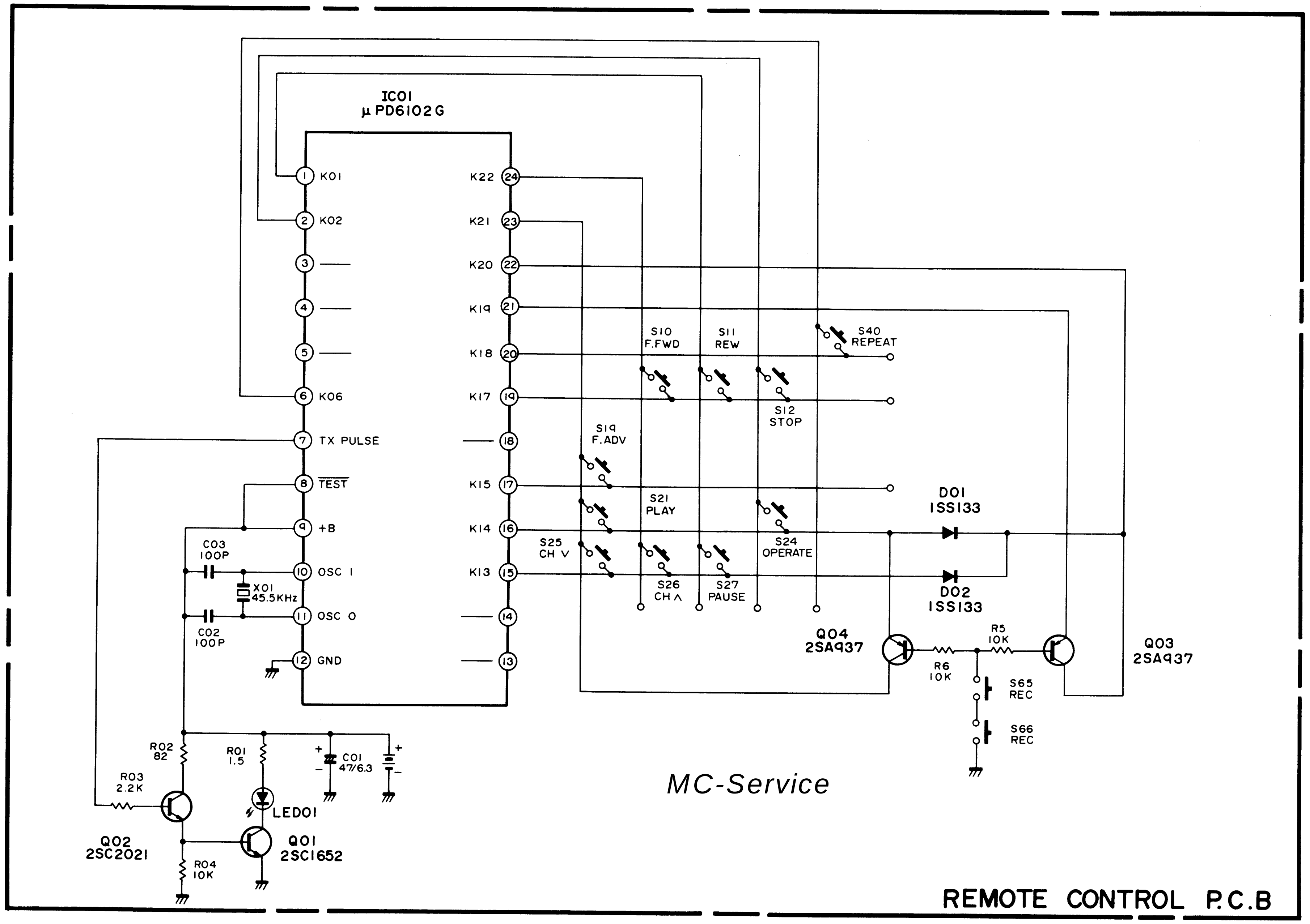
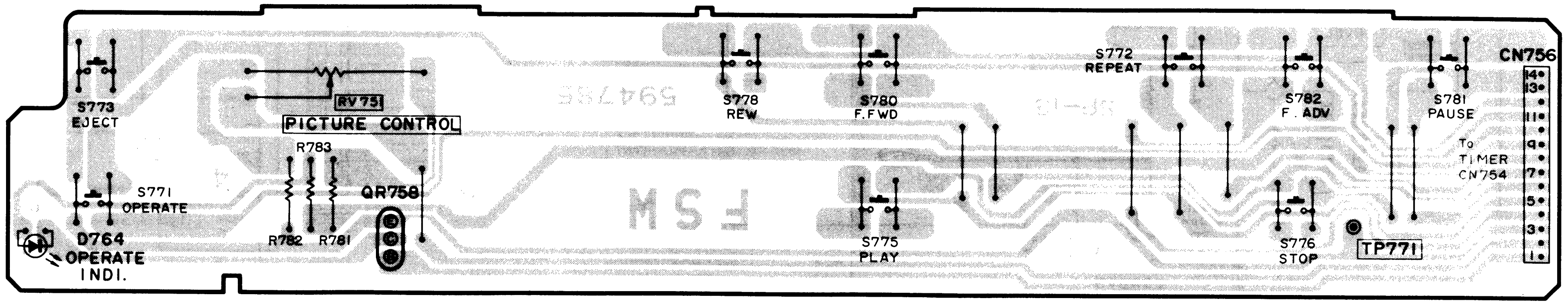
RF CONVERTER	5-29
PREAMP	5-30
SERVO	5-39
Y/CHROMA	5-42
REGULATOR	5-51
INTERNAL WIRING DIAGRAM	5-55

PERIPHERAL BOARD (PERIPHERIE-LEITERPLATTE)


CN2
1
2
3
4
5
6
7
8
9
BRN
GRY
GRY
GRY
GRY
GRY
GRY
GRY
GRY
7
6
5
4
3
2
1
To
SYSTEM CONTROL
(MAIN)
PG902
D141
END LAMP P.C.B
SUPPLY END SENSOR P.C.B
Q141
PG2
1
3
5
7
RED
BLU
M
CASSETTE LOADING
MOTOR
S143
S144
Q142
TAKE-UP END SENSOR
CASSETTE
IN/DOWN
CASSETTE
UP
CASSETTE LOADING MOTOR P.C.B
CN5
1
2
3
4
5
6
7
8
9
10
11
MECHANISM
STATE SWITCH
LOADING MOTOR
SAFETY
TAB SWITCH
To
SYSTEM CONTROL
(MAIN)
PG901
IC141
3
1
BRN
RED
ORN
TAKE-UP REEL SENSOR P.C.B
E
D
C
B
A
1
2
3
4

REMOTE CONTROL/OPERATION SWITCH (FERNBEDIENUNG/FUNKTIONSSCHALTER) – VT-110E –

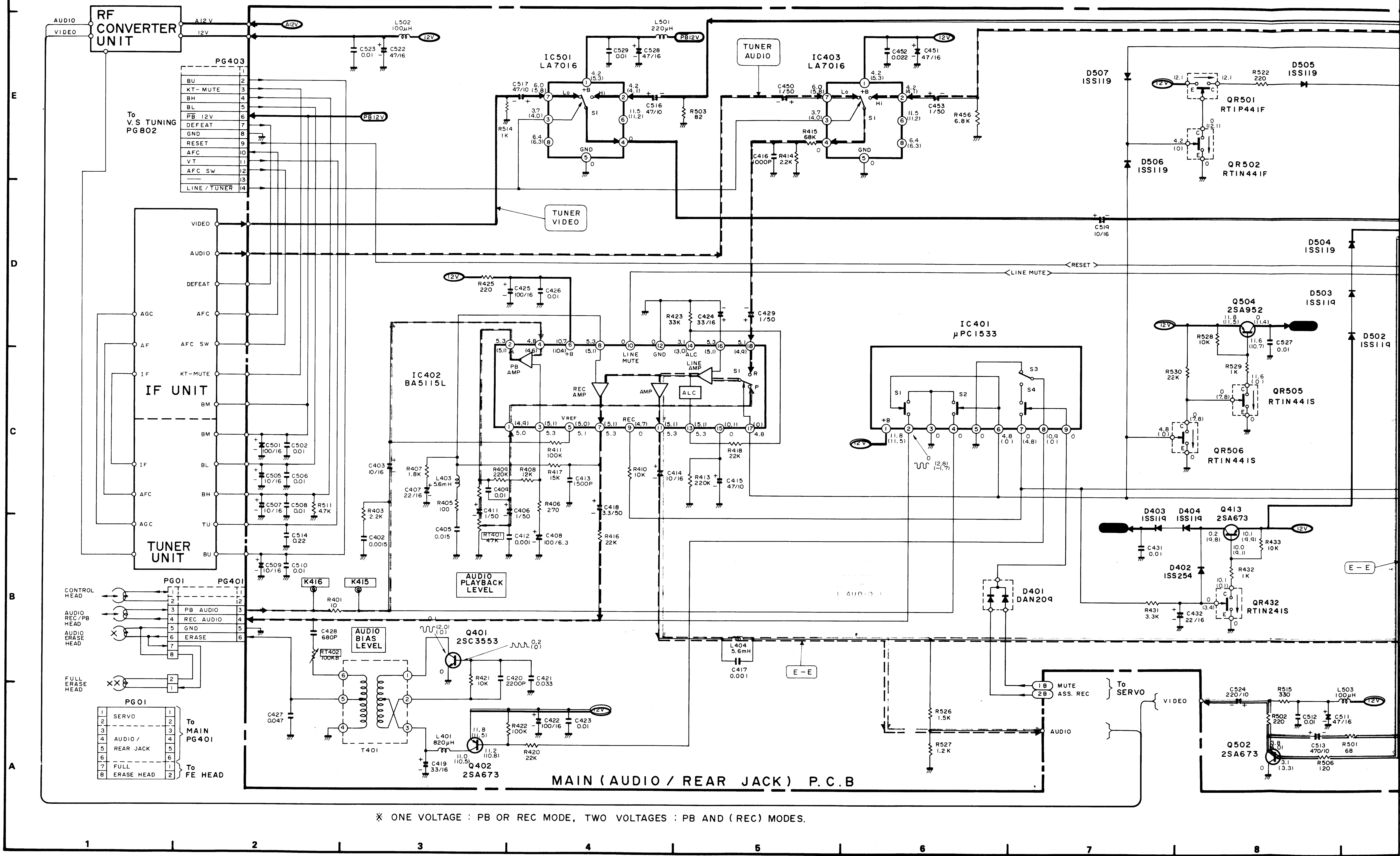

IC01
μ PD6102G
1 K01
2 K02
3
4
5
6 K06
7 TX PULSE
8 TEST
9 +B
10 OSC I
11 OSC O
12 GND
K22 24
K21 23
K20 22
K19 21
K18 20
K17 19
18
K15 17
K14 16
K13 15
14
13
S10 F.FWD
S11 REW
S40 REPEAT
S12 STOP
S19 F.ADV
S21 PLAY
S24 OPERATE
S25 CH V
S26 CH ∧
S27 PAUSE
D01 1SS133
D02 1SS133
Q04 2SA937
Q03 2SA937
R5 10K
R6 10K
S65 REC
S66 REC
C03 100P
X01 45.5KHz
C02 100P
R02 82
R01 1.5
C01 47/6.3
R03 2.2K
LED01
Q02 2SC2021
Q01 2SC1652
R04 10K
REMOTE CONTROL P.C.B


S773 EJECT
RV751
PICTURE CONTROL
R783
R782 R781
QR758
S771 OPERATE
D764 OPERATE INDI.
S778 REW
S780 F.FWD
S775 PLAY
S772 REPEAT
S782 F. ADV
S781 PAUSE
S776 STOP
TP771
CN756
To TIMER CN754
14
13
11
9
7
5
3
1
FSM

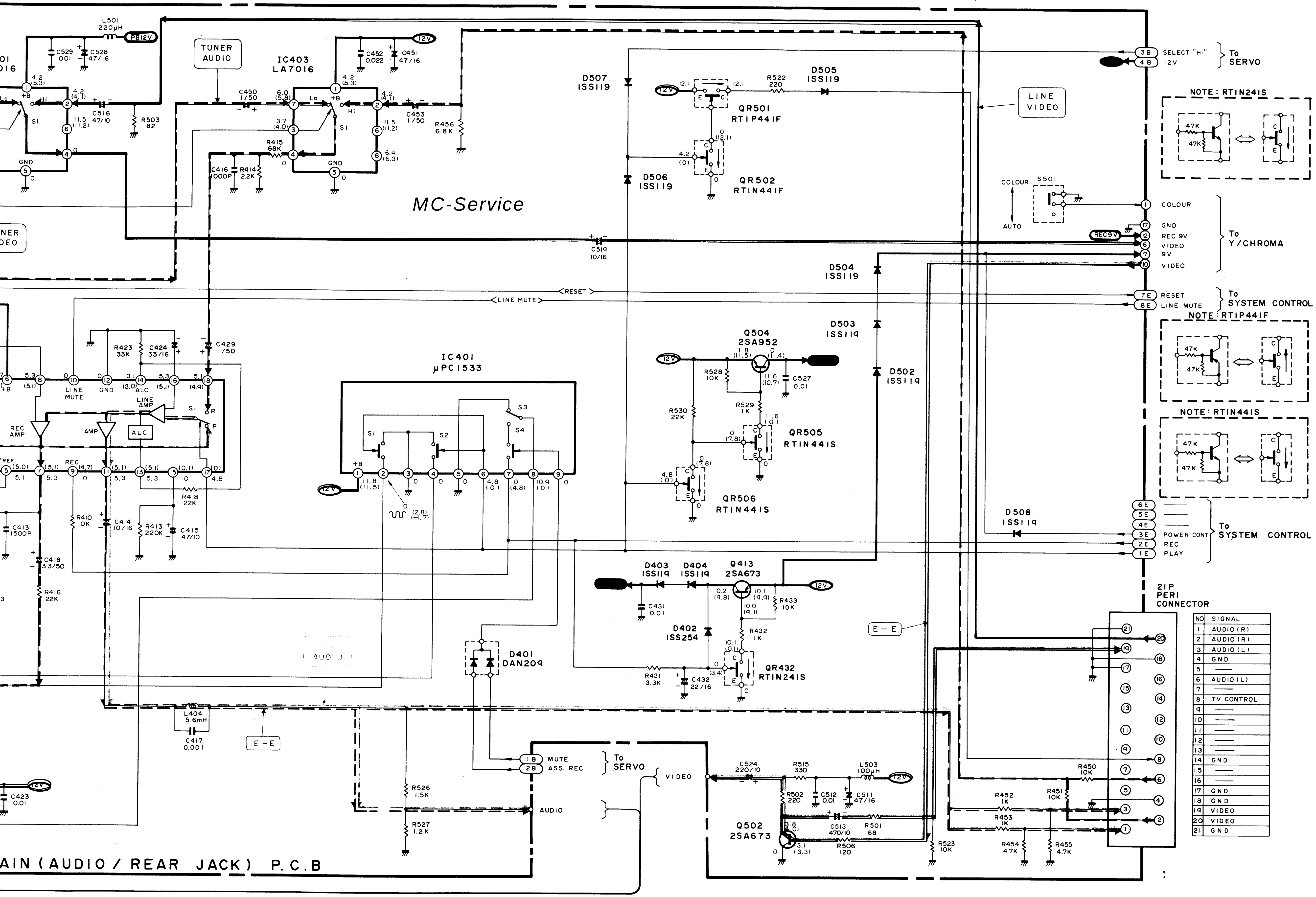
OPERATION SWITCH P.C.B

5 6 7 8 9 10 11

AUDIO/REAR JACK (AUDIO-BUCHSE)


RF CONVERTER UNIT
AUDIO
VIDEO
A12V
12V
PG403
BU
KT-MUTE
BH
BL
PB 12V
DEFEAT
GND
RESET
AFC
VT
AFC SW
LINE / TUNER
To V.S TUNING PG802
IF UNIT
TUNER UNIT
VIDEO
AUDIO
DEFEAT
AGC
AFC
AF
AFC SW
IF
KT-MUTE
BM
BL
BH
TU
BU
L502 100μH
C523 0.01
C522 47/16
L501 220μH
PB12V
IC501 LA7016
C529 0.01
C528 47/16
C517 47/10
C516 47/10
R514 1K
R503 82
S1
Lo
Hi
+B
GND
TUNER VIDEO
TUNER AUDIO
IC403 LA7016
C452 0.022
C451 47/16
C450 1/50
C453 1/50
R415 68K
C416 1000P
R414 2.2K
R456 6.8K
D507 ISS119
D506 ISS119
D505 ISS119
R522 220
QR501 RT1P441F
QR502 RTIN441F
C519 10/16
D504 ISS119
D503 ISS119
D502 ISS119
RESET
LINE MUTE
Q504 2SA952
R528 10K
R529 1K
C527 0.01
R530 22K
QR505 RTIN441S
QR506 RTIN441S
IC401 μPC1533
S1
S2
S3
S4
IC402 BA5115L
R425 220
C425 100/16
C426 0.01
R423 33K
C424 33/16
C429 1/50
PB AMP
REC AMP
AMP
LINE AMP
ALC
LINE MUTE
VREF
REC
C403 10/16
R407 1.8K
L403 5.6mH
C407 22/16
R405 100
C405 0.015
R403 2.2K
C402 0.0015
R409 220K
C409 0.01
C411 1/50
RT401 47K
R408 12K
C406 1/50
C412 0.001
R411 100K
R417 15K
C413 1500P
R406 270
C408 100/6.3
C418 3.3/50
R416 22K
R410 10K
C414 10/16
R413 220K
C415 47/10
R418 22K
C501 100/16
C502 0.01
C505 10/16
C506 0.01
C507 10/16
C508 0.01
R511 4.7K
C514 0.22
C509 10/16
C510 0.01
K416
K415
R401 10
AUDIO PLAYBACK LEVEL
D403 ISS119
D404 ISS119
Q413 2SA673
C431 0.01
R433 10K
D402 ISS254
R432 1K
R431 3.3K
C432 22/16
QR432 RTIN241S
D401 DAN209
E – E
CONTROL HEAD
AUDIO REC/PB HEAD
AUDIO ERASE HEAD
FULL ERASE HEAD
PG01
PG401
PB AUDIO
REC AUDIO
GND
ERASE
C428 680P
RT402 100KB
AUDIO BIAS LEVEL
Q401 2SC3553
R421 10K
C420 2200P
C421 0.033
C427 0.047
T401
L401 820μH
Q402 2SA673
C419 33/16
R422 100K
C422 100/16
C423 0.01
R420 22K
L404 5.6mH
C417 0.001
R526 1.5K
R527 1.2K
1B MUTE
2B ASS. REC
AUDIO
To SERVO
VIDEO
C524 220/10
R515 330
L503 100μH
R502 220
C512 0.01
C511 47/16
C513 470/10
R501 68
R506 120
Q502 2SA673
SERVO
AUDIO / REAR JACK
FULL ERASE HEAD
To MAIN PG401
To FE HEAD
MAIN (AUDIO / REAR JACK) P.C.B
A
B
C
D
E
1
2
3
4
5
6
7
8

※ ONE VOLTAGE : PB OR REC MODE, TWO VOLTAGES : PB AND (REC) MODES.


L501 220μH
PB12V
C529 0.01
C528 47/16
C516 47/10
R503 82
TUNER AUDIO
IC403 LA7016
C450 1/50
C452 0.022
C451 47/16
C453 1/50
R456 6.8K
R415 68K
C416 1000P
R414 2.2K
GND
Lo
Hi
S1
+B
12V
D507 1SS119
D505 1SS119
R522 220
QR501 RT1P441F
QR502 RT1N441F
D506 1SS119
LINE VIDEO
C519 10/16
D504 1SS119
D503 1SS119
D502 1SS119
RESET
LINE MUTE
R423 33K
C424 33/16
C429 1/50
LINE AMP
REC AMP
AMP
ALC
S1
R
P
IC401 μPC1533
S1 S2 S3 S4
Q504 2SA952
R528 10K
C527 0.01
R530 22K
R529 1K
QR505 RT1N441S
QR506 RT1N441S
R410 10K
C414 10/16
R413 220K
C415 47/10
R418 22K
C413 1500P
C418 3.3/50
R416 22K
C423 0.01
D403 1SS119
D404 1SS119
Q413 2SA673
C431 0.01
R433 10K
D402 1SS254
R432 1K
R431 3.3K
C432 22/16
QR432 RT1N241S
D401 DAN209
E-E
L404 5.6mH
C417 0.001
1B MUTE
2B ASS. REC
To SERVO
VIDEO
AUDIO
R526 1.5K
R527 1.2K
C524 220/10
R515 330
L503 100μH
R502 220
C512 0.01
C511 47/16
Q502 2SA673
C513 470/10
R501 68
R506 120
R523 10K
R450 10K
R452 1K
R453 1K
R451 10K
R454 4.7K
R455 4.7K
D508 1SS119
3B SELECT "Hi"
4B 12V
To SERVO
NOTE: RTIN241S
NOTE: RTIP441F
NOTE: RTIN441S
47K
COLOUR
S501
AUTO
COLOUR
GND
REC 9V
VIDEO
9V
VIDEO
To Y/CHROMA
7E RESET
8E LINE MUTE
To SYSTEM CONTROL
6E 5E 4E
3E POWER CONT.
2E REC
1E PLAY
To SYSTEM CONTROL
21P PERI CONNECTOR
4 5 6 7 8 9 10 11

NO	SIGNAL
1	AUDIO (R)
2	AUDIO (R)
3	AUDIO (L)
4	GND
5	——
6	AUDIO (L)
7	——
8	TV CONTROL
9	——
10	——
11	——
12	——
13	——
14	GND
15	——
16	——
17	GND
18	GND
19	VIDEO
20	VIDEO
21	GND

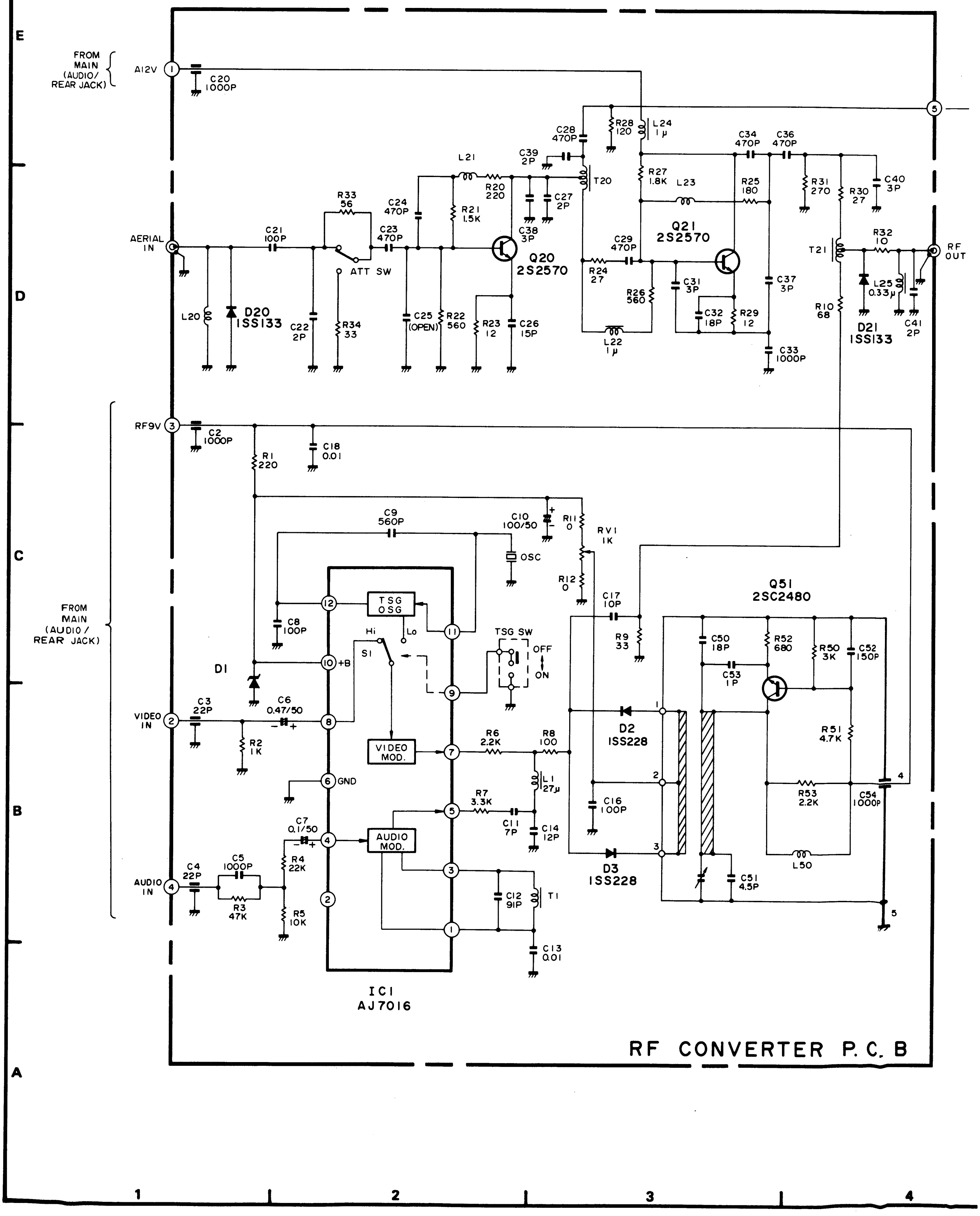
AIN (AUDIO / REAR JACK) P. C. B

E, TWO VOLTAGES : PB AND (REC) MODES.

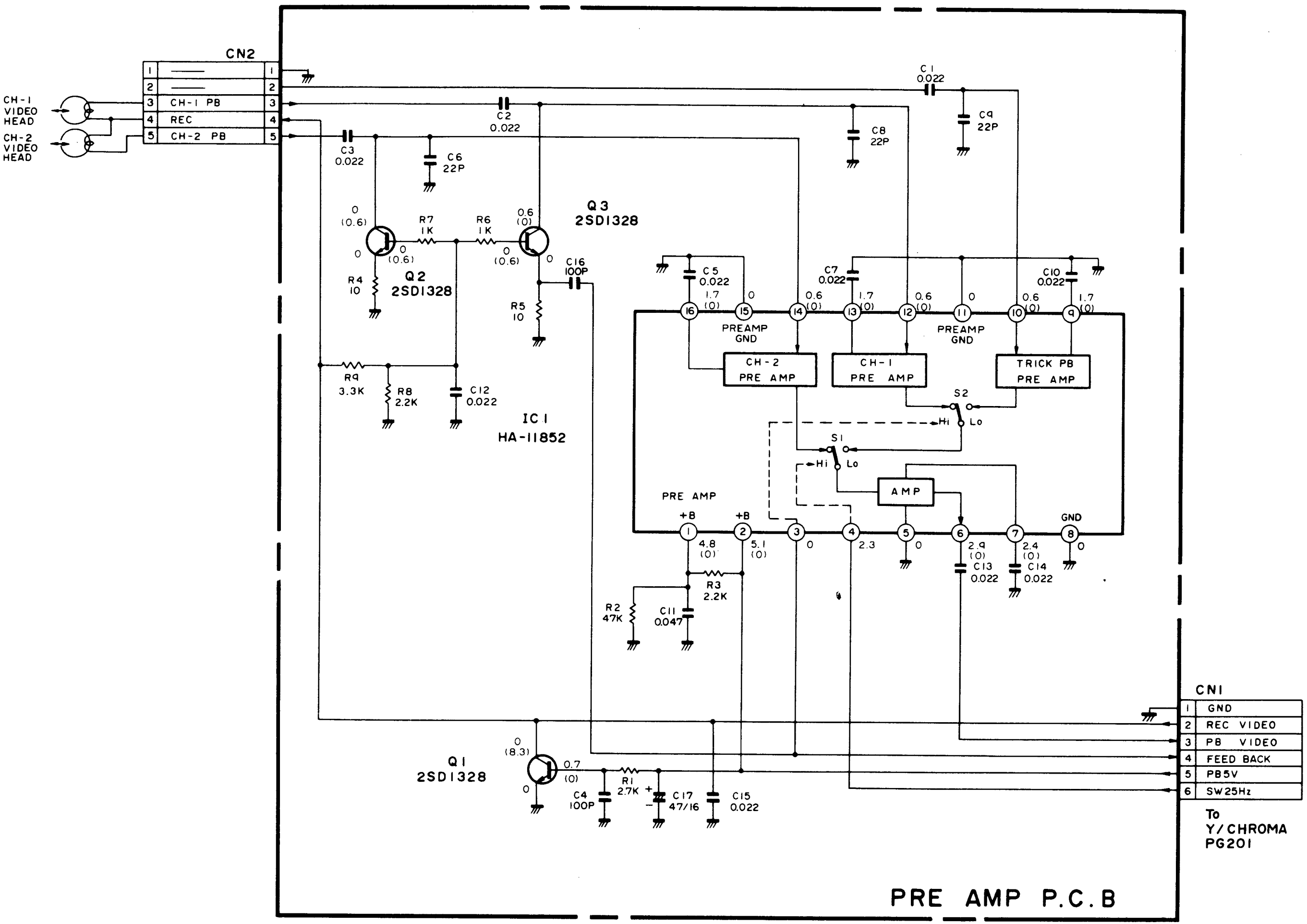
SCHEMATIC DIAGRAM PAGE

TUNER UNIT.............................. 5-2
IF UNIT.................................... 5-3
V·S TUNING.............................. 5-5
TIMER/OPERATION SWITCH
  – VT-110E –......................... 5-11
TIMER/OPERATION SWITCH
  – VT-120E –......................... 5-14
SYSTEM CONTROL................. 5-20
REMOTE CONTROL................ 5-24
AUDIO/REAR JACK................ 5-26
RF CONVERTER..................... 5-29
PREAMP................................. 5-30
SERVO.................................... 5-39
Y/CHROMA............................ 5-42
REGULATOR.......................... 5-51
INTERNAL WIRING DIAGRAM 5-55

RF CONVERTER (HF-KONVERTER)


E
D
C
B
A
1
2
3
4
FROM MAIN (AUDIO/ REAR JACK)
A12V ①
C20 1000P
⑤
R28 120
L24 1μ
C28 470P
C39 2P
T20
C34 470P
C36 470P
L21
R20 220
C27 2P
R27 1.8K
L23
R25 180
R31 270
R30 27
C40 3P
R33 56
C24 470P
R21 1.5K
C38 3P
Q21 2S2570
C23 470P
C21 100P
AERIAL IN
ATT SW
Q20 2S2570
C29 470P
R24 27
T21
R32 10
RF OUT
D20 1SS133
L20
C22 2P
R34 33
C25 (OPEN)
R22 560
R23 12
C26 15P
R26 560
C31 3P
C32 18P
R29 12
C37 3P
R10 68
L25 0.33μ
D21 1SS133
C41 2P
L22 1μ
C33 1000P
RF9V ③
C2 1000P
R1 220
C18 0.01
C9 560P
C10 100/50
R11 0
RV1 1K
OSC
R12 0
Q51 2SC2480
C17 10P
R9 33
TSG OSG
Hi
Lo
S1
TSG SW
OFF
ON
C8 100P
C50 18P
R52 680
R50 3K
C52 150P
C53 1P
D1
+B
VIDEO IN ②
C3 22P
C6 0.47/50
R2 1K
D2 1SS228
VIDEO MOD.
R6 2.2K
R8 100
R51 4.7K
GND
L1 27μ
R7 3.3K
C16 100P
R53 2.2K
C54 1000P
C7 0.1/50
C11 7P
C14 12P
AUDIO MOD.
L50
AUDIO IN ④
C4 22P
C5 1000P
R4 22K
R3 47K
R5 10K
D3 1SS228
C51 4.5P
C12 91P
T1
C13 0.01
IC1 AJ7016
RF CONVERTER P.C.B

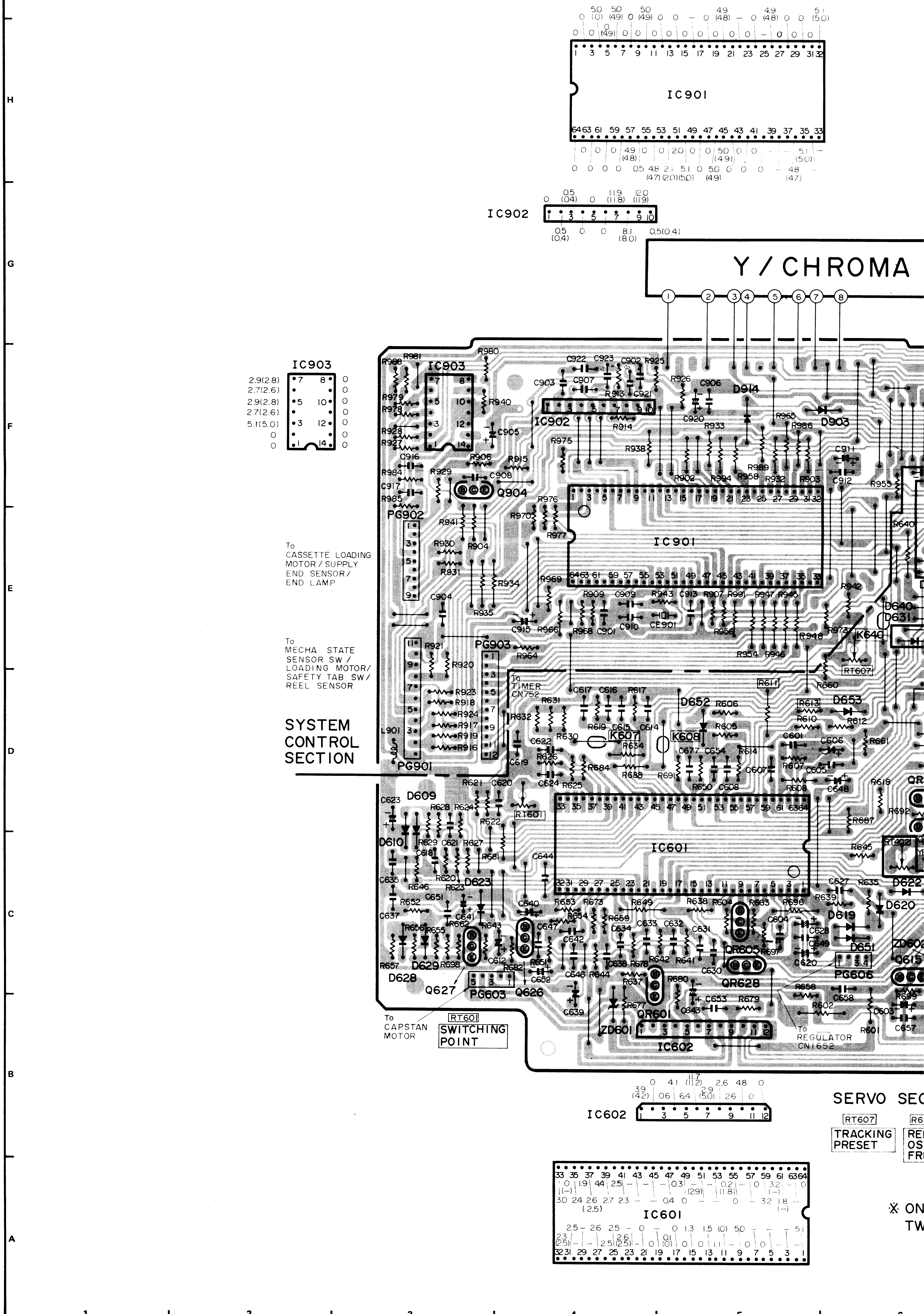
PREAMP (CORVERSTÄRKER)

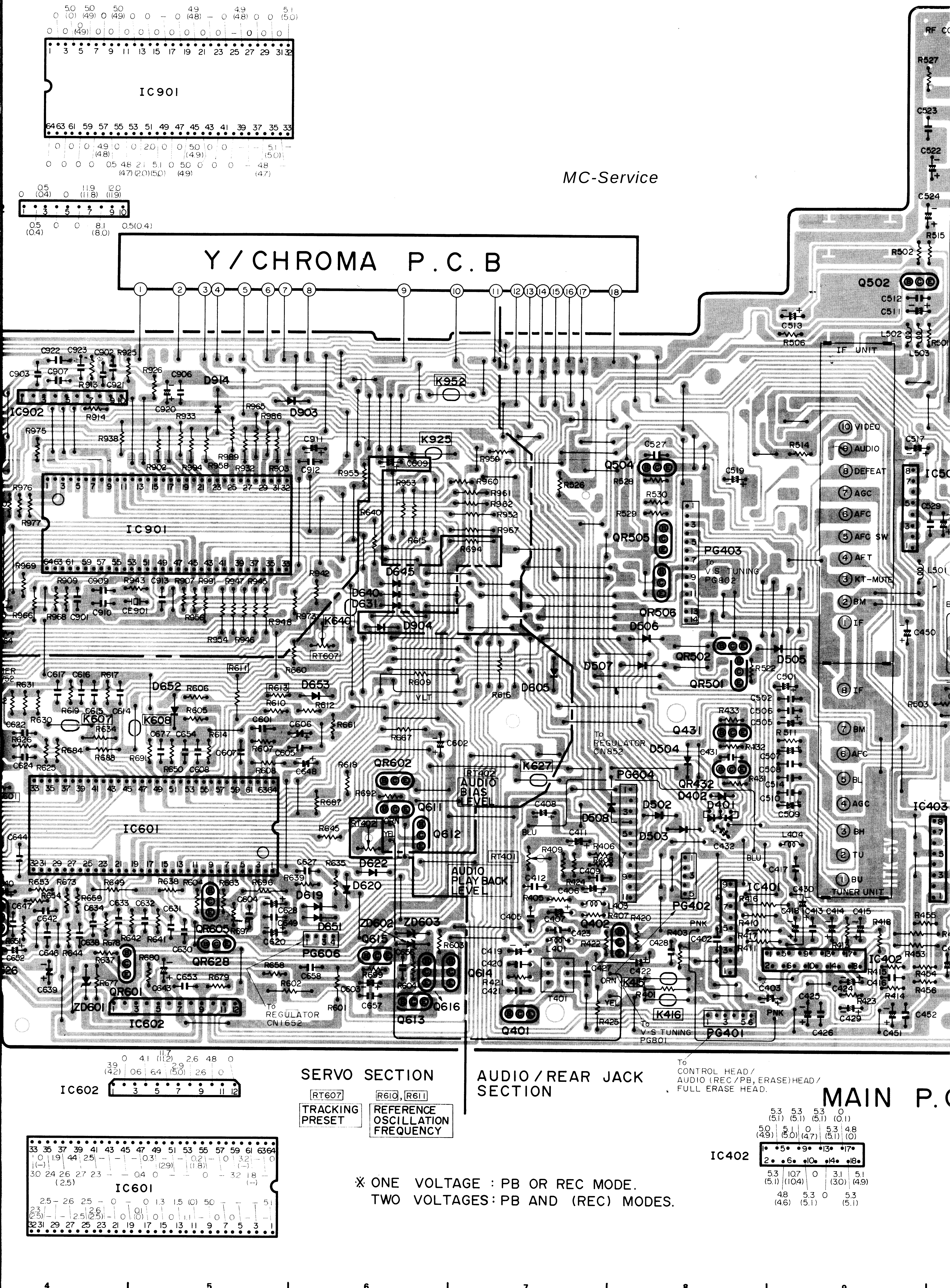

CN2
CH-1 VIDEO HEAD
CH-2 VIDEO HEAD
CH-1 PB
REC
CH-2 PB
C1 0.022
C2 0.022
C3 0.022
C6 22P
C8 22P
C9 22P
Q3 2SD1328
Q2 2SD1328
R7 1K
R6 1K
R4 10
R5 10
C16 100P
C5 0.022
C7 0.022
C10 0.022
R9 3.3K
R8 2.2K
C12 0.022
IC1 HA-11852
PREAMP GND
CH-2 PRE AMP
CH-1 PRE AMP
TRICK PB PRE AMP
S2
S1
Hi
Lo
AMP
PRE AMP
+B
GND
R3 2.2K
R2 47K
C11 0.047
C13 0.022
C14 0.022
Q1 2SD1328
C4 100P
R1 2.7K
C17 47/16
C15 0.022
CN1
GND
REC VIDEO
PB VIDEO
FEED BACK
PB5V
SW25Hz
To Y/CHROMA PG201
PRE AMP P.C.B

※ONE VOLTAGE : PB OR REC MODE,
TWO VOLTAGES : PB AND (REC) MODE.

SCHEMATIC DIAGRAM	PAGE
TUNER UNIT	5-2
IF UNIT	5-3
V·S TUNING	5-5
TIMER/OPERATION SWITCH -VT-110E-	5-11
TIMER/OPERATION SWITCH -VT-120E-	5-14
SYSTEM CONTROL	5-20
REMOTE CONTROL	5-24
AUDIO/REAR JACK	5-26
RF CONVERTER	5-29
PREAMP	5-30
SERVO	5-39
Y/CHROMA	5-42
REGULATOR	5-51
INTERNAL WIRING DIAGRAM	5-55

MAIN (HAUPT)


IC901
IC902
IC903
IC601
IC602
Y / CHROMA
SYSTEM CONTROL SECTION
To CASSETTE LOADING MOTOR / SUPPLY END SENSOR / END LAMP
To MECHA STATE SENSOR SW / LOADING MOTOR / SAFETY TAB SW / REEL SENSOR
To TIMER CN752
To CAPSTAN MOTOR
To REGULATOR CN1652
RT601 SWITCHING POINT
SERVO SEC
RT607 TRACKING PRESET
PG901
PG902
PG903
PG603
PG606
Q904
Q626
Q627
QR601
QR605
QR628
K607
K608
K640
D609
D610
D623
D628
D629
D652
D653
D903
D914
ZD601
L901
CE901
A
B
C
D
E
F
G
H
1
2
3
4
5
※ ON
TW


IC901
IC902
Y/CHROMA P.C.B
IC601
IC602
IC401
IC402
IC403
Q502
Q504
Q401
Q402
Q431
IF UNIT
VIDEO
AUDIO
DEFEAT
AGC
AFC
AFC SW
AFT
KT-MUTE
BM
IF
BL
BH
TU
BU
TUNER UNIT
PG401
PG402
PG403
PG604
PG606
K952
K925
K640
K607
K608
K627
K415
K416
RT402 AUDIO BIAS LEVEL
RT401 AUDIO PLAY BACK LEVEL
RT607
To REGULATOR CN852
To REGULATOR CN1652
To V.S TUNING PG802
To V.S TUNING PG801
To CONTROL HEAD/ AUDIO (REC/PB, ERASE) HEAD/ FULL ERASE HEAD.
4
5
6
7
8
9

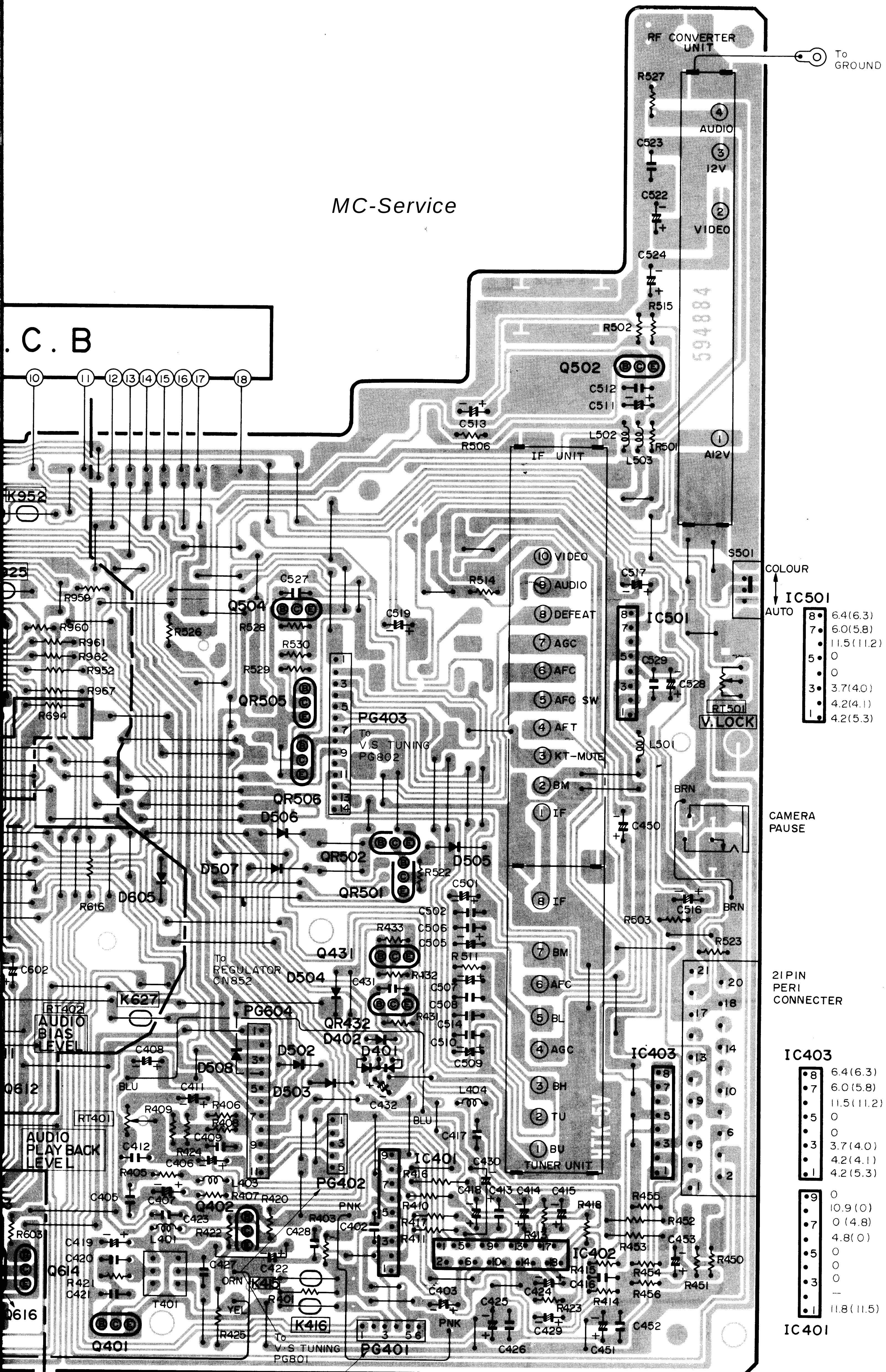
SERVO SECTION

RT607	R610, R611
TRACKING PRESET	REFERENCE OSCILLATION FREQUENCY

AUDIO / REAR JACK SECTION

MAIN P.C

※ ONE VOLTAGE : PB OR REC MODE.
TWO VOLTAGES: PB AND (REC) MODES.


RF CONVERTER UNIT
To GROUND
R527
④ AUDIO
C523
③ 12V
C522
② VIDEO
C524
R515
R502
594884
Q502
C512
C511
C513
R506
L502
L503
R501
① A12V
IF UNIT
.C.B
10
11
12
13
14
15
16
17
18
K952
525
R959
R960
R961
R962
R952
R967
R694
C527
Q504
R528
R526
R530
R529
QR505
QR506
PG403
To V.S TUNING PG802
C519
R514
⑩ VIDEO
⑨ AUDIO
⑧ DEFEAT
⑦ AGC
⑥ AFC
⑤ AFC SW
④ AFT
③ KT-MUTE
② BM
① IF
C517
S501
COLOUR
AUTO
IC501
C529
C528
RT501
V. LOCK
L501
BRN
CAMERA PAUSE
C450
D506
D507
QR502
QR501
D505
R522
D605
R616
C501
C502
C506
C505
⑧ IF
C516
BRN
R603
R523
R433
Q431
R511
To REGULATOR CN852
D504
C431
R432
C507
C508
C514
C510
C509
R431
QR432
D402
D401
C432
⑦ BM
⑥ AFC
⑤ BL
④ AGC
③ BH
② TU
① BU
TUNER UNIT
21PIN PERI CONNECTER
21
20
17
18
14
13
10
9
6
5
2
1
IC403
C602
RT402
AUDIO BIAS LEVEL
K627
PG604
D508
D502
D503
C408
BLU
C411
R406
R409
R408
RT401
AUDIO PLAY BACK LEVEL
C409
C412
R424
C406
R405
L403
L404
BLU
C417
IC401
C430
R416
C418
C413
C414
C415
R418
R455
C405
C407
Q402
R407
R420
PG402
PNK
R410
R417
R411
C402
R403
R452
R453
C453
C419
C420
C421
R421
L401
C425
R422
C428
C427
C422
T401
K415
ORN
YEL
R401
R425
K416
To V.S TUNING PG801
PG401
1 3 5 6
PNK
IC402
R415
C416
R454
R456
R451
R450
C403
C425
C424
R423
R414
C429
C426
C451
C452
Q401
Q612
Q614
Q616
R603

AUDIO / REAR JACK SECTION

To
CONTROL HEAD/
AUDIO (REC/PB, ERASE) HEAD/
FULL ERASE HEAD.

MAIN P.C.B

IC501

8	6.4(6.3)
7	6.0(5.8)
	11.5(11.2)
5	0
	0
3	3.7(4.0)
	4.2(4.1)
1	4.2(5.3)

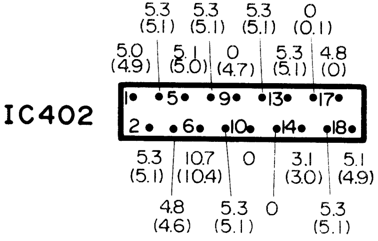
IC403

8	6.4(6.3)
7	6.0(5.8)
	11.5(11.2)
5	0
	0
3	3.7(4.0)
	4.2(4.1)
1	4.2(5.3)

9	0
	10.9(0)
7	0(4.8)
	4.8(0)
5	0
	0
3	0
	—
1	11.8(11.5)

IC401

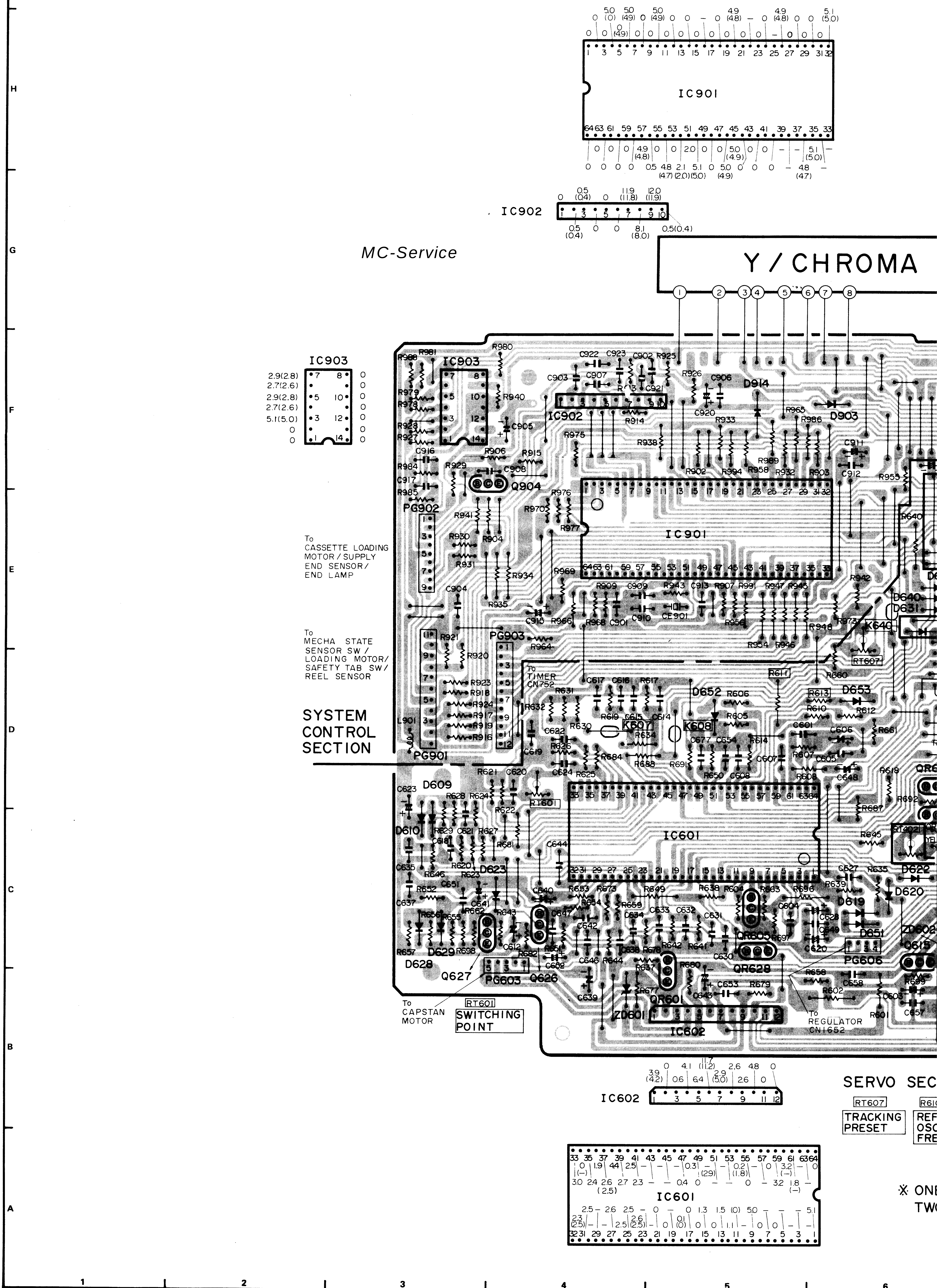
IC402

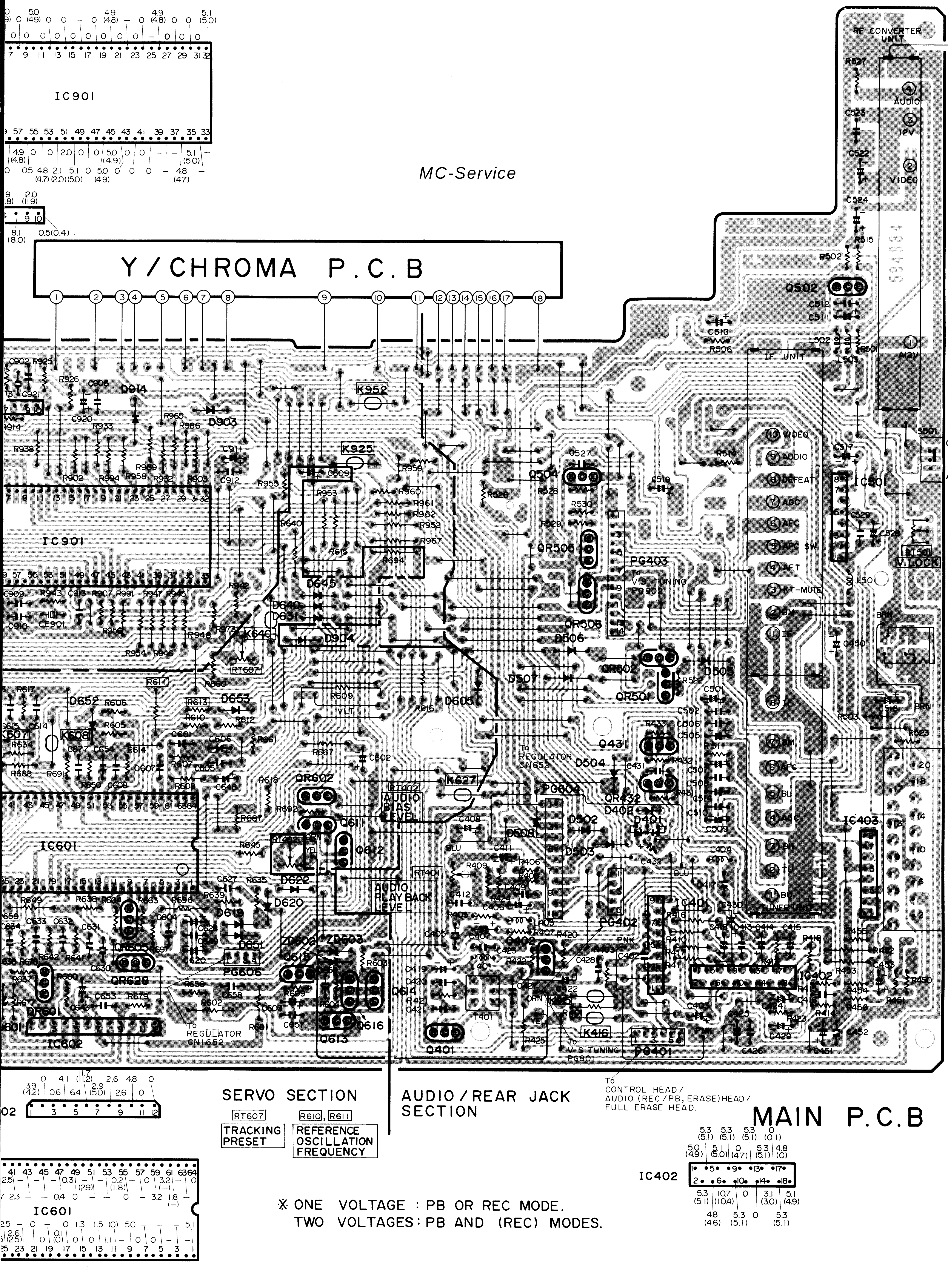

5.3 (5.1)
5.3 (5.1)
5.3 (5.1)
0 (0.1)
5.0 (4.9)
5.1 (5.0)
0 (4.7)
5.3 (5.1)
4.8 (0)
1
5
9
13
17
2
6
10
14
18
5.3 (5.1)
10.7 (10.4)
0
3.1 (3.0)
5.1 (4.9)
4.8 (4.6)
5.3 (5.1)
0
5.3 (5.1)

E
ION
CY

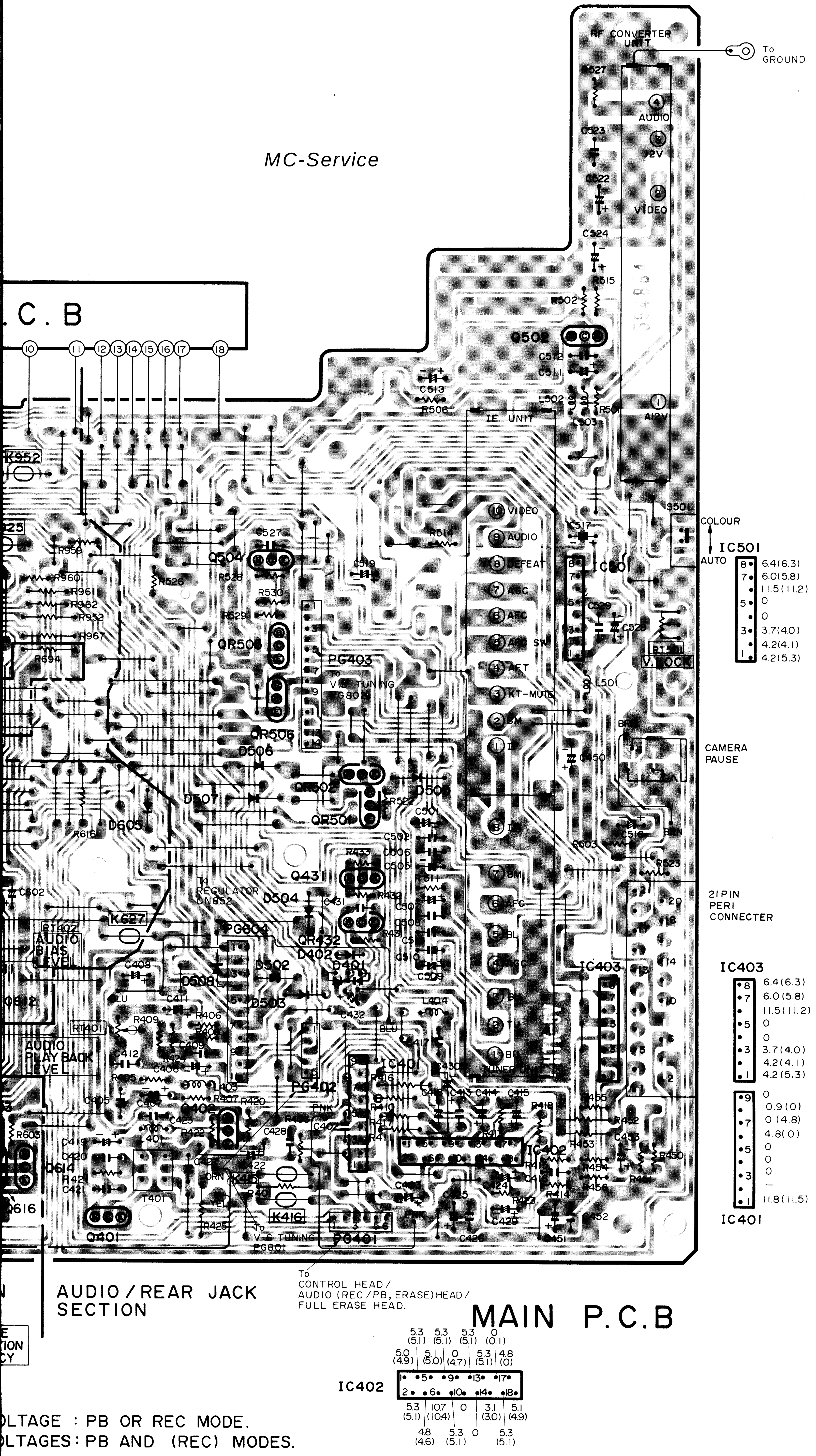
LTAGE : PB OR REC MODE.
LTAGES : PB AND (REC) MODES.

MAIN (HAUPT)


IC901
IC902
IC903
IC601
IC602
Y / CHROMA
To CASSETTE LOADING MOTOR / SUPPLY END SENSOR / END LAMP
To MECHA STATE SENSOR SW / LOADING MOTOR / SAFETY TAB SW / REEL SENSOR
SYSTEM CONTROL SECTION
To TIMER CN752
To CAPSTAN MOTOR
RT601
SWITCHING POINT
To REGULATOR CN1652
SERVO SEC
RT607
TRACKING PRESET
R610
REF OSC FRE
※ ONE
TWO
PG901
PG902
PG903
PG603
PG606
Q904
Q626
Q627
QR601
QR605
QR628
D903
D914
D609
D610
D623
D628
D629
D652
D653
D619
D620
D622
D651
ZD601
K607
K608
K640
H
G
F
E
D
C
B
A
1
2
3
4
5
6


Y/CHROMA P.C.B
IC901
IC601
IC602
IC401
IC402
IC403
IC501
RF CONVERTER UNIT
AUDIO
12V
VIDEO
A12V
IF UNIT
TUNER UNIT
VIDEO
AUDIO
DEFEAT
AGC
AFC
AFC SW
AFT
KT-MUTE
BM
IF
BL
BH
TU
BU
V.LOCK
To V.S TUNING PG802
To REGULATOR CN852
To REGULATOR CN1652
To V.S TUNING PG801
PG403
PG404
PG402
PG401
PG606
AUDIO BIAS LEVEL
AUDIO PLAY BACK LEVEL
RT402
RT401
RT607
K952
K925
K640
K627
K608
K607
K416
SERVO SECTION
RT607
TRACKING PRESET
R610, R611
REFERENCE OSCILLATION FREQUENCY
AUDIO/REAR JACK SECTION
To CONTROL HEAD/ AUDIO (REC/PB, ERASE) HEAD/ FULL ERASE HEAD.
MAIN P.C.B
5
6
7
8
9
10

※ ONE VOLTAGE : PB OR REC MODE.
TWO VOLTAGES : PB AND (REC) MODES.



RF CONVERTER UNIT
To GROUND
④ AUDIO
③ 12V
② VIDEO
① A12V
R527
C523
C522
C524
R515
R502
Q502
C512
C511
C513
R506
L502
R501
L503
IF UNIT
⑩ VIDEO
⑨ AUDIO
⑧ DEFEAT
⑦ AGC
⑥ AFC
⑤ AFC SW
④ AFT
③ KT-MUTE
② BM
① IF
⑧ IF
⑦ BM
⑥ AFC
⑤ BL
④ AGC
③ BH
② TU
① BU
TUNER UNIT
S501
COLOUR
AUTO
IC501
C517
C529
C528
RT501
V.LOCK
L501
BRN
CAMERA PAUSE
C450
C516
R503
R523
21PIN PERI CONNECTER
IC403
IC401
IC402
Q504
C527
R528
R530
R529
QR505
PG403
To V.S TUNING PG802
QR506
D506
D507
QR502
QR501
D505
R522
R514
C519
R526
C501
C502
C506
C505
R433
Q431
R432
R431
C431
QR432
D504
To REGULATOR CN852
K627
RT402
AUDIO BIAS LEVEL
PG604
D508
D502
D503
D402
D401
C432
L404
RT401
AUDIO PLAY BACK LEVEL
C408
C411
R409
R406
C409
C412
R424
C406
R405
L403
PG402
R407
R420
C405
C407
Q402
C423
R422
C428
C419
C420
L401
R421
C421
Q614
T401
C427
C422
K415
ORN
YEL
R425
K416
Q401
To V.S TUNING PG801
PG401
R603
Q616
R416
C418
C413
C414
C415
R418
R410
R417
R411
C402
R403
R455
R452
C453
R453
R450
R454
R456
R451
R414
C403
C425
C424
C429
C426
C451
C452
R423
K952
R959
R960
R961
R962
R952
R967
R694
R616
D605
C602
BLU
PNK
594884
.C. B
⑩ ⑪ ⑫ ⑬ ⑭ ⑮ ⑯ ⑰ ⑱
IC501
8 6.4(6.3)
7 6.0(5.8)
11.5(11.2)
5 0
0
3 3.7(4.0)
4.2(4.1)
1 4.2(5.3)
IC403
8 6.4(6.3)
7 6.0(5.8)
11.5(11.2)
5 0
0
3 3.7(4.0)
4.2(4.1)
1 4.2(5.3)
IC401
9 0
10.9(0)
7 0(4.8)
4.8(0)
5 0
0
3 0
–
1 11.8(11.5)
IC402
5.3 (5.1) 5.3 (5.1) 5.3 (5.1) 0 (0.1)
5.0 (4.9) 5.1 (5.0) 0 (4.7) 5.3 (5.1) 4.8 (0)
1 5 9 13 17
2 6 10 14 18
5.3 (5.1) 10.7 (10.4) 0 3.1 (3.0) 5.1 (4.9)
4.8 (4.6) 5.3 (5.1) 0 5.3 (5.1)
To CONTROL HEAD/ AUDIO (REC/PB, ERASE) HEAD/ FULL ERASE HEAD.

AUDIO / REAR JACK SECTION

MAIN P.C.B

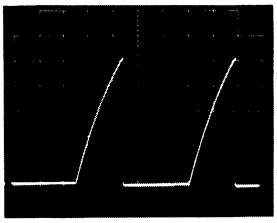
LTAGE : PB OR REC MODE.

LTAGES : PB AND (REC) MODES.

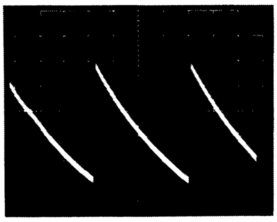
SERVO CIRCUIT WAVEFORMS (WELLENFORM)

[IC601] **(REC: Colour bar Video in/PB: Alignment tape)**

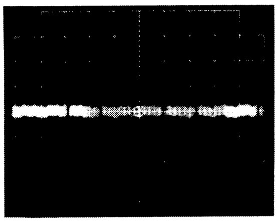
① PIN2 REC/PB
0.5V/10ms. div.



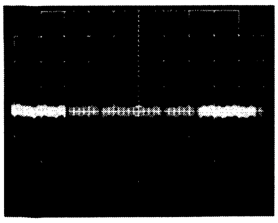
② PIN3 REC/PB
0.1V/10ms. div.



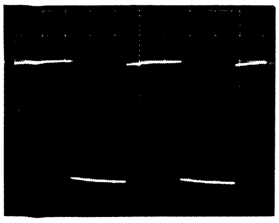
③ PIN4 REC/PB
50mV/10ms. div.



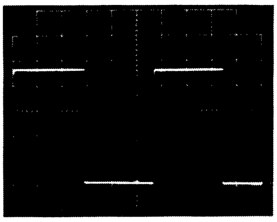
④ PIN5 REC/PB
50mV/10ms. div.



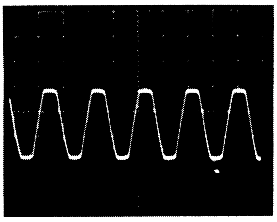
⑤ PIN11 REC/PB
1V/0.2ms. div.



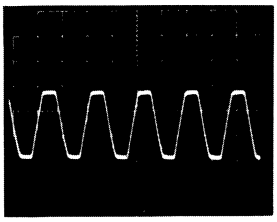
⑥ PIN22 REC/PB
1V/20μs. div.



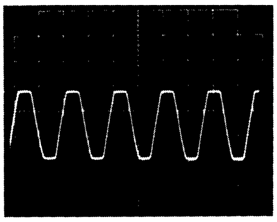
⑦ PIN28 REC/PB
0.5V/1ms. div.



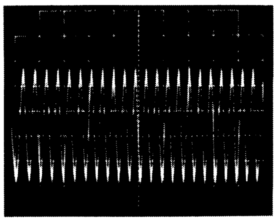
⑧ PIN29 REC/PB
0.5V/1ms. div.



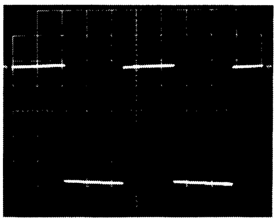
⑨ PIN30 REC/PB
1V/1ms. div.



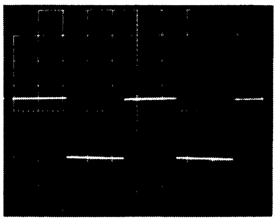
⑩ PIN32 REC/PB
50mV/0.5μs. div.



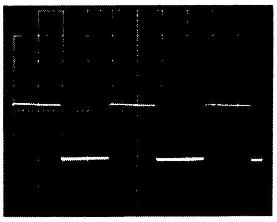
⑪ PIN42 REC/PB
1V/0.1ms. div.



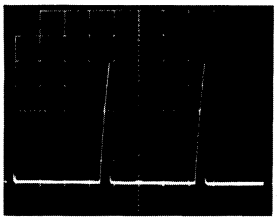
⑫ PIN43 REC/PB
2V/0.1ms. div.



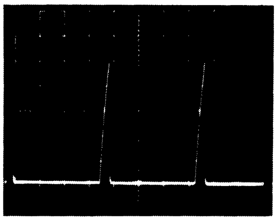
⑬ PIN44 REC/PB
2V/10ms. div.



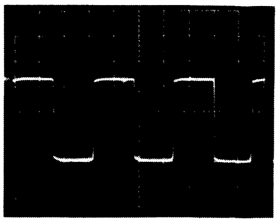
⑭ PIN45 REC/PB
0.5V/5ms. div.



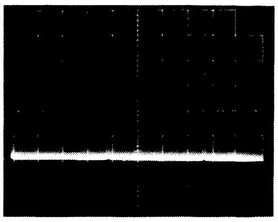
⑮ PIN46 REC/PB
0.5V/5ms. div.



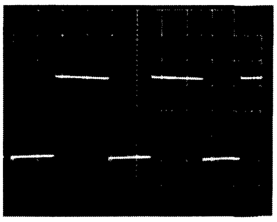
⑯ PIN50 REC/PB
1V/1ms. div.



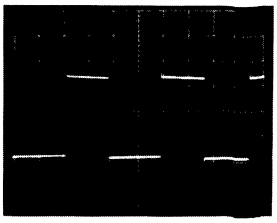
⑰ PIN53 REC/PB
1V/5ms. div.



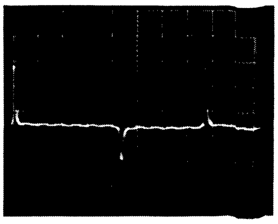
⑱ PIN59 REC
1V/10ms. div.



⑲ PIN60 REC
1V/10ms. div.

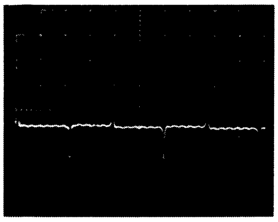


⑳ PIN62 PB
1V/5ms. div.



[IC601]

㉑ PIN63 PB
1V/10ms. div.



SCHEMATIC DIAGRAM	PAGE
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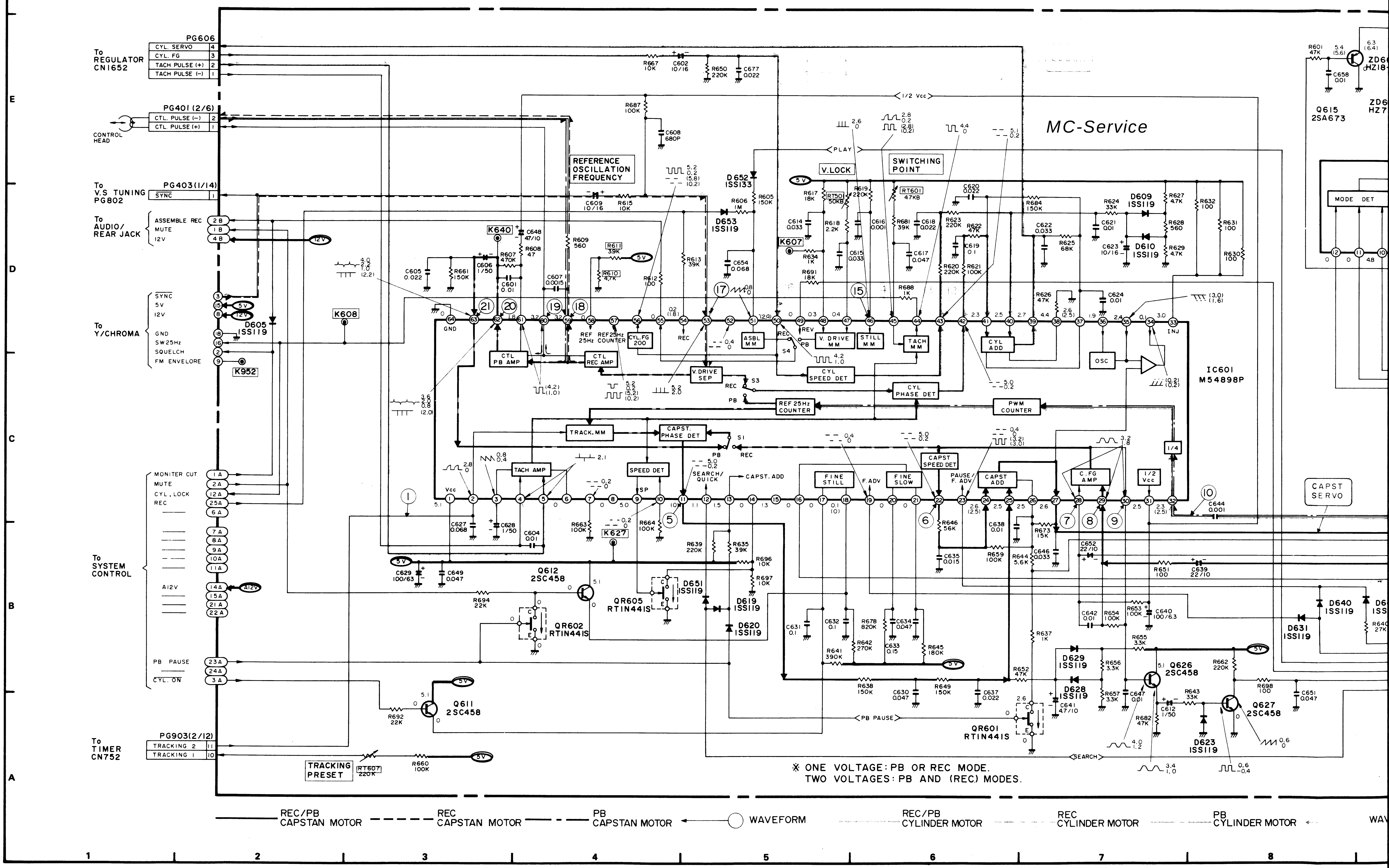
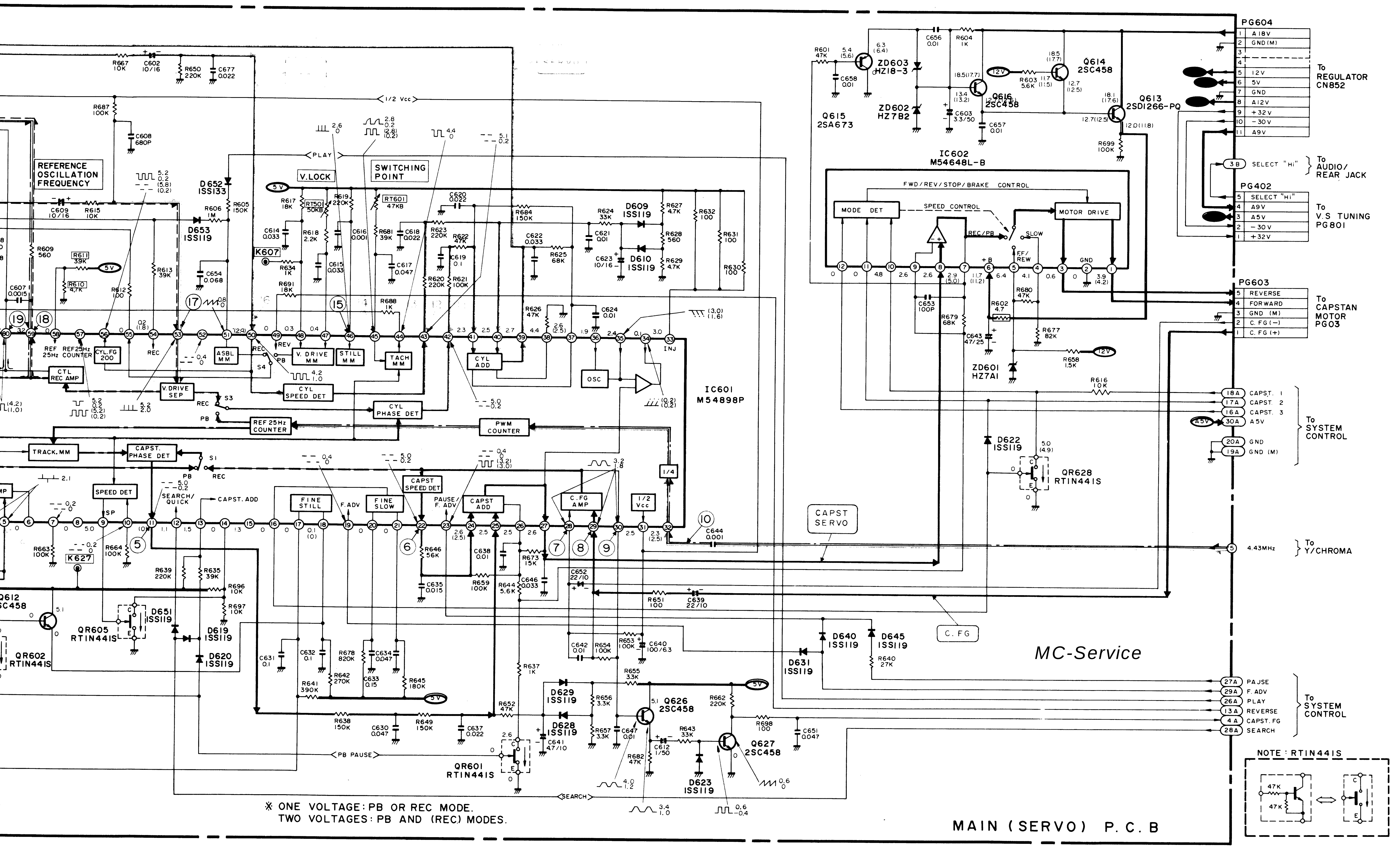
SERVO


To REGULATOR CN1652
PG606
CYL. SERVO
CYL. FG
TACH PULSE (+)
TACH PULSE (−)
CONTROL HEAD
PG401 (2/6)
CTL. PULSE (−)
CTL. PULSE (+)
To V.S TUNING PG802
PG403 (1/14)
SYNC
To AUDIO/ REAR JACK
ASSEMBLE REC
MUTE
12V
To Y/CHROMA
SYNC
5V
12V
GND
SW25Hz
SQUELCH
FM ENVELOPE
D605 1SS119
K608
K952
K640
K607
K627
To SYSTEM CONTROL
MONITER CUT
MUTE
CYL, LOCK
REC
A12V
PB PAUSE
CYL. ON
To TIMER CN752
PG903 (2/12)
TRACKING 2
TRACKING 1
TRACKING PRESET
RT607 220K
R660 100K
REFERENCE OSCILLATION FREQUENCY
MC-Service
1/2 Vcc
PLAY
V.LOCK
SWITCHING POINT
RT501 50KB
RT601 47KB
D652 1SS133
D653 1SS119
D609 1SS119
D610 1SS119
CTL PB AMP
CTL REC AMP
CYL.FG 200
V.DRIVE SEP
ASBL MM
V. DRIVE MM
STILL MM
TACH MM
CYL SPEED DET
CYL PHASE DET
REF 25Hz COUNTER
CYL ADD
OSC
PWM COUNTER
IC601 M54898P
INJ
GND
Vcc
REF 25Hz
REF25Hz COUNTER
REC
REV
PB
S3
S4
S1
TRACK. MM
CAPST. PHASE DET
TACH AMP
SPEED DET
SEARCH/ QUICK
CAPST. ADD
FINE STILL
FINE SLOW
F. ADV
CAPST SPEED DET
PAUSE/ F. ADV
CAPST ADD
C.FG AMP
1/2 Vcc
1/4
CAPST SERVO
Q612 2SC458
QR605 RTIN441S
QR602 RTIN441S
D651 1SS119
D619 1SS119
D620 1SS119
Q611 2SC458
QR601 RTIN441S
D629 1SS119
D628 1SS119
Q626 2SC458
Q627 2SC458
D623 1SS119
D640 1SS119
D631 1SS119
Q615 2SA673
MODE DET
PB PAUSE
SEARCH
5V
12V
A12V
① ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑮ ⑰ ⑱ ⑲ ⑳ ㉑
A
B
C
D
E
1
2
3
4
5
6
7
8

※ ONE VOLTAGE: PB OR REC MODE.
TWO VOLTAGES: PB AND (REC) MODES.

REC/PB CAPSTAN MOTOR	REC CAPSTAN MOTOR	PB CAPSTAN MOTOR	WAVEFORM	REC/PB CYLINDER MOTOR	REC CYLINDER MOTOR	PB CYLINDER MOTOR

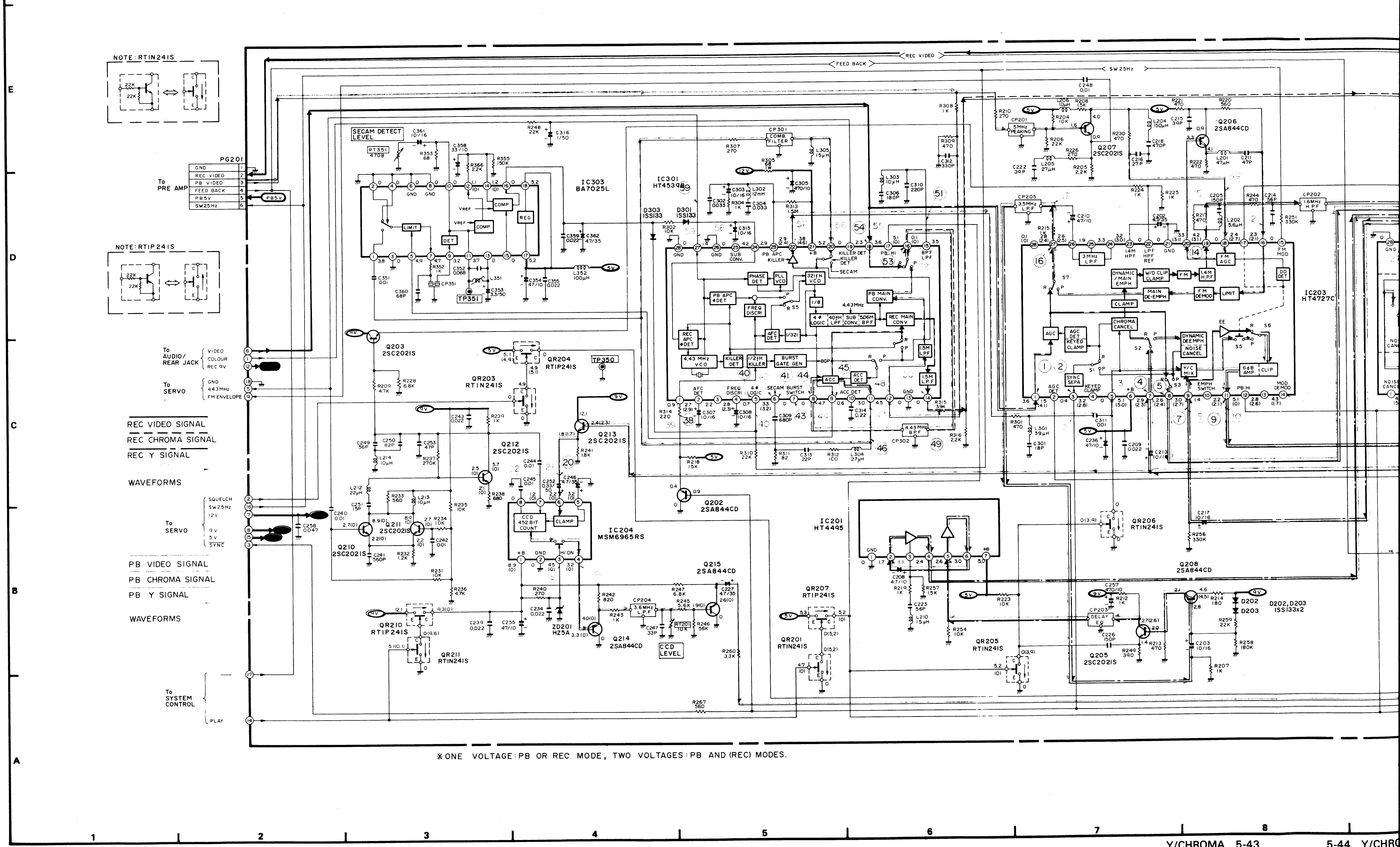

REFERENCE OSCILLATION FREQUENCY
V.LOCK
SWITCHING POINT
IC601 M54898P
IC602 M54648L-B
FWD/REV/STOP/BRAKE CONTROL
MODE DET
SPEED CONTROL
MOTOR DRIVE
REC/PB
SLOW
FF/REW
REF 25Hz
REF 25Hz COUNTER
CYL.FG 200
CTL REC AMP
V.DRIVE SEP
ASBL MM
V. DRIVE MM
STILL MM
TACH MM
CYL ADD
CYL SPEED DET
CYL PHASE DET
REF 25Hz COUNTER
PWM COUNTER
OSC
INJ
TRACK.MM
CAPST. PHASE DET
SPEED DET
SEARCH/QUICK
CAPST. ADD
FINE STILL
F. ADV
FINE SLOW
CAPST SPEED DET
PAUSE/F. ADV
CAPST ADD
C.FG AMP
1/2 Vcc
1/4
CAPST SERVO
C. FG
1/2 Vcc
PLAY
PB PAUSE
SEARCH
Q615 2SA673
ZD603 HZ18-3
ZD602 HZ7B2
Q616 2SC458
Q614 2SC458
Q613 2SD1266-PQ
ZD601 HZ7A1
D622 1SS119
QR628 RTIN441S
D652 1SS133
D653 1SS119
D609 1SS119
D610 1SS119
D651 1SS119
D619 1SS119
D620 1SS119
QR605 RTIN441S
QR602 RTIN441S
Q612 2SC458
QR601 RTIN441S
D629 1SS119
D628 1SS119
Q626 2SC458
Q627 2SC458
D623 1SS119
D640 1SS119
D645 1SS119
D631 1SS119
K607
K627
PG604
A18V
GND(M)
12V
5V
GND
A12V
+32V
-30V
A9V
To REGULATOR CN852
SELECT "Hi"
To AUDIO/ REAR JACK
PG402
A9V
A5V
-30V
+32V
To V.S TUNING PG801
PG603
REVERSE
FORWARD
GND (M)
C. FG (-)
C. FG (+)
To CAPSTAN MOTOR PG03
CAPST. 1
CAPST. 2
CAPST. 3
A5V
GND
GND (M)
To SYSTEM CONTROL
4.43MHz
To Y/CHROMA
PAUSE
F. ADV
PLAY
REVERSE
CAPST. FG
SEARCH
To SYSTEM CONTROL
NOTE: RTIN441S
47K
47K
MC-Service
4
5
6
7
8
9
10
11

※ ONE VOLTAGE: PB OR REC MODE.
TWO VOLTAGES: PB AND (REC) MODES.

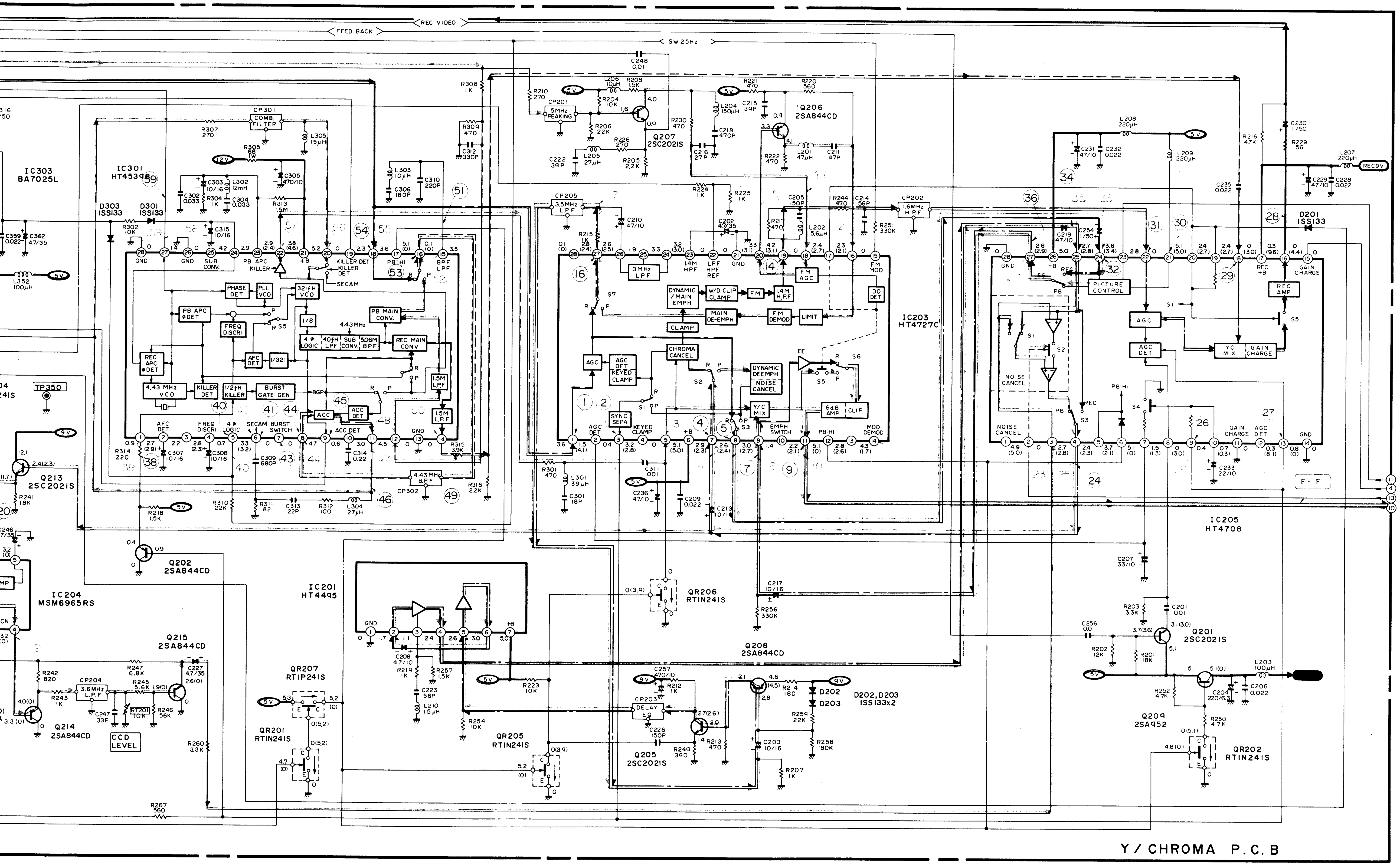
MAIN (SERVO) P. C. B

PB CAPSTAN MOTOR ◄— ○ WAVEFORM REC/PB CYLINDER MOTOR REC CYLINDER MOTOR PB CYLINDER MOTOR WAVEFORM

Y/CHROMA (LUMINANZ/CHROMINANZ)


NOTE: RTIN241S
NOTE: RTIP241S
PG201
GND
REC VIDEO
PB VIDEO
FEED BACK
PB5V
SW25Hz
To PRE AMP
To AUDIO/REAR JACK
VIDEO
COLOUR
REC 9V
To SERVO
GND
4.43MHz
FM ENVELOPE
REC VIDEO SIGNAL
REC CHROMA SIGNAL
REC Y SIGNAL
WAVEFORMS
SQUELCH
SW25Hz
12V
9V
5V
SYNC
PB VIDEO SIGNAL
PB CHROMA SIGNAL
PB Y SIGNAL
WAVEFORMS
To SYSTEM CONTROL
PLAY
FEED BACK
REC VIDEO
SW25Hz
SECAM DETECT LEVEL
IC303 BA7025L
LIMIT
DET
COMP
REG
VREF
TP351
IC301 HT4539B
D303 1SS133
D301 1SS133
CP301 COMB. FILTER
PHASE DET
PLL VCO
321fH VCO
PB APC ΦDET
FREQ DISCRI
AFC DET
1/321
1/8
4Φ LOGIC
40fH LPF
SUB CONV.
5.06M BPF
REC MAIN CONV
PB MAIN CONV.
REC APC ΦDET
4.43 MHz VCO
KILLER DET
1/2fH KILLER
BURST GATE GEN
ACC
ACC DET
1.5M LPF
KILLER DET
SECAM
PB APC KILLER
BPF LPF
CP302 4.43MHz B.P.F
Q203 2SC2021S
QR204 RTIP241S
QR203 RTIN241S
TP350
Q212 2SC2021S
Q213 2SC2021S
Q210 2SC2021S
Q211 2SC2021S
IC204 MSM6965RS
CCD 452 BIT COUNT
CLAMP
Q215 2SA844CD
Q214 2SA844CD
ZD201 HZ5A
CP204 3.6MHz L.P.F
RT201 10K
CCD LEVEL
QR210 RTIP241S
QR211 RTIN241S
Q202 2SA844CD
IC201 HT4495
QR207 RTIP241S
QR201 RTIN241S
QR205 RTIN241S
Q207 2SC2021S
CP201 5MHz PEAKING
Q206 2SA844CD
CP205 3.5MHz LPF
CP202 1.6MHz H.P.F
IC203 HT4727C
3MHz LPF
14M HPF
LPF HPF REF
FM MOD
FM AGC
1.4M H.P.F
DYNAMIC /MAIN EMPH
W/D CLIP CLAMP
FM
MAIN DE-EMPH
FM DEMOD
LIMIT
DO DET
CLAMP
AGC
AGC DET KEYED CLAMP
CHROMA CANCEL
DYNAMIC DEEMPH
NOISE CANCEL
SYNC SEPA
KEYED CLAMP
Y/C MIX
EMPH SWITCH
6dB AMP
CLIP
MOD DEMOD
QR206 RTIN241S
Q208 2SA844CD
CP203 DELAY
Q205 2SC2021S
D202
D203
D202, D203 1SS133x2

※ ONE VOLTAGE: PB OR REC MODE, TWO VOLTAGES: PB AND (REC) MODES.


REC VIDEO
FEED BACK
SW 25Hz
IC303
BA7025L
IC301
HT4539
D303
1SS133
D301
1SS133
CP301
COMB FILTER
PHASE DET
PLL VCO
32fH VCO
PB APC φDET
FREQ DISCRI
AFC DET
1/32
1/8
4φ LOGIC
40fH LPF
SUB CONV.
5.06M BPF
PB MAIN CONV.
REC MAIN CONV
REC APC φDET
4.43 MHz VCO
KILLER DET
1/2fH KILLER
BURST GATE GEN
ACC
ACC DET
1.5M LPF
4.43MHz BPF
CP302
TP350
Q213
2SC2021S
Q202
2SA844CD
IC204
MSM6965RS
Q215
2SA844CD
Q214
2SA844CD
CP204
3.6MHz L.P.F
CCD LEVEL
QR201
RTIN241S
QR207
RTIP241S
IC201
HT4495
QR205
RTIN241S
Q205
2SC2021S
CP203
DELAY
QR206
RTIN241S
Q208
2SA844CD
D202, D203
1SS133x2
Q207
2SC2021S
CP201
5MHz PEAKING
Q206
2SA844CD
CP205
3.5MHz LPF
3MHz LPF
DYNAMIC /MAIN EMPH
W/D CLIP CLAMP
FM
1.4M H.PF
FM AGC
MAIN DE-EMPH
FM DEMOD
LIMIT
DO DET
CLAMP
AGC
AGC DET KEYED CLAMP
CHROMA CANCEL
SYNC SEPA
DYNAMIC DEEMPH NOISE CANCEL
Y/C MIX
6dB AMP
CLIP
IC203
HT4727C
CP202
1.6MHz H.P.F
IC205
HT4708
PICTURE CONTROL
AGC
AGC DET
REC AMP
YC MIX
GAIN CHARGE
NOISE CANCEL
D201
1SS133
Q201
2SC2021S
Q209
2SA952
QR202
RTIN241S
REC9V
PICTURE CONT.
CURRENT UP
TRICK PLAY
VIDEO
To SYSTEM CONTROL
To AUDIO/ REAR JACK
E - E
Y / CHROMA P.C.B

MODE, TWO VOLTAGES: PB AND (REC) MODES.

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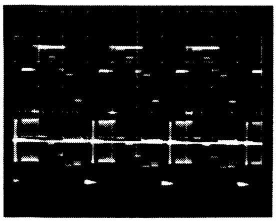
Y/CHROMA	5-42
REGULATOR	5-51
INTERNAL WIRING DIAGRAM	5-55

4 5 6 7 8 9 10 11

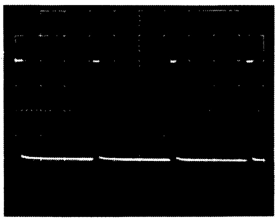
Y/CHROMA CIRCUIT WAVEFORMS (WELLENFORM)

[IC203] **(REC: Colour bar Video in/PB: Alignment tape)**

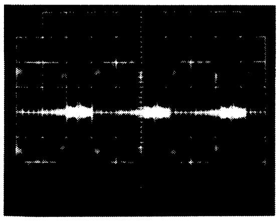
① PIN1 REC
0.1V/20μs. div.



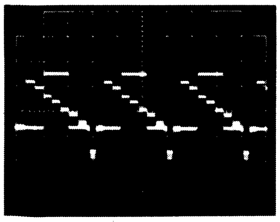
② PIN3 REC/PB
1V/20μs. div.



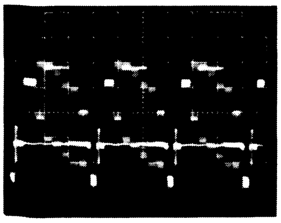
③ PIN5 PB
50mV/20μs. div.



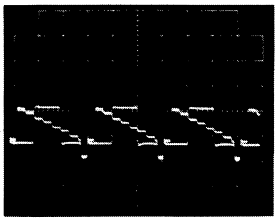
④ PIN7 REC/PB
0.1V/20μs. div.



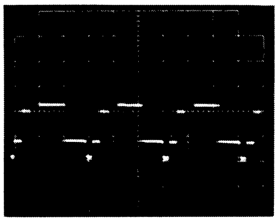
⑤ PIN8 REC
50mV/20μs. div.



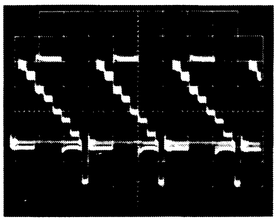
⑥ PIN8 PB
0.5V/20μs. div.



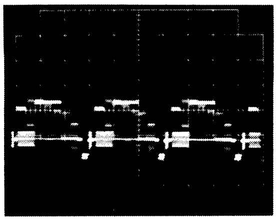
⑦ PIN9 REC
0.1V/20μs. div.



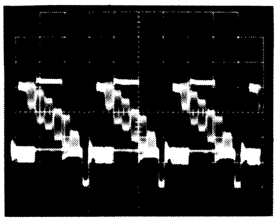
⑧ PIN9 PB
0.2V/20μs. div.



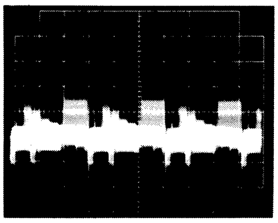
⑨ PIN11 REC
0.1V/20μs. div.



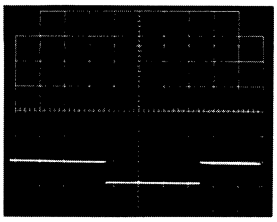
⑩ PIN11 PB
0.5V/20μs. div.



⑪ PIN14 PB
0.2V/20μs. div.

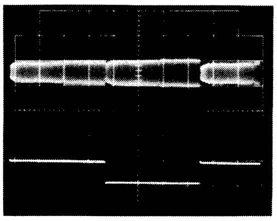


⑫ PIN16 PB
0.5V/5ms. div.



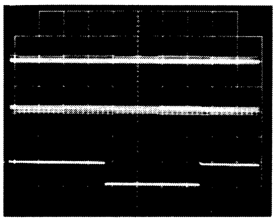
(SW25Hz: 5Vdiv.)

⑬ PIN18 PB
0.5V/5ms. div.



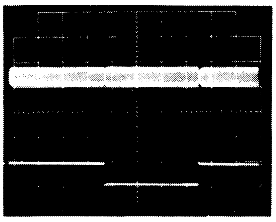
(SW25Hz: 5Vdiv.)

⑭ PIN19 REC
0.5V/5ms. div.



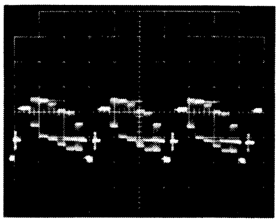
(SW25Hz: 5Vdiv.)

⑮ PIN20 PB
0.5V/5ms. div.

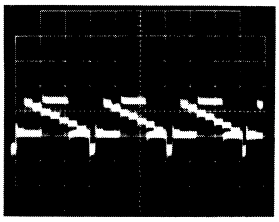


(SW25Hz: 5Vdiv.)

⑯ PIN27 REC
0.1V/20μs. div.

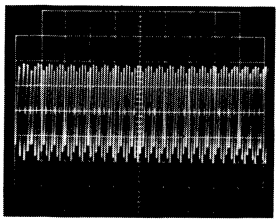


⑰ PIN27 PB
0.1V/20μs. div.

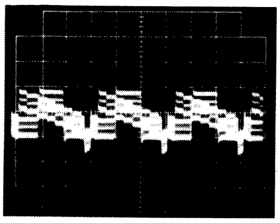


[IC204]

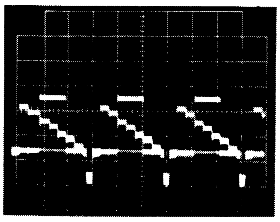
⑱ PIN3 PB
0.2V/0.5μs. div.



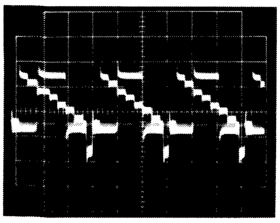
⑲ PIN4 PB
0.5V/20μs. div.



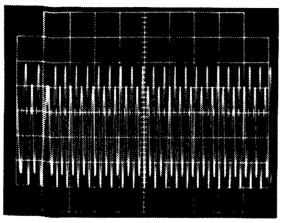
⑳ PIN6 REC
0.1V/20μs. div.



㉑ PIN6 PB
0.1V/20μs. div.

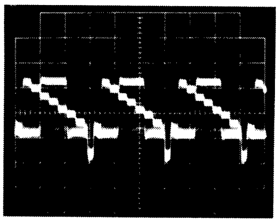


㉒ PIN7 PB
0.1V/0.5μs. div.

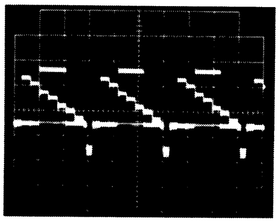


[IC205]

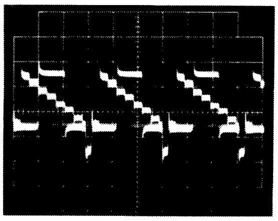
㉓ PIN3 PB
0.1V/20μs. div.



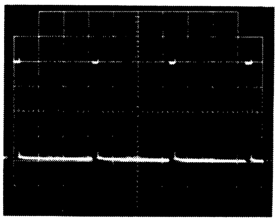
㉔ PIN 4 REC
10mV/20μs. div.



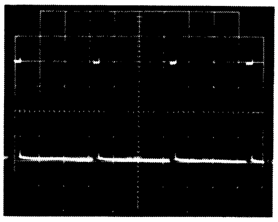
㉕ PIN4 PB
10mV/20μs. div.



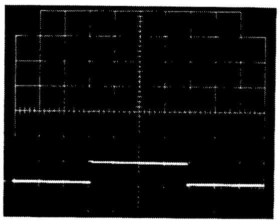
㉖ PIN9 REC/PB
1V/20μs. div.



㉗ PIN13 REC/PB
1V/20μs. div.

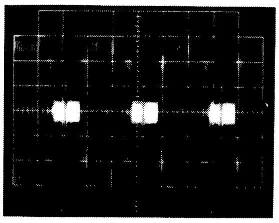


㉘ PIN16 REC
0.5V/5ms. div.

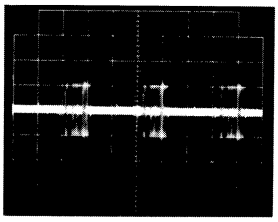


(SW25Hz: 5Vdiv.)

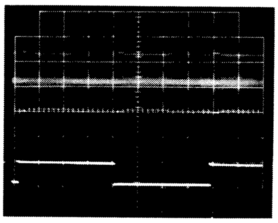
㉙ PIN18 REC
20mV/20μs. div.



㉚ PIN21 REC
50mV/20μs. div.

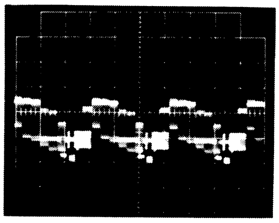


㉛ PIN22 REC
0.2V/5ms. div.

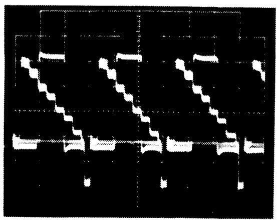


(SW25Hz: 5Vdiv.)

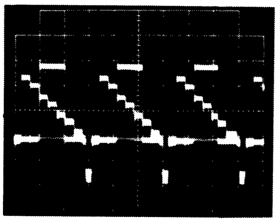
㉜ PIN24 REC
0.1V/20μs. div.



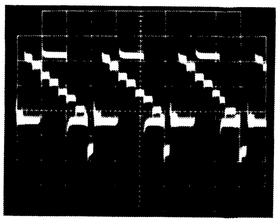
㉝ PIN24 PB
0.2V/20μs. div.



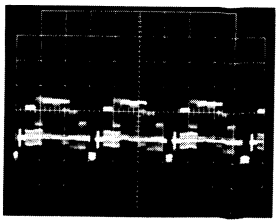
㉞ PIN25 REC
0.1V/20μs. div.



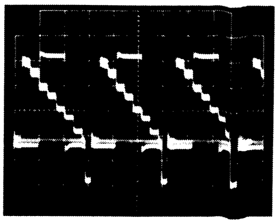
㉟ PIN25 PB
0.1V/20μs. div.



㊱ PIN27 REC
0.1V/20μs. div.

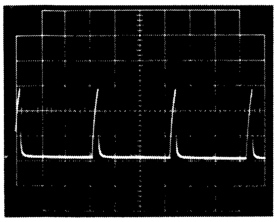


㊲ PIN27 PB
0.2V/20μs. div.

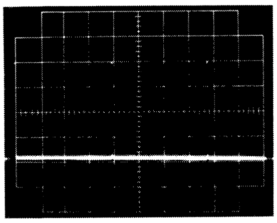


[IC301]

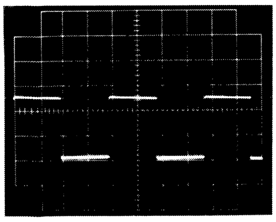
㊳ PIN1 REC
1V/20μs. div.



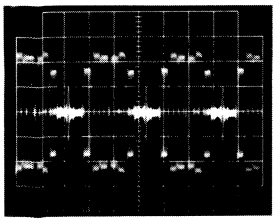
㊴ PIN1 PB
1V/0.5ms. div.



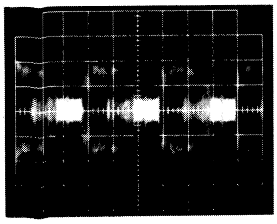
㊵ PIN5 REC/PB
0.5V/10ms. div.



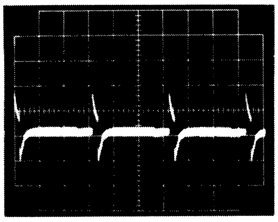
㊶ PIN6 REC
0.1V/20μs. div.



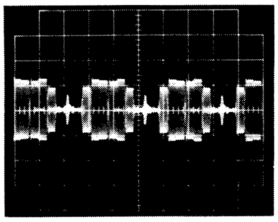
㊷ PIN6 PB
20mV/20μs. div.



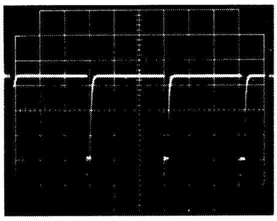
㊸ PIN7 REC/PB
0.1V/20μs. div.



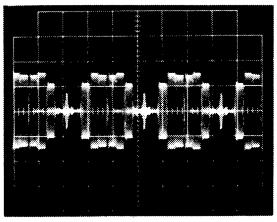
㊹ PIN8 REC/PB
50mV/20μs. div.



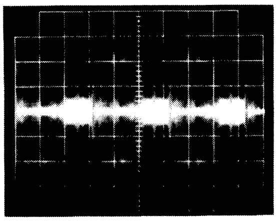
㊺ PIN9 REC/PB
1V/20μs. div.



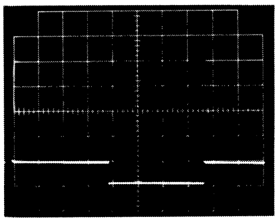
㊻ PIN11 REC
0.2V/20μs. div.



㊼ PIN11 PB
0.2V/20μs. div.

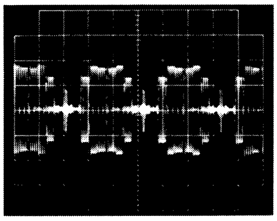


㊽ PIN12 PB
50mV/0.5ms. div.

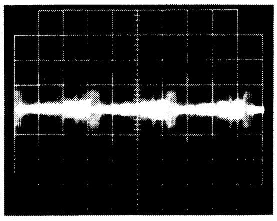


(SW25Hz: 5Vdiv.)

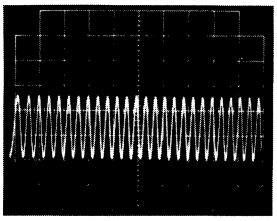
㊾ PIN14 REC
0.1V/20μs. div.



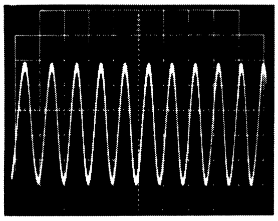
㊿ PIN14 PB
50mV/20μs. div.



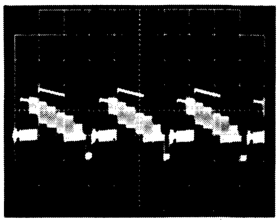
(51) PIN15 REC
0.1V/0.5μs. div.



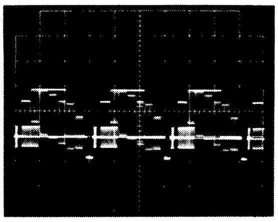
(52) PIN15 PB
50mV/0.2μs. div.



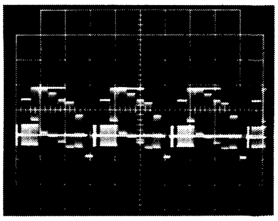
(53) PIN16 REC
0.2V/20μs. div.



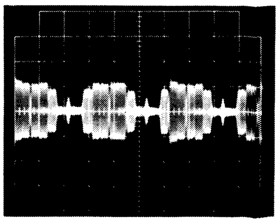
(54) PIN18 REC
0.2V/20μs. div.



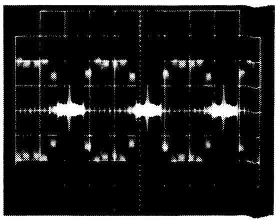
(55) PIN18 PB
0.2V/20μs. div.



(56) PIN20 PB
50mV/20μs. div.

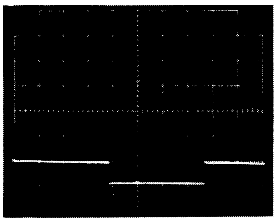


(57) PIN22 PB
0.1V/20μs. div.



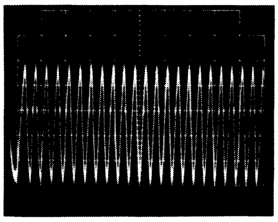
[IC301]

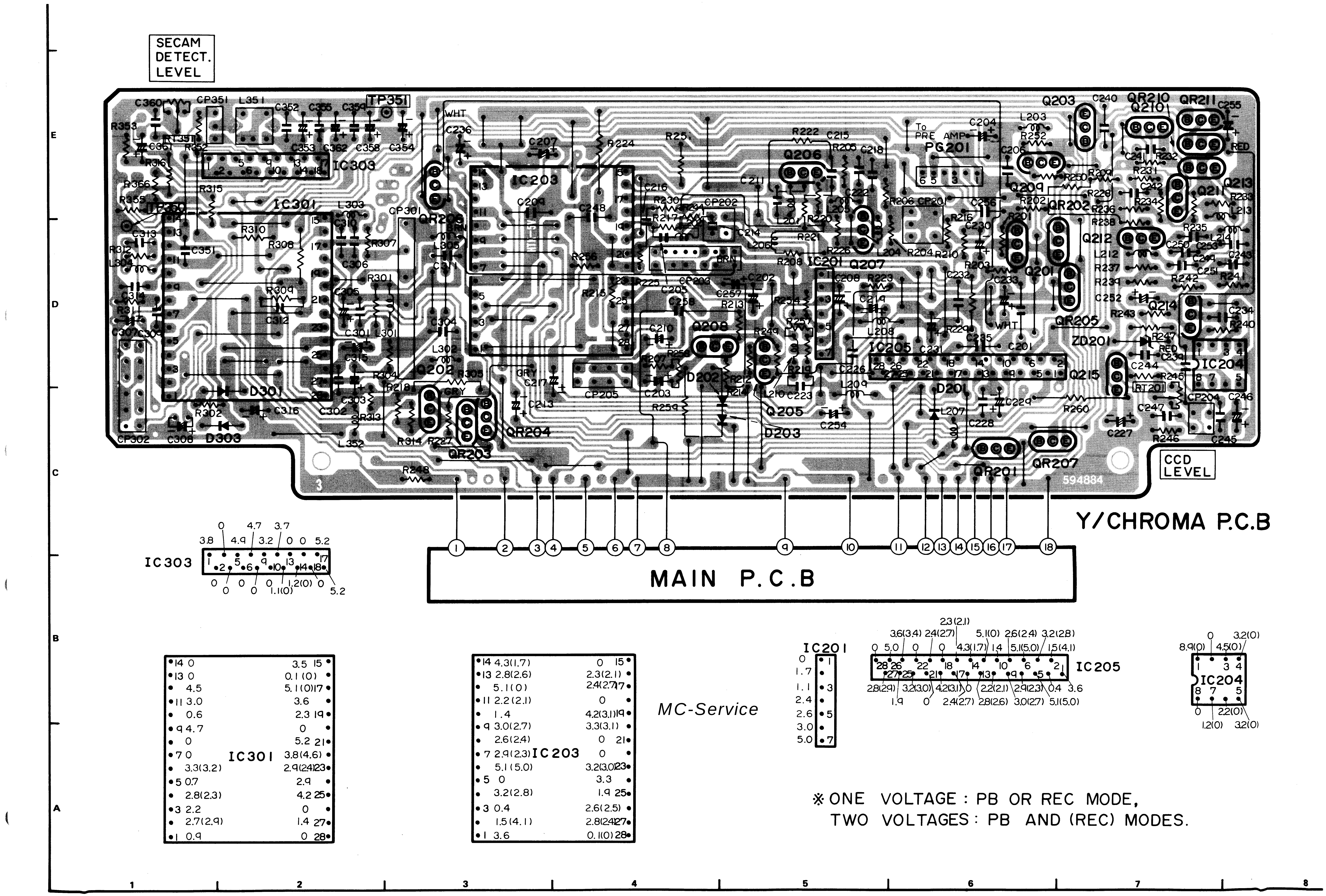
(58) PIN25 PB
0.1V/5ms. div.



(SW25Hz: 5Vdiv.)

(59) PIN27 REC/PB
50mV/0.5μs. div.

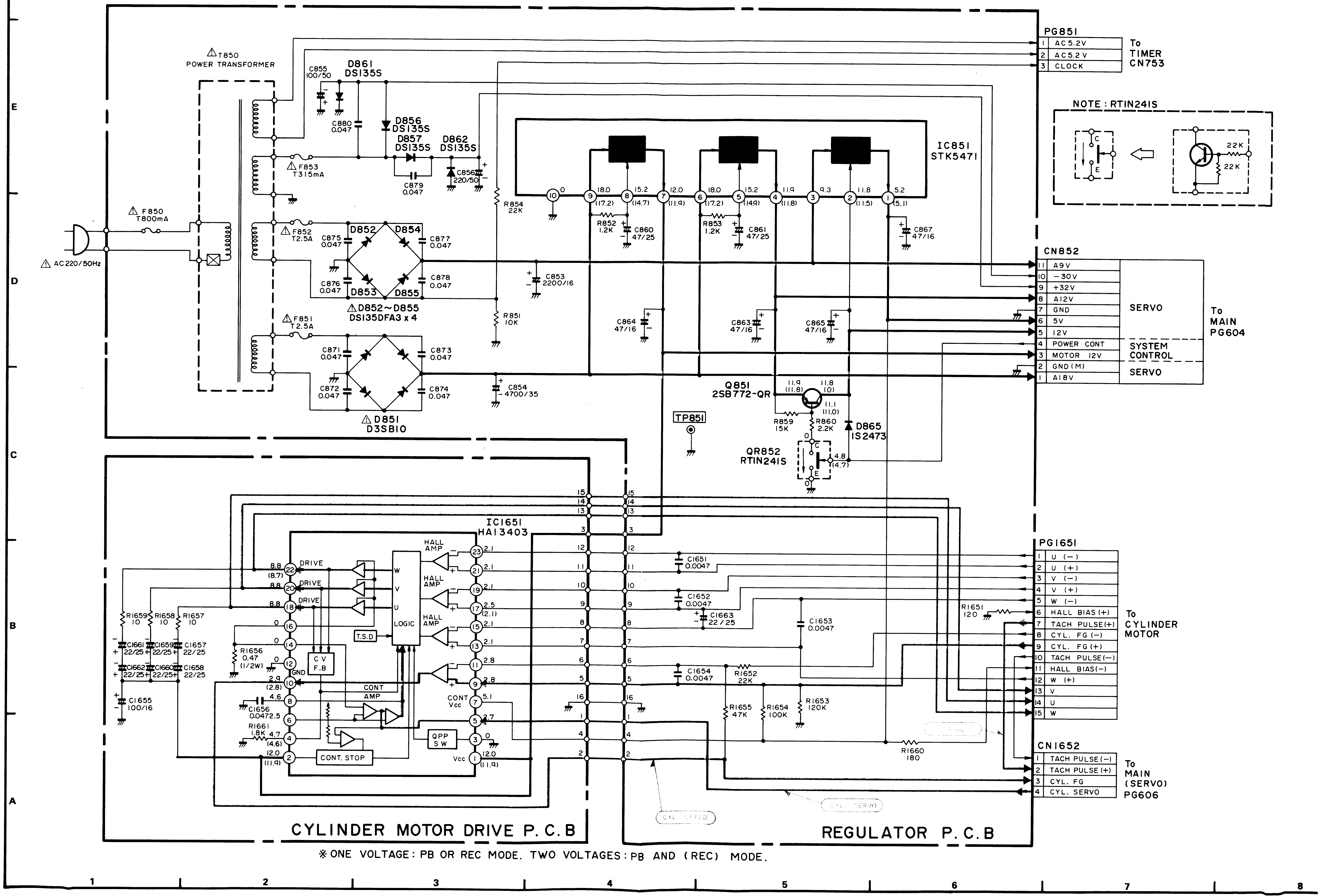



SECAM DETECT. LEVEL
CCD LEVEL
TP351
TP350
IC301
IC303
IC203
IC201
IC205
IC204
Q203
QR210
QR211
Q206
Q209
QR202
Q212
Q211
Q213
Q207
Q201
QR205
Q214
ZD201
Q208
D202
D203
Q205
D201
Q215
QR201
QR207
QR204
QR203
QR206
Q202
D301
D303
PG201
To PRE AMP
WHT
GRY
BRN
RED
594884
MAIN P.C.B
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
IC303
IC301
IC203
IC201
IC205
IC204
1 2 3 4 5 6 7 8

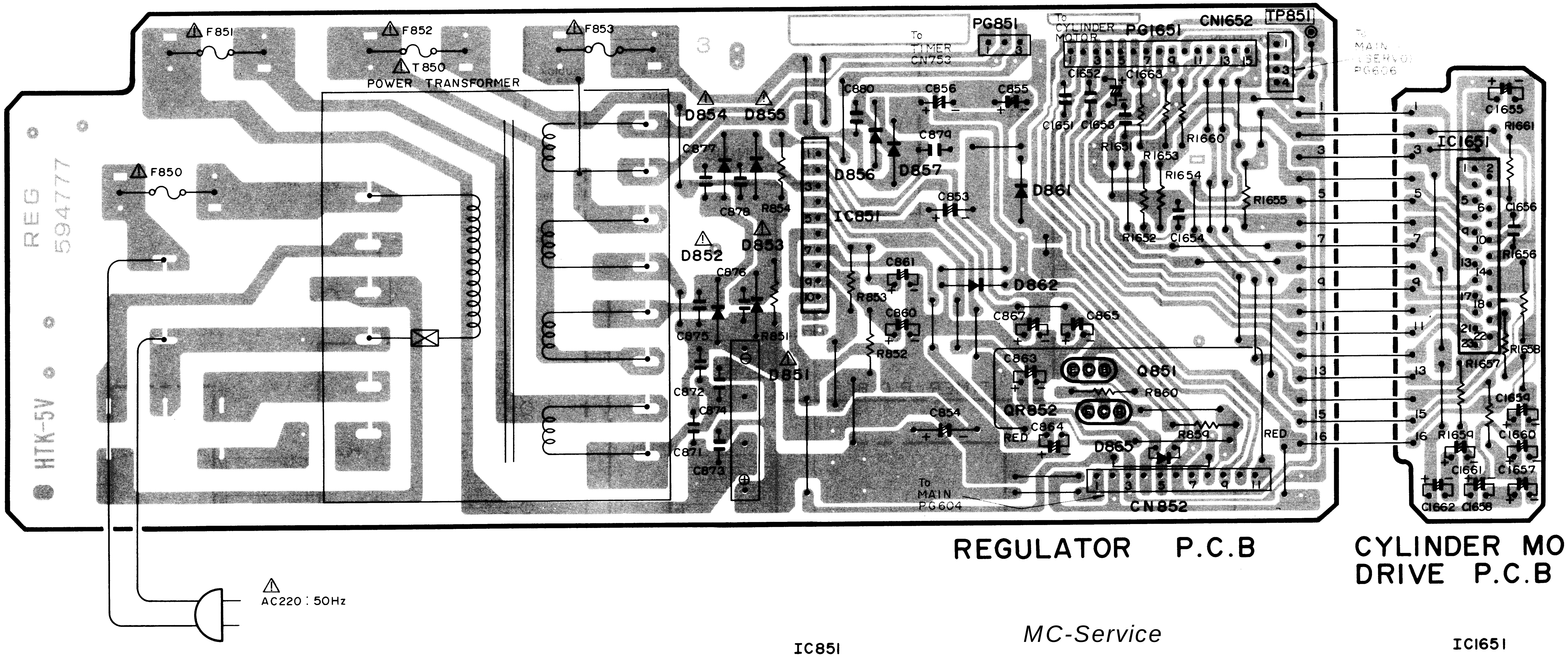
Y/CHROMA P.C.B

※ ONE VOLTAGE : PB OR REC MODE,
TWO VOLTAGES : PB AND (REC) MODES.

REGULATOR (REGLER)


T850
POWER TRANSFORMER
AC 220/50Hz
F850
T800mA
F853
T315mA
F852
T2.5A
F851
T2.5A
C855 100/50
D861 DS135S
C880 0.047
D856 DS135S
D857 DS135S
D862 DS135S
C879 0.047
C856 220/50
D852
D854
D853
D855
C875 0.047
C876 0.047
C877 0.047
C878 0.047
D852~D855 DS135DFA3 x 4
C871 0.047
C872 0.047
C873 0.047
C874 0.047
D851 D3SB10
R854 22K
R851 10K
C853 2200/16
C854 4700/35
IC851 STK5471
R852 1.2K
C860 47/25
R853 1.2K
C861 47/25
C867 47/16
C864 47/16
C863 47/16
C865 47/16
Q851 2SB772-QR
R859 15K
R860 2.2K
D865 1S2473
QR852 RTIN241S
TP851
NOTE : RTIN241S
22K
22K
PG851
1 AC5.2V
2 AC5.2V
3 CLOCK
To TIMER CN753
CN852
11 A9V
10 -30V
9 +32V
8 A12V
7 GND
6 5V
5 12V
4 POWER CONT
3 MOTOR 12V
2 GND(M)
1 A18V
SERVO
SYSTEM CONTROL
SERVO
To MAIN PG604
IC1651 HA13403
HALL AMP
DRIVE
W
V
U
LOGIC
T.S.D
CV F.B
CONT AMP
QPP SW
CONT. STOP
CONT Vcc
Vcc
GND
R1659 10
R1658 10
R1657 10
C1661 22/25
C1659 22/25
C1657 22/25
C1662 22/25
C1660 22/25
C1658 22/25
C1655 100/16
R1656 0.47 (1/2W)
C1656 0.047
R1661 1.8K
C1651 0.0047
C1652 0.0047
C1663 22/25
C1653 0.0047
C1654 0.0047
R1652 22K
R1655 47K
R1654 100K
R1653 120K
R1651 120
R1660 180
PG1651
1 U (-)
2 U (+)
3 V (-)
4 V (+)
5 W (-)
6 HALL BIAS (+)
7 TACH PULSE(+)
8 CYL. FG (-)
9 CYL. FG (+)
10 TACH PULSE(-)
11 HALL BIAS(-)
12 W (+)
13 V
14 U
15 W
To CYLINDER MOTOR
CN1652
1 TACH PULSE(-)
2 TACH PULSE(+)
3 CYL. FG
4 CYL. SERVO
To MAIN (SERVO) PG606
CYLINDER MOTOR DRIVE P.C.B
REGULATOR P.C.B
1
2
3
4
5
6
7
8
A
B
C
D
E

※ ONE VOLTAGE: PB OR REC MODE. TWO VOLTAGES: PB AND (REC) MODE.


F851
F852
F853
F850
T850
POWER TRANSFORMER
REG
594777
HTK-5V
D854
D855
D852
D853
D851
D856
D857
D861
D862
D865
IC851
IC1651
Q851
QR852
C880
C856
C855
C879
C853
C877
C878
C876
C875
C872
C874
C871
C873
C861
C860
C867
C865
C863
C864
C854
R854
R853
R851
R852
R860
R859
RED
PG851
To TIMER CN753
To CYLINDER MOTOR
PG1651
CN1652
TP851
To MAIN (SERVO) PG606
To MAIN PG604
CN852
C1652
C1663
C1651
C1653
R1651
R1653
R1660
R1654
R1655
R1652
C1654
C1655
R1661
C1656
R1656
R1658
R1657
C1659
C1660
R1659
C1661
C1657
C1662
C1658
AC220 : 50Hz

REGULATOR P.C.B

CYLINDER MOTOR DRIVE P.C.B

MC-Service

IC851

Pin	Voltage
1	5.2 (5.1)
	11.8 (11.5)
3	9.3
	11.9 (11.8)
5	15.2 (14.9)
	18.0 (17.2)
7	12.0 (11.9)
	15.2 (14.7)
9	18.0 (17.2)
10	0

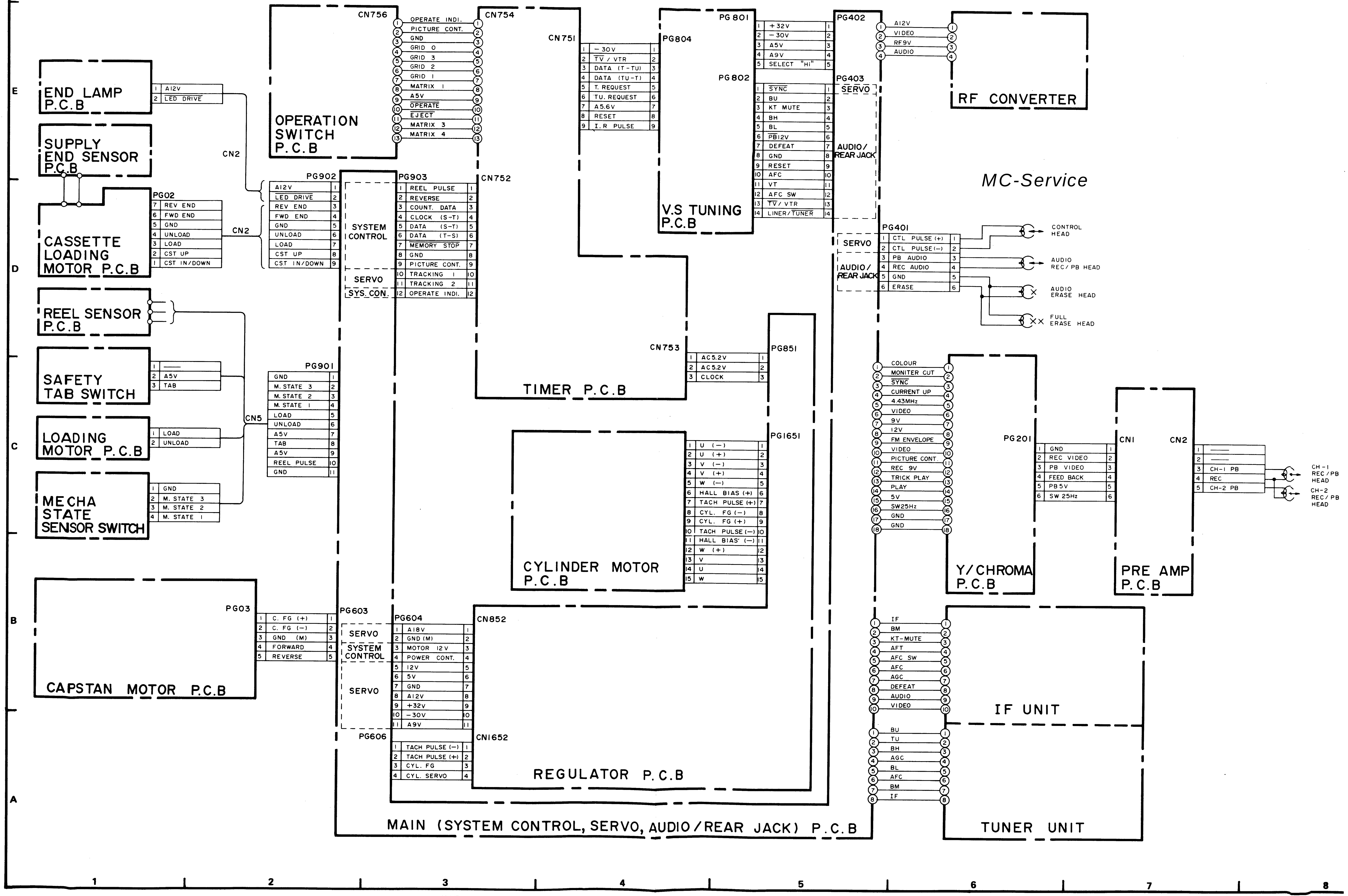
※ ONE VOLTAGE : PB OR REC MODE.
TWO VOLTAGES : PB AND (REC) MODE.

IC1651

Voltage	Pin	Pin	Voltage
12.0 (11.9)	1	2	12.0 (11.9)
0			4.7 (4.6)
2.7	5	6	2.5
5.1			4.6
2.8	9	10	2.9 (2.8)
2.8			0
2.1	13	14	0
2.1			0
2.5 (2.1)	17	18	8.8
2.1			8.8
2.1	21		8.8 (8.7)
2.1	23	22	

SCHEMATIC DIAGRAM	PAGE
TUNER UNIT	5-2
IF UNIT	5-3
V.S TUNING	5-5
TIMER/OPERATION SWITCH -VT-110E-	5-11
TIMER/OPERATION SWITCH -VT-120E-	5-14
SYSTEM CONTROL	5-20
REMOTE CONTROL	5-24
AUDIO/REAR JACK	5-26
RF CONVERTER	5-29
PREAMP	5-30
SERVO	5-39
Y/CHROMA	5-42
REGULATOR	5-51
INTERNAL WIRING DIAGRAM	5-55

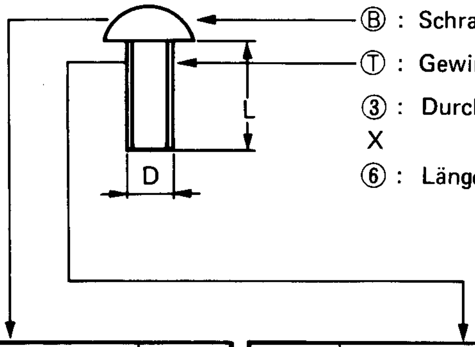
INTERNAL WIRING DIAGRAM (KABELANSCHLUSSDIAGRAMM)


E
D
C
B
A
1
2
3
4
5
6
7
8
END LAMP P.C.B
1 A12V
2 LED DRIVE
SUPPLY END SENSOR P.C.B
CN2
CASSETTE LOADING MOTOR P.C.B
PG02
7 REV END
6 FWD END
5 GND
4 UNLOAD
3 LOAD
2 CST UP
1 CST IN/DOWN
REEL SENSOR P.C.B
SAFETY TAB SWITCH
1 —
2 A5V
3 TAB
LOADING MOTOR P.C.B
1 LOAD
2 UNLOAD
MECHA STATE SENSOR SWITCH
1 GND
2 M. STATE 3
3 M. STATE 2
4 M. STATE 1
CN5
OPERATION SWITCH P.C.B
CN756
1 OPERATE INDI.
2 PICTURE CONT.
3 GND
4 GRID 0
5 GRID 3
6 GRID 2
7 GRID 1
8 MATRIX 1
9 A5V
10 OPERATE
11 EJECT
12 MATRIX 3
13 MATRIX 4
CN754
PG902
A12V 1
LED DRIVE 2
REV END 3
FWD END 4
GND 5
UNLOAD 6
LOAD 7
CST UP 8
CST IN/DOWN 9
SYSTEM CONTROL
SERVO
SYS. CON.
PG903
1 REEL PULSE
2 REVERSE
3 COUNT. DATA
4 CLOCK (S-T)
5 DATA (S-T)
6 DATA (T-S)
7 MEMORY STOP
8 GND
9 PICTURE CONT.
10 TRACKING 1
11 TRACKING 2
12 OPERATE INDI.
CN752
PG901
GND 1
M. STATE 3 2
M. STATE 2 3
M. STATE 1 4
LOAD 5
UNLOAD 6
A5V 7
TAB 8
A5V 9
REEL PULSE 10
GND 11
CN751
1 −30V
2 TV/VTR
3 DATA (T-TU)
4 DATA (TU-T)
5 T. REQUEST
6 TU. REQUEST
7 A5.6V
8 RESET
9 I.R PULSE
PG804
V.S TUNING P.C.B
PG801
1 +32V
2 −30V
3 A5V
4 A9V
5 SELECT "HI"
PG802
1 SYNC
2 BU
3 KT MUTE
4 BH
5 BL
6 PB12V
7 DEFEAT
8 GND
9 RESET
10 AFC
11 VT
12 AFC SW
13 TV/VTR
14 LINER/TUNER
PG402
1 A12V
2 VIDEO
3 RF9V
4 AUDIO
RF CONVERTER
PG403
SERVO
AUDIO/REAR JACK
PG401
SERVO
AUDIO/REAR JACK
1 CTL PULSE (+)
2 CTL PULSE (−)
3 PB AUDIO
4 REC AUDIO
5 GND
6 ERASE
CONTROL HEAD
AUDIO REC/PB HEAD
AUDIO ERASE HEAD
FULL ERASE HEAD
TIMER P.C.B
CN753
1 AC5.2V
2 AC5.2V
3 CLOCK
PG851
CYLINDER MOTOR P.C.B
PG1651
1 U (−)
2 U (+)
3 V (−)
4 V (+)
5 W (−)
6 HALL BIAS (+)
7 TACH PULSE (+)
8 CYL. FG (−)
9 CYL. FG (+)
10 TACH PULSE (−)
11 HALL BIAS' (−)
12 W (+)
13 V
14 U
15 W
1 COLOUR
2 MONITER CUT
3 SYNC
4 CURRENT UP
5 4.43MHz
6 VIDEO
7 9V
8 12V
9 FM ENVELOPE
10 VIDEO
11 PICTURE CONT.
12 REC 9V
13 TRICK PLAY
14 PLAY
15 5V
16 SW25Hz
17 GND
18 GND
Y/CHROMA P.C.B
PG201
1 GND
2 REC VIDEO
3 PB VIDEO
4 FEED BACK
5 PB5V
6 SW 25Hz
CN1
CN2
PRE AMP P.C.B
1 —
2 —
3 CH-1 PB
4 REC
5 CH-2 PB
CH-1 REC/PB HEAD
CH-2 REC/PB HEAD
CAPSTAN MOTOR P.C.B
PG03
1 C. FG (+)
2 C. FG (−)
3 GND (M)
4 FORWARD
5 REVERSE
PG603
SERVO
SYSTEM CONTROL
SERVO
PG606
PG604
1 A18V
2 GND (M)
3 MOTOR 12V
4 POWER CONT.
5 12V
6 5V
7 GND
8 A12V
9 +32V
10 −30V
11 A9V
CN852
CN1652
1 TACH PULSE (−)
2 TACH PULSE (+)
3 CYL. FG
4 CYL. SERVO
REGULATOR P.C.B
1 IF
2 BM
3 KT-MUTE
4 AFT
5 AFC SW
6 AFC
7 AGC
8 DEFEAT
9 AUDIO
10 VIDEO
IF UNIT
1 BU
2 TU
3 BH
4 AGC
5 BL
6 AFC
7 BM
8 IF
TUNER UNIT
MAIN (SYSTEM CONTROL, SERVO, AUDIO/REAR JACK) P.C.B

EXPLOSIONSZEICHNUNGEN

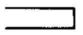
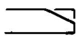
Schrauben-Klassifikation

Beispiel: BT3 x 6

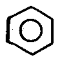


Ⓑ : Schraubenkopfart
Ⓣ : Gewindetyp
③ : Durchmesser (D)
X
⑥ : Länge (L)

Abkürzung	Bezeichnung	Form
Kein symbol	Rundkopfschraube	
P	Zylinderkopfschraube	
B	Halbrundschraube	
O	Linsenkopf-Senkschraube	
F	Senkschraube	

Abkürzung	Bezeichnung	Form
Kein symbol	Maschinenschraube	
t	Schneidschraube Typ 1 (selbstschneidend)	
T	Schneidschraube Typ 2 (selbstschneidend)	
f	Blechschraube (für Metall)	
Hinweis: Blechschrauben sind selbstschneidend; die selbstschneidenden maschinenschrauben können durch Schneidschrauben ersetzt werden.		

Unterlegescheiben und Muttern

Abkürzung	Bezeichnung	Form
W SW LW	Unterlegescheibe Federscheibe Sicherungsscheibe	
E	E-Ring	
N	Mutter	
Hinweis: Für Muttern und Scheiben werden der Innendurchmesser angegeben.		

Schmierung

Die Schmierpunkte sind in den Explosionszeichnungen durch Symbole (Ⓢ, Ⓗ) gekennzeichnet.
Die im Diagramm gezeigten Schmierpunkte sind mit folgenden Schmiermittel zu schmieren:

Ⓢ Sonic-Gleitöl (Nr. 1600)
Ⓗ Hitazol (MO-138)

MECHANICAL PARTS LIST (CABINET ASSEMBLY SECTION)

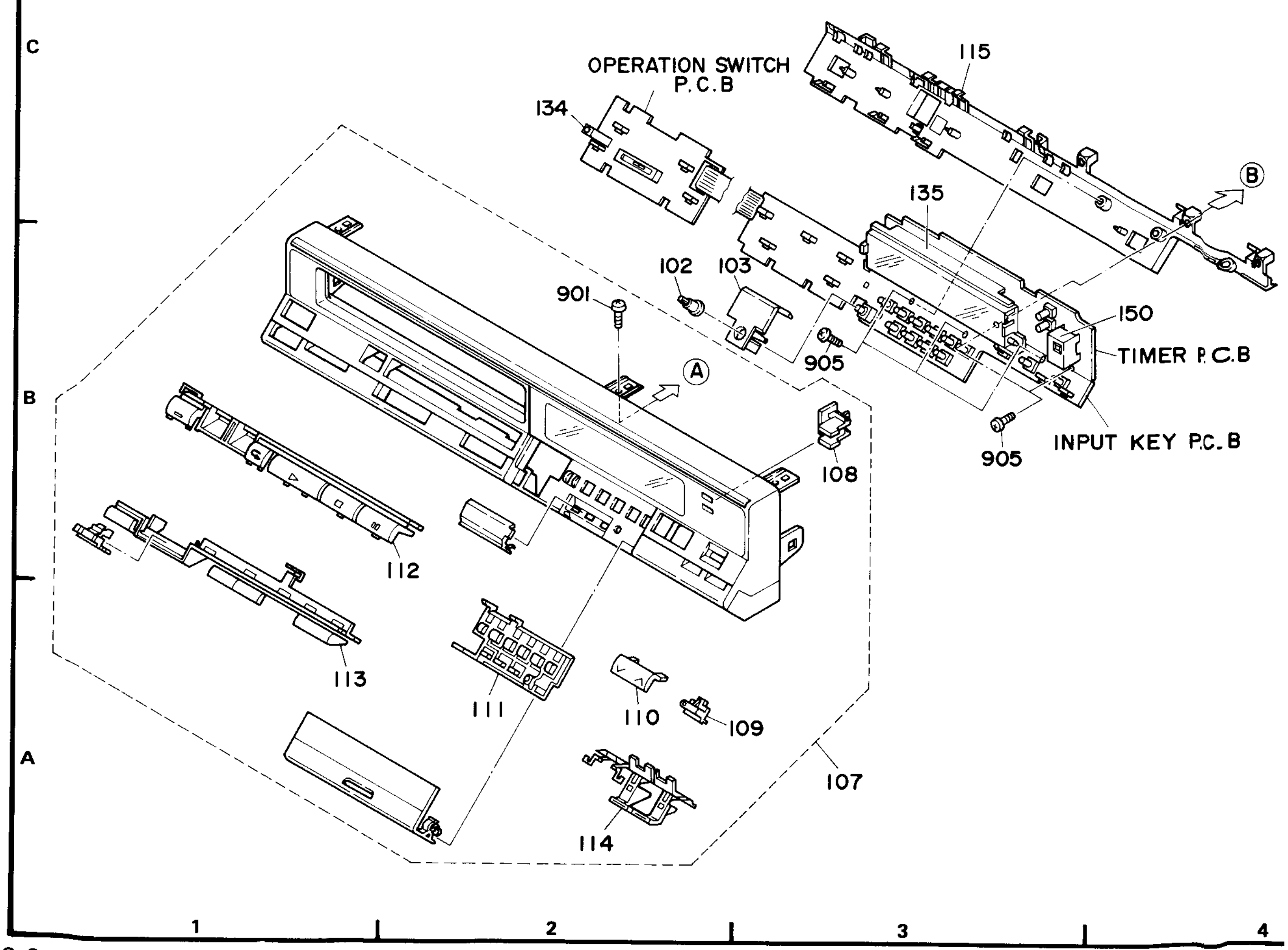
SYMBOL-NO.	P-NO.	DESCRIPTION
		FOR FINAL ASSEMBLY
101	6189398	DOOR-CASSETTE
102	6076843	KNOB - VT-110E -
102	6077031	ROTARY KNOB - VT-120E -
103	6175503	PRESET COVER - VT-110E -
103	6892333	HOLDER - VT-120E -
104	7741444	FELT (LEG)
105	6001561	BOTTOM COVER
106	6001894	TOP COVER ASSEMBLY
107	6238441	FRONT PANEL ASSEMBLY - VT-110E -
107	6238491	FRONT PANEL ASSEMBLY - VT-120E -
108	6083802	BUTTON - VT-110E -
108	6083613	BUTTON - VT-120E -
109	6083762	BUTTON - VT-110E -
109	6083572	BUTTON - VT-120E -
110	6083752	BUTTON (CHANNEL) - VT-110E -
110	6083582	BUTTON - VT-120E -
111	6083812	BUTTON - VT-110E -
111	6083603	BUTTON - VT-120E -
112	6083783	BUTTON (PLAY) - VT-110E -
112	6083892	BUTTON - VT-120E -
113	6084921	BUTTON - VT-110E -
114	6083795	BUTTON - VT-110E -
114	6083593	BUTTON - VT-120E -
115	6083832	BUTTON (POWER) - VT-110E -
115	6890461	PCB HOLDER - VT-120E -
116	6864241	CAP
117	6592111	RUBBER CAP
118	6083784	BUTTON (STOP)
119	6753911	FUSE COVER
120	6026751	REAR PANEL
123	6795152	RIVET
124	6890562	HINGE
125	6890501	STUD

MECHANICAL PARTS LIST (CABINET ASSEMBLY SECTION)

SYMBOL-NO.	P-NO.	DESCRIPTION
126	6794591	BUSHING
⚠ 127	5746157	POWER CORD WITH PLUG
⚠ 128	5213811	POWER TRANSFORMER
130	6890442	REAR PIECE – VT-110E –
130	6892513	REAR PIECE – VT-120E –
131	5658191	JACK PLATE – VT-110E –
131	5672971	JACK PLATE – VT-120E –
132	5586591	TUNER IF BLOCK
133	5587621	RF CONVERTOR
134	6875562	LED HOLDER – VT-120E –
134	6890631	LED HOLDER – VT-120E –
135	6891531	DISPLAY HOLDER
150	5490295	IR MODULE
901	8699410	BT SCREW 3MMD × 10MM BLACK
902	7784428	SCREW (M3)
903	8741406	BIND SCREW – 3MMD × 6MM
904	8691408	BT SCREW 3MMD × 8MM
905	8699410	BT SCREW 3MMD × 10MM BLACK
906	8699412	BT SCREW 3MMD × 12MM BLACK
907	8691608	SCREW 4 × 8BT

SYMBOL-NO.	P-NO.	DESCRIPTION
908	8691414	BT SCREW 3MMD × 14MM
909	8691408	BIND HEAD TAPPING SCREW 3MMD × 8MM
		FOR ACCESSORIES
801	4650102	OPERATING GUIDE – VT-110E –
801	4650272	OPERATING GUIDE – VT-120E –
802	5898876	CONNECTOR CORD
803	5638871	REMOTE HAND SET – VT-110E –
803	5638902	REMOTE CONTROL BOX – VT-120E –
		FOR CHASSIS ASSEMBLY
001	5959561	REGULATOR PCB ASSEMBLY
002	5959551	TIMER PCB ASSEMBLY – VT-110E –
003	5959471	OPERATION SWITCH PCB ASSEMBLY – VT-110E –
004	5927931	MAIN PCB ASSEMBLY
005	7094711	END LED PCB
006	7095031	REEL SENSOR PCB

CABINET SECTION (GEHÄUSEEINHEIT) – VT-120E –



SYMBOL-NO.	P-NO.	DESCRIPTION
Q808	5321214	TRANSISTOR 2SD468BC SILICON 190MHZ 0.9W
Q810	5327031	TRANSISTOR 2SA673C
Q811	5327031	TRANSISTOR 2SA673C
Q814	5323902	TRANSISTOR 2SC1740-S
Q851	5323334	TRANSISTOR 2SB772-QR
Q904	5327001	TRANSISTOR 2SC458CD
QR201	5327081	TRANSISTOR RT1N241S
QR203	5327081	TRANSISTOR RT1N241S
QR204	5327083	TRANSISTOR RT1P241S
QR205	5327081	TRANSISTOR RT1N241S
QR206	5327083	TRANSISTOR RT1P241S
QR210	5327083	TRANSISTOR RT1P241S
QR211	5327081	TRANSISTOR RT1N241S
QR432	5327082	TRANSISTOR RT1N241S
QR501	5324094	TRANSISTOR RT1P441S
QR502	5324092	TRANSISTOR RT1N441S
QR505	5324092	TRANSISTOR RT1N441S
QR506	5324092	TRANSISTOR RT1N441S
QR601	5327082	TRANSISTOR RT1N441S
QR602	5327082	TRANSISTOR RT1N441S
QR605	5327082	TRANSISTOR RT1N441S
QR628	5327082	TRANSISTOR RT1N441S
QR758	5324092	TRANSISTOR RT1N441S
QR801	5327082	TRANSISTOR RT1N441S
QR804	5327082	TRANSISTOR RT1N441S
QR812	5327082	TRANSISTOR RT1N441S
QR852	5327081	TRANSISTOR RT1N241S
ZD201	5331014	DIODE HZ5A SI ZENER
ZD601	5339105	DIODE HZ7A1
ZD602	5339101	DIODE HZ7B2
ZD603	5331271	DIODE HZ18-3
ZD751	5332633	ZENER DIODE RD4R7J B1-2
ZD752	5330322	DIODE HZ9B SI ZENER 1MHZ 0.4W
ZD753	5331588	DIODE RD2. 7E-B2
ZD801	5366151	IC UPC574J
ZD802	5339102	DIODE HZ5A
ZD803	5331274	DIODE ZENER HZ30-1

TRANSFORMERS

SYMBOL-NO.	P-NO.	DESCRIPTION
T401	5262531	BIAS COIL

COILS

SYMBOL-NO.	P-NO.	DESCRIPTION
L201	5159145	CHOKE COIL 22µH
L202	5159143	CHOKE COIL 15µH
L204	5159158	CHOKE COIL 220µH
L205	5159143	CHOKE COIL 15µH
L207	5159082	CHOKE COIL 220µH ±10%
L208	5159082	CHOKE COIL 220µH ±10%
L209	5159158	CHOKE COIL 220µH
L210	5159151	CHOKE COIL 56µH
L212	5159145	CHOKE COIL 22µH
L213	5159141	CHOKE COIL 10µH
L214	5159141	CHOKE COIL 10µH
L301	5159148	CHOKE COIL 39µH
L302	5150577	CHOKE COIL 12mH
L303	5153031	CHOKE COIL 10µH
L304	5159146	CHOKE COIL 27µH

SYMBOL-NO.	P-NO.	DESCRIPTION
L305	5159143	CHOKE COIL 15µH
L351	5120849	TRAP COIL
L352	5159077	CHOKE COIL 100µH ±10%
L401	5152349	CHOKE COIL 820µH
L403	5159111	CHOKE COIL 5600µH
L404	5152346	CHOKE COIL 5.6mH
L501	5159158	CHOKE COIL 220µH
L502	5159154	CHOKE COIL 100µH
L503	5159154	CHOKE COIL 100µH
L901	5159077	CHOKE COIL 100µH ±10%

CRYSTALS

SYMBOL-NO.	P-NO.	DESCRIPTION
X751	5781611	CRYSTAL
X801	5781121	XTAL

MISCELLANEOUS

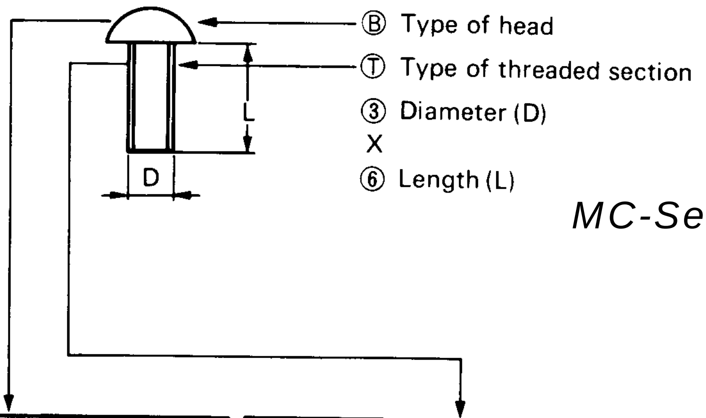
SYMBOL-NO.	P-NO.	DESCRIPTION
BZ799	5409271	BUZZER – VT120E –
CE901	5781121	XTAL
CP201	5123839	TRAP COIL
CP202	5169002	HIGH PASS FILTER
CP203	5169012	DELAY LINE
CP204	5169003	LOW PASS FILTER
CP205	5169022	LOW PASS FILTER
CP301	5785814	DELAY LINE
CP302	5163081	BAND PASS FILTER
CP351	5160431	BAND PASS FILTER
DG751	5311772	TIMER DISPLAY
⚠ F850	5720175	FUSE 0.8A
⚠ F851	5721064	FUSE 2.5A
⚠ F852	5721064	FUSE 2.5A
⚠ F853	5720171	FUSE 315MA
PD751	5490295	IR MODULE
S143	5633362	PUSH SWITCH
S144	5633362	PUSH SWITCH
S501	5622462	SLIDE SWITCH
S751	5635061	SWITCH
S752	5635061	SWITCH
S753	5635061	SWITCH
S754	5635061	SWITCH
S755	5635061	SWITCH
S756	5635061	SWITCH
S759	5635061	SWITCH
S760	5635061	SWITCH
S761	5635061	SWITCH
S762	5635061	SWITCH
S764	5635061	SWITCH
S765	5635061	SWITCH
S766	5635061	SWITCH
S768	5635061	SWITCH
S769	5635061	SWITCH
S771	5635061	SWITCH – VT-110E –
S772	5635061	SWITCH – VT-110E –
S773	5635061	SWITCH – VT-110E –
S775	5635061	SWITCH – VT-110E –
S776	5635061	SWITCH – VT-110E –
S778	5635061	SWITCH – VT-110E –
S780	5635061	SWITCH – VT-110E –
S781	5635061	SWITCH – VT-110E –
S782	5635061	SWITCH – VT-110E –
S786	5635061	SWITCH – VT-110E –

SYMBOL-NO.	P-NO.	DESCRIPTION	SYMBOL-NO.	P-NO.	DESCRIPTION
S787	5635061	SWITCH – VT-110E –	S778	5635111	SMK CONNECTOR (V-10) – VT-120E –
S771	5635111	SMK CONNECTOR (V-10) – VT-120E –	S780	5635111	SMK CONNECTOR (V-10) – VT-120E –
S772	5635111	SMK CONNECTOR (V-10) – VT-120E –	S781	5635111	SMK CONNECTOR (V-10) – VT-120E –
S773	5635111	SMK CONNECTOR (V-10) – VT-120E –	S782	5635111	SMK CONNECTOR (V-10) – VT-120E –
S774	5635111	SMK CONNECTOR (V-10) – VT-120E –	S786	5635111	SMK CONNECTOR (V-10) – VT-120E –
S775	5635111	SMK CONNECTOR (V-10) – VT-120E –	S787	5635111	SMK CONNECTOR (V-10) – VT-120E –
S776	5635111	SMK CONNECTOR (V-10) – VT-120E –	S799	5622801	SWITCH – VT-120E –

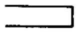
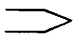
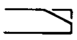
EXPLODED VIEWS

SCREW CLASSIFICATION

Example: BT3 × 6



Abbre-viation	Name	Shape
No symbol	Brazier head	
P	Pan head	
B	Binding head	
O	Oval countersunk head	
F	Flat countersunk head	

Abbre-viation	Name	Shape
No symbol	Machine (clamps without tapping)	
t	Tapping (clamps with tapping) Type 1	
T	Tapping (clamps with tapping) Type 2	
f	Forming tight (for metal)	

Note Since the forming tight screw tightens while self-tapping, machine screws can be replaced by tapping screws.

Washers and Nuts

Abbre-viation	Name	Shape
W SW LW	Washer Spring washer Locking washer	
E	E-ring	
N	Nut	

Note Internal dia is indicated for nuts and washers.

LUBRICATION

Lubrication points are shown in the exploded view diagrams by marks (Ⓢ, Ⓗ)

Lubricants shown in the diagram are as follows.

Ⓢ Sonic slider oil (# 1600)

Ⓗ Hitazol (MO-138)

SYMBOL-NO.	P-NO.	DESCRIPTION
RV751	5027225	RESISTOR VARIABLE 10KOHM
RV752	5009131	VARIABLE 500KOHM

SEMI-CONDUCTORS

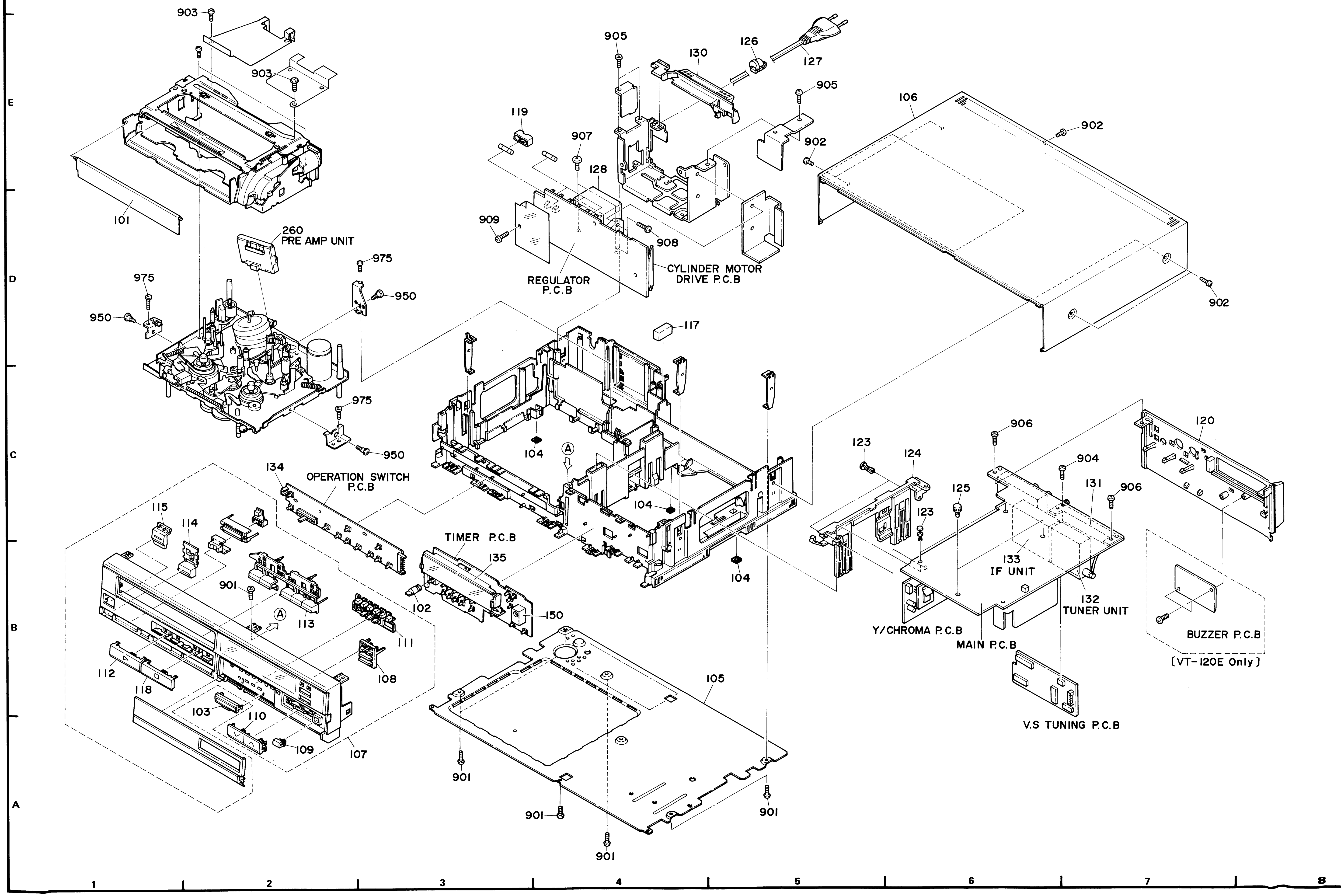
SYMBOL-NO.	P-NO.	DESCRIPTION
D201	5339071	DIODE 1SS119
D301	5339071	DIODE 1SS119
D303	5339071	DIODE 1SS119
D401	5339091	DIODE DAN209
D402	5339071	DIODE 1SS119
D502	5339071	DIODE 1SS119
D503	5339071	DIODE 1SS119
D504	5339071	DIODE 1SS119
D505	5339071	DIODE 1SS119
D506	5339071	DIODE 1SS119
D507	5339071	DIODE 1SS119
D605	5339071	DIODE 1SS119
D609	5339071	DIODE 1SS119
D610	5339071	DIODE 1SS119
D619	5339071	DIODE 1SS119
D620	5339071	DIODE 1SS119
D622	5339071	DIODE 1SS119
D623	5339071	DIODE 1SS119
D628	5339071	DIODE 1SS119
D629	5339071	DIODE 1SS119
D631	5339071	DIODE 1SS119
D640	5339071	DIODE 1SS119
D645	5339071	DIODE 1SS119
D651	5339071	DIODE 1SS119
D652	5339071	DIODE 1SS119
D653	5339071	DIODE 1SS119
D751	5339021	DIODE 1SS133
D752	5339021	DIODE 1SS133
D753	5339021	DIODE 1SS133
D754	5331592	DIODE 1SS133
D760	5331592	DIODE 1SS133
D764	5381211	LED SEL-2213C
D801	5339071	DIODE 1SS119
D802	5339071	DIODE 1SS119
D803	5339071	DIODE 1SS119
D804	5339071	DIODE 1SS119
D805	5339071	DIODE 1SS119
D806	5339071	DIODE 1SS119
⚠ D851	5332741	DIODE D3SB10
⚠ D852	5331671	DIODE DS135D-FA3
⚠ D853	5331671	DIODE DS135D-FA3
⚠ D854	5331671	DIODE DS135D-FA3
⚠ D855	5331671	DIODE DS135D-FA3
D856	5331671	DIODE DS135D-FA3
D857	5331671	DIODE DS135D-FA3
D861	5331671	DIODE DS135D-FA3
D862	5331671	DIODE DS135D-FA3
D865	5330571	DIODE 1S2473VE SI 100MHZ 250MW 10NS
D903	5339071	DIODE 1SS119
D904	5339071	DIODE 1SS119
D914	5339071	DIODE 1SS119
IC201	5370821	IC HT4495
IC203	5370844	IC HT4727
IC204	5362262	IC MSM6965RS
IC205	5370502	IC HT4408
IC301	5370273	IC HT4539B
IC303	5366641	IC BA7025L
IC401	5366331	IC UPC1533HA
IC402	5364931	IC BA5115L
IC403	5369431	IC LA7016
IC501	5369431	IC LA7016
IC601	5367301	IC M54898P
IC602	5369913	IC M54648L-B
IC751	5361996	IC HD614045SD53
IC801	5361834	IC M50161-354SP
IC802	5366132	IC LA7934
IC803	5361071	IC M58657P
IC804	5721802	ICP-N5 IC PROTECTOR
IC805	5721802	ICP-N5 IC PROTECTOR
IC851	5353651	IC STK5471
IC901	5361812	IC HD614042SD37
IC902	5367111	IC M54649L
IC903	5365673	IC NJM2901N
IC1651	5355582	IC HA13403
Q141	5381681	TRANSISTOR PT-23F-F PHOTO
Q142	5381682	TRANSISTOR PT-23F-HLD PHOTO
Q201	5327062	TRANSISTOR 2SC1740S
Q202	5321255	TRANSISTOR 2SA844CD SILICON 200MHZ 0.3W
Q203	5321292	TRANSISTOR 2SC1740S SILICON 250MHZ 0.3W
Q205	5327062	TRANSISTOR 2SC1740S
Q206	5327062	TRANSISTOR 2SC1740S
Q207	5327062	TRANSISTOR 2SC1740S
Q208	5321255	TRANSISTOR 2SA844CD
Q209	5322732	TRANSISTOR 2SA952ML2 SILICON 160MHZ 0.6W
Q210	5327062	TRANSISTOR 2SC1740S
Q211	5327062	TRANSISTOR 2SC1740S
Q212	5327062	TRANSISTOR 2SC1740S
Q213	5327062	TRANSISTOR 2SC1740S
Q214	5321255	TRANSISTOR 2SA844CD SILICON 200MHZ 0.3W
Q215	5321255	TRANSISTOR 2SA844CD SILICON 200MHZ 0.3W
Q401	5327101	TRANSISTOR 2SC3553BC
Q402	5327031	TRANSISTOR 2SA673C
Q431	5327031	TRANSISTOR 2SA673C
Q502	5327031	TRANSISTOR 2SA673C
Q504	5322732	TRANSISTOR 2SA952ML2 SILICON 160MHZ 0.6W
Q611	5327001	TRANSISTOR 2SC458CD
Q612	5327001	TRANSISTOR 2SC458CD
Q613	5323461	TRANSISTOR 2SD1266PQ
Q614	5327001	TRANSISTOR 2SC458CD
Q615	5327031	TRANSISTOR 2SA673C
Q616	5327001	TRANSISTOR 2SC458CD
Q626	5327001	TRANSISTOR 2SC458CD
Q627	5327001	TRANSISTOR 2SC458CD
Q751	5321663	TRANSISTOR 2SC2021RS SILICON 180MHZ 0.3W
Q754	5321663	TRANSISTOR 2SC2021RS SILICON 180MHZ 0.3W
Q755	5321663	TRANSISTOR 2SC2021RS SILICON 180MHZ 0.3W
Q802	5327011	TRANSISTOR 2SC1740RS
Q803	5327001	TRANSISTOR 2SC458CD

REPLACEMENT PARTS LIST (ERSATZTEILLISTE)

ELECTRICAL PARTS LIST

SYMBOL-NO.	P-NO.	DESCRIPTION
	CAPACITORS	
C201	0208374	CERAMIC DISC 0.01μF ±20% 50V
C204	0256608	ELECTROLYTIC 220μF 6.3V
C208	0256613	ELECTROLYTIC 4.7μF 35V
C209	0208375	CERAMIC DISC 0.022μF ±10% 50V
C211	0208357	CERAMIC DISC 56pF ±5% 50V
C214	0208360	CERAMIC DISC 100pF ±5% 50V
C217	0256613	ELECTROLYTIC 4.7μF 35V
C218	0208363	CERAMIC DISC 330 pF ±10% 50V
C222	0208352	CERAMIC DISC 22pF 50V
C223	0208360	CERAMIC DISC 100pF ±5% 50V
C228	0208375	CERAMIC DISC 0.022μF ±10% 50V
C232	0208375	CERAMIC DISC 0.022μF ±10% 50V
C234	0208375	CERAMIC DISC 0.022μF ±10% 50V
C236	0207085	ELECTROLYTIC 47MF, 10V
C240	0208374	CERAMIC DISC 0.01μF ±20% 50V
C241	0249592	CERAMIC DISC 560pF ±10% 50V
C242	0208374	CERAMIC DISC 0.01μF ±20% 50V
C244	0208374	CERAMIC DISC 0.01μF ±20% 50V
C245	0208374	CERAMIC DISC 0.01μF ±20% 50V
C248	0208374	CERAMIC DISC 0.01μF ±20% 50V
C249	0208357	CERAMIC DISC 56pF 50V
C250	0208364	CERAMIC DISC 82pF 50V
C251	0208350	CERAMIC DISC 15pF ±5% 50V
C253	0208356	CERAMIC DISC 47pF 50V
C254	0207064	ELECTROLYTIC 1MF, 50V
C255	0207085	ELECTROLYTIC 47MF, 10V
C256	0208374	CERAMIC DISC 0.01μF ±20% 50V
C301	0208351	CERAMIC DISC 18pF 50V
C309	0208365	CERAMIC DISC 680pF ±10% 50V
C313	0208352	CERAMIC DISC 22pF 50V
C351	0208374	CERAMIC DISC 0.01μF ±20% 50V
C355	0208375	CERAMIC DISC 0.022μF ±10% 50V
C360	0208358	CERAMIC DISC 68pF ±5% 50V
C416	0208367	CERAMIC DISC 1000pF ±10% 50V
C423	0208374	CERAMIC DISC 0.01μF ±20% 50V
C425	0207092	ELECTROLYTIC 100μF 16V
C426	0208374	CERAMIC DISC 0.01μF ±10% 50V
C428	0208365	CERAMIC DISC 680pF ±10% 50V
C502	0208374	CERAMIC DISC 0.01μF ±20% 50V
C506	0208374	CERAMIC DISC 0.01μF ±20% 50V
C508	0208374	CERAMIC DISC 0.01μF ±20% 50V
C510	0208374	CERAMIC DISC 0.01μF ±20% 50V
C512	0208374	CERAMIC DISC 0.01μF ±20% 50V
C513	0256789	CAPACITOR 470μF 10V ELECTROLYTIC
C522	0207086	CAPACITOR 47μF 16V ELECTROLYTIC
C523	0208374	CERAMIC DISC 0.01μF ±20% 50V
C524	0256782	ELECTROLYTIC 220μF 10V
C527	0208374	CERAMIC DISC 0.01μF ±20% 50V
C529	0208374	CERAMIC DISC 0.01μF ±20% 50V
C604	0208374	CERAMIC DISC 0.01μF ±20% 50V
C605	0208375	CERAMIC DISC 0.022μF ±20% 50V
C607	0208368	CERAMIC DISC 1500pF ±20% 50V
C608	0208365	CERAMIC DISC 680pF ±10% 50V
C616	0208367	CERAMIC DISC 1000pF ±10% 50V
C618	0208375	CERAMIC DISC 0.022 μF ±10% 50V
C620	0208375	CERAMIC DISC 0.022μF ±10% 50V
C621	0208374	CERAMIC DISC 0.01μF ±20% 50V
C624	0208374	CERAMIC DISC 0.01μF ±20% 50V
C637	0208375	CERAMIC DISC 0.022μF ±10% 50V
C638	0208374	CERAMIC DISC 0.01μF ±20% 50V
C641	0256475	TANTALUM 4.7μF ±30% 10V
C642	0208374	CERAMIC DISC 0.01μF ±20% 50V
C644	0208367	CERAMIC DISC 1000pF ±10% 50V
C653	0208360	CERAMIC DISC 100pF ±5% 50V
C751	0256488	CAPACITOR 0.1F 5.5V
C770	5058562	TRIMMER 22pF
C801	0208357	CERAMIC DISC 56pF ±5% 50V
C815	0208360	CERAMIC DISC 100pF ±5% 50V
C816	0208354	CERAMIC DISC 33pF ±5% 50V
C817	0208354	CERAMIC DISC 33pF ±5% 50V
C825	0256180	CAPACITOR 1μF 50V ELECTROLYTIC
C854	0256657	ELECTROLYTIC 4700μF 35V
C856	0256635	ELECTROLYTIC 220μF 50V
C860	0256607	ELECTROLYTIC 47μF 25V
C861	0256607	ELECTROLYTIC 47μF 25V
C863	0256627	ELECTROLYTIC 47MF, 16V
C864	0256627	ELECTROLYTIC 47MF, 16V
C865	0256627	ELECTROLYTIC 47MF, 16V
C867	0256627	ELECTROLYTIC 47MF, 16V
C901	0208374	CERAMIC DISC 0.01μF ±20% 50V
C902	0208375	CERAMIC DISC 0.022μF ±20% 50V
C903	0208375	CERAMIC DISC 0.022μF ±20% 50V
C904	0208374	CERAMIC DISC 0.01μF ±20% 50V
C906	0208374	CERAMIC DISC 0.01μF ±20% 50V
C907	0208375	CERAMIC DISC 0.022μF ±20% 50V
C908	0208374	CERAMIC DISC 0.01μF ±20% 50V
C909	0208354	CERAMIC DISC 33pF ±5% 50V
C910	0208354	CERAMIC DISC 33pF ±5% 50V
C912	0208374	CERAMIC DISC 0.01μF ±20% 50V
C913	0208374	CERAMIC DISC 0.01μF ±20% 50V
C1657	0256618	ELECTROLYTIC 22μF 25V
C1658	0256618	ELECTROLYTIC 22μF 25V
C1659	0256618	ELECTROLYTIC 22μF 25V
C1660	0256618	ELECTROLYTIC 22μF 25V
C1661	0256618	ELECTROLYTIC 22μF 25V
C1662	0256618	ELECTROLYTIC 22μF 25V
C1663	0256618	ELECTROLYTIC 22μF 25V
	RESISTORS	
R215	0170348	CARBON FILM 470OHM ±5% 1/8W
R305	0171015	METAL FILM 68OHM ±5% 1W
R602	0249681	POSISTOR 4.7OHM
RT201	5007435	RESISTOR SEMI VARIABLE 10KOHM
RT351	5007431	RESISTOR SEMI VARIABLE 470OHM
RT401	5007899	SEMI VARIABLE 47KOHM
RT402	5007901	SEMI VARIABLE 100KOHM
RT501	5009142	RESISTOR VARIABLE 50KOHM
RT601	5007899	SEMI VARIABLE 47KOHM
RT607	5007902	SEMI VARIABLE 220KOHM

CABINET SECTION (GEHÄUSEEINHEIT) – VT-110E –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PRE AMP UNIT
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902
119
907
128
909
908
REGULATOR
P.C.B
CYLINDER MOTOR
DRIVE P.C.B
117
104
Ⓐ
104
104
134
OPERATION SWITCH
P.C.B
115
114
901
Ⓐ
113
111
108
112
118
103
110
109
107
102
TIMER P.C.B
135
150
105
901
901
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901
123
124
125
123
906
904
131
906
120
133
IF UNIT
132
TUNER UNIT
Y/CHROMA P.C.B
MAIN P.C.B
BUZZER P.C.B
(VT-120E Only)
V.S TUNING P.C.B
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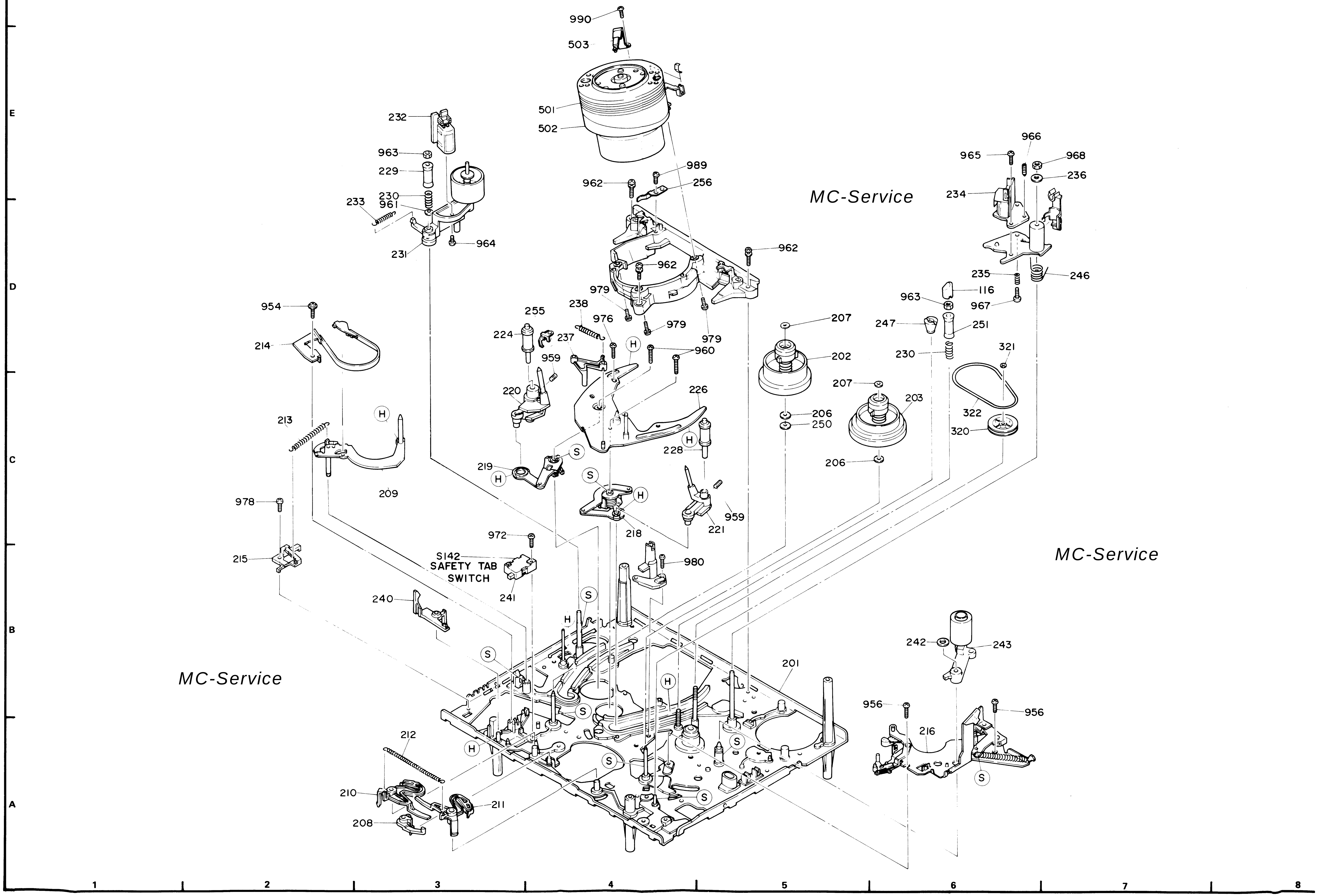
CHASSIS (I) SECTION (CHASSIS [I])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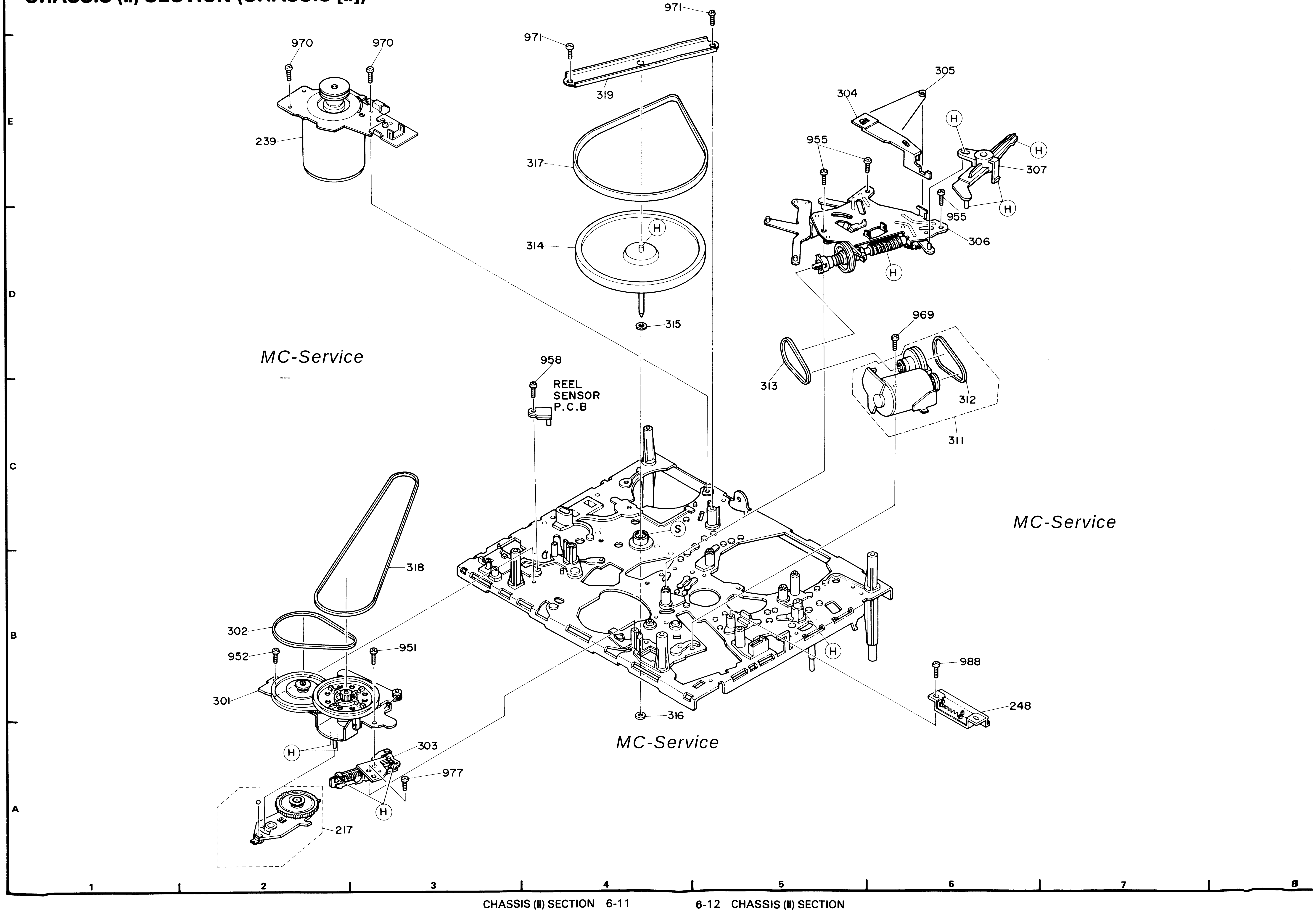
CHASSIS (II) SECTION (CHASSIS [II])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969
958
REEL
SENSOR
P.C.B
313
312
311
S
318
302
952
951
H
988
301
248
316
H
303
977
H
217
E
D
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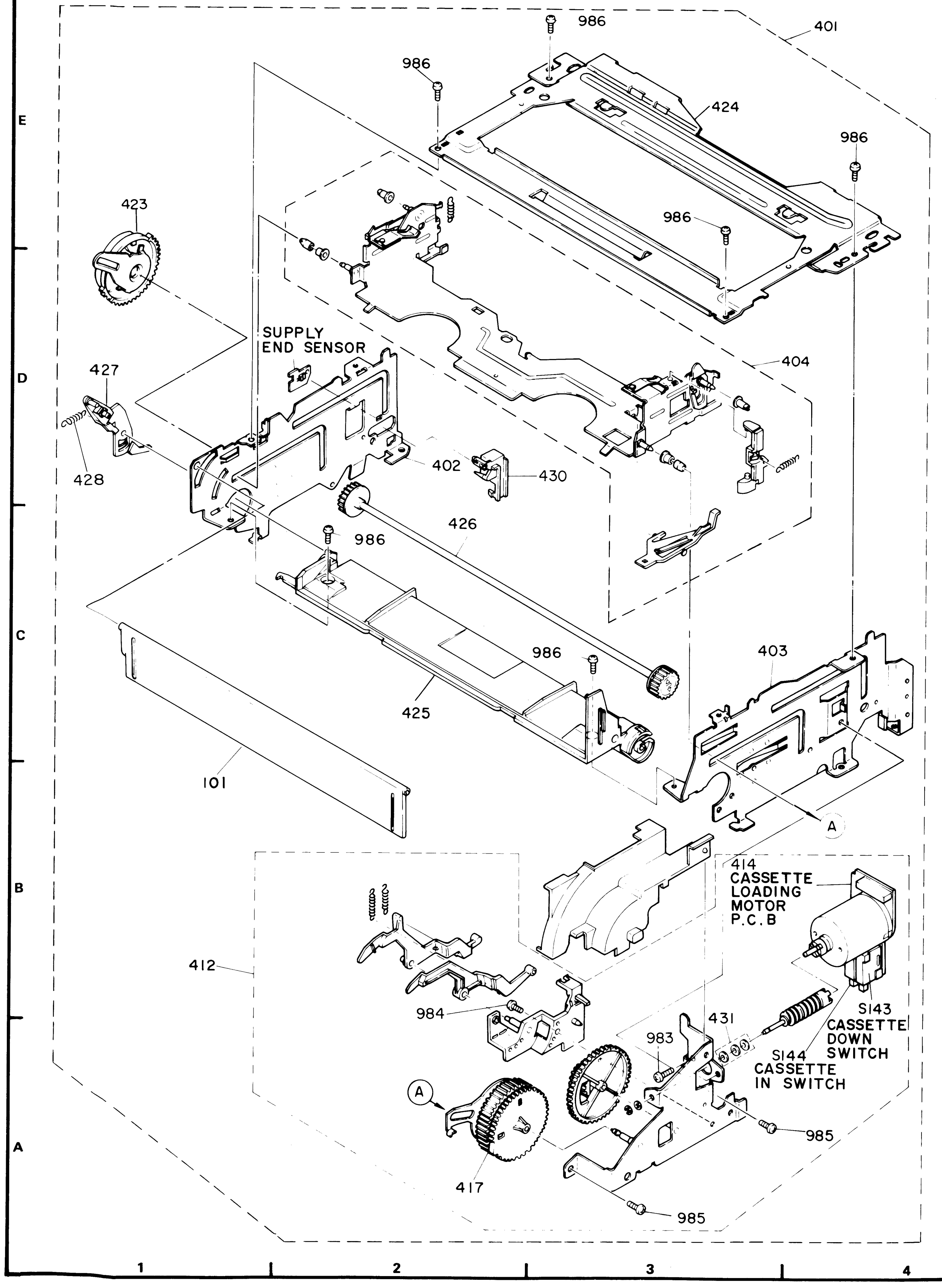
CASSETTE LOADING MECHANISM SECTION (CASSETTEN-LADEMECHANISMUS)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401
424
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423
SUPPLY END SENSOR
404
427
428
402
430
426
986
986
403
425
101
A
412
414 CASSETTE LOADING MOTOR P.C.B
984
431
983
S143 CASSETTE DOWN SWITCH
S144 CASSETTE IN SWITCH
A
985
417
985
E
D
C
B
A
1
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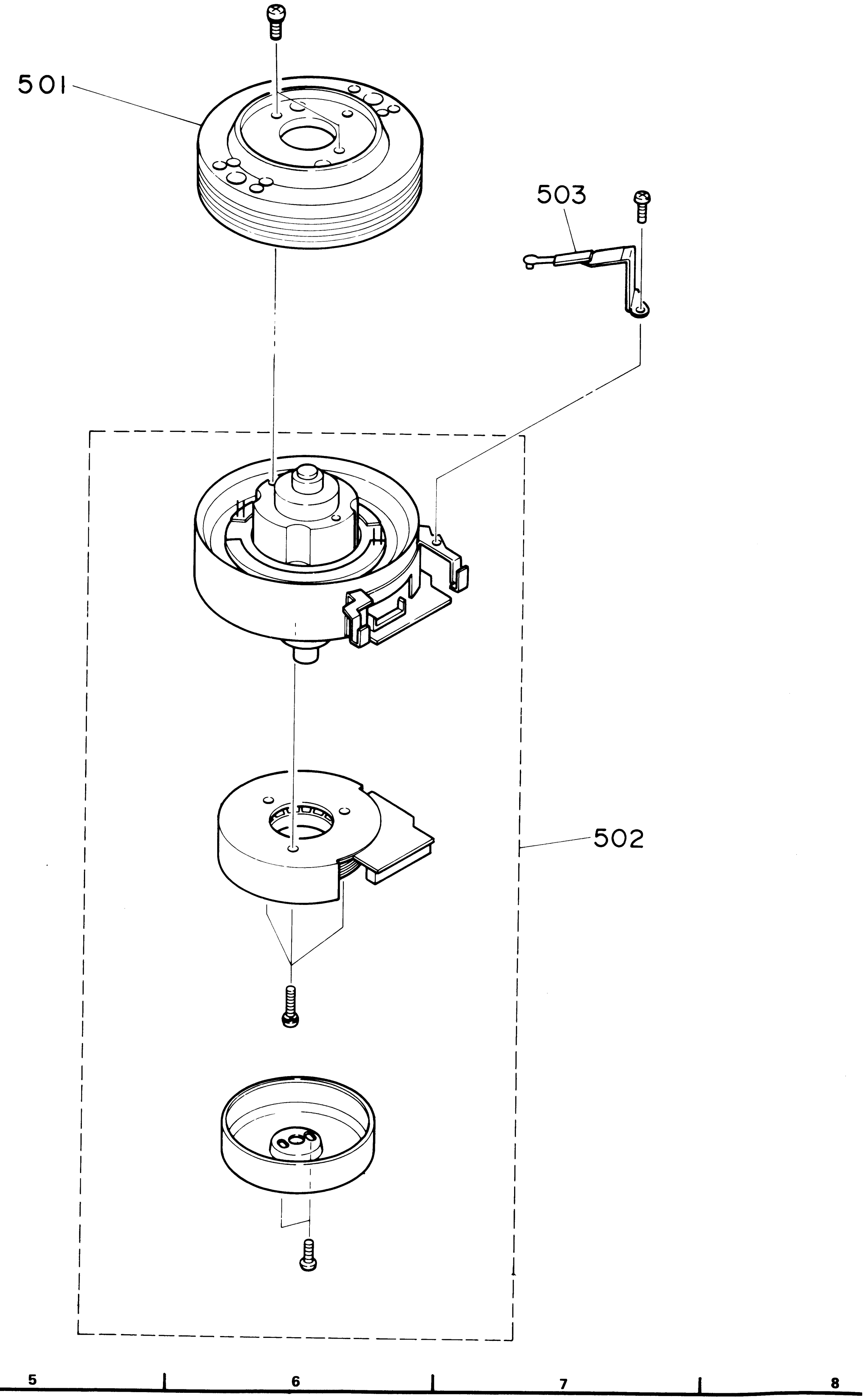
3
4

CYLINDER MOTOR SECTION (KOPFTROMMELMOTOR)


501
503
502
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8

MECHANICAL PARTS LIST (CHASSIS/CASSETTE LOADING MECHANISM/CYLINDER MOTOR ASSEMBLY SECTION)

SYMBOL-NO	P-NO	DESCRIPTION
		FOR FINAL ASSEMBLY
202	6415391	REEL TABLE-SUPPLY
203	6415412	REEL TABLE-TAKE UP
206	7787412	WASHER
207	7778859	POLYSLIDER WASHER
208	6865662	ARM-BRAKE
209	7386841	TENSION ARM
210	6865804	BRAKE L
211	6865812	BRAKE R
212	6302471	SPRING
213	6543864	SPRING
214	7376271	TENSION BAND
215	6879421	BT.SPRING HOLDER
216	7386882	ARM BRACKET
217	6886792	ARM
218	7376303	LOADING LINK (RIGHT) ASSEMBLY
219	7376313	LOADING LINK (LEFT) ASSEMBLY
220	6978301	GUIDE ROLLER BASE (I)
221	6974661	BASE
224	6869481	GUIDE ROLLER
226	7386892	GUIDE BASE HOLDER
228	6868061	GUIDE ROLLER ASSEMBLY (OUT)
229	7570671	TAPE GUIDE (I)
230	6304903	SPRING
231	6879902	IMPEDANCE ARM ASSEMBLY
232	5446151	FULL ERASE HEAD
233	6302391	SPRING
234	5446161	AUDIO CONTROL HEAD
235	6304906	SPRING
236	7786245	WASHER
237	6878932	SUB BRAKE
238	6300084	SPRING
239	5578761	MOTOR-CAPSTAN
240	6865675	RECORDING PREVENTION ARM
241	5633971	SWITCH (S142)
242	7788143	POLYSLIDER WASHER
243	6979842	PRESSURE ROLLER ASSEMBLY
246	6547811	SPRING
247	6979042	SCREW
248	5625141	SWITCH
250	6873291	COLLAR
251	4504401	TAPE GUIDE
255	6877521	COLLAR
256	6539101	SPRING
260	5372041	PRE AMP PCB ASSEMBLY
301	6886824	CLUCH PLATE ASSEMBLY
302	6355561	BELT
303	7386971	SLIDER-BRAKE
304	6865733	MODE SLIDER
305	6547821	SPRING
306	6889552	GEAR
307	6865791	TENTION ARM
311	7386931	MOTOR(DC) 3.7W 65G LOADING
312	6356111	BELT
313	6356451	BELT
314	6375031	FLYWHEEL
315	7788142	POLYSLIDER WASHER (THRUST)
316	7788861	WASHER
317	6356101	BELT
318	6356081	BELT
319	7386833	PLATE
320	6869291	PULLEY
321	7778859	POLYSLIDER WASHER
322	6355561	BELT
401	7397052	FRONT LOADING ASSEMBLY
402	7386744	BRACKET
403	7386701	BRACKET(R)
404	7386813	HOLDER-CASSETTE
412	7394493	BRACKET-MOTOR
414	5946911	MOTOR CBA
417	6879104	LOADING GEAR ASSEMBLY (R)
423	6879093	LOADING GEAR ASSEMBLY (L)
424	7390551	PLATE
425	6887322	FRONT HOLDER
426	4500402	SHAFT
427	6879153	DOOR ARM
428	6301027	SPRING
430	6879182	GUIDE PIECE
501	5457471	UPPER CYLINDER
502	5457481	LOWER CYLINDER
503	5792631	BRUSH
950	7541395	SPECIAL SCREW
951	8691408	BIND HEAD TAPPING SCREW 3MMD X 8MM
952	8741408	SCREW (B3X8)
954	7781133	BT SCREW 3MMD
955	8691408	BIND HEAD TAPPING SCREW 3MMD X 8MM
956	8691408	BIND HEAD TAPPING SCREW 3MMD X 8MM
958	8691408	BIND HEAD TAPPING SCREW 3MMD X 8MM
959	7773083	SCREW
960	8741408	SCREW (B3X8)
961	8812114	WASHER - 3MMD SMALL
962	8650412	SCREW 3X12 WITH SPRING WASHER
963	8821114	3D NUT
964	8741103	SCREW(2X3B)
965	7781872	SCREW-3MMDX8MM
966	7773086	SCREW
967	8741414	BINDING SCREW - 3MMD X 14MM
968	8821114	3D NUT
969	8741408	SCREW (B3X8)
970	8691408	BIND HEAD TAPPING SCREW 3MMD X 8MM
971	8691408	BIND HEAD TAPPING SCREW 3MMD X 8MM
972	8691312	BT BIND SCREW-2.6MMDX12MM
975	8699410	BT BIND HEAD SCREW 3MMD X 14MM BLACK
976	7782781	SCREW 3X8BT

SYMBOL-NO	P-NO	DESCRIPTION
977	8691408	BIND HEAD TAPPING SCREW 3MMD X 8MM
978	8741408	SCREW (B3X8)
979	8650408	SCREW
980	8741406	BIND SCREW - 3MMD X 6MM
983	8741403	BIND SCREW-3MMDX3MM
985	8671406	DT SCREW-3MMDX6MM
986	8678405	DT SCREW-3MMDX5MM (BLACK)
988	8691410	SCREW
989	8711103	PAN HEAD SCREW 2X3
990	8741406	BIND SCREW - 3MMD X 6MM